Low-noise 3-D Bending Pixel Transistor for Small Pixel CMOS Image Sensors

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Abstract— We demonstrated a low-noise back-illuminated CMOS image sensor, employing a three-dimensional (3-D) vertical gate structured bending transistor for in-pixel source-follower (SF) amplifiers. The 3-D gate structured SF was simply formed by adding a field oxide recess process near the channel region. To maximize the effective channel area, a considerate 3-D gate structure into a bending-type SF was devised. Firstly, the vertical gate structure was partially adopted on the current path in bending-SF. Three different types of 3-D bending SF were compared in terms of trans-conductance (g_m) and the effective channel width (W_{eff}). Then, in an optimized SF structure, the g_m and W_{eff} were improved up to 9% and 20%, respectively, compared to the planar bending-SF. This leads to the reduction of temporal random noise by 2% compared to the planar one. Furthermore, as the depth of vertical gate increases from $0.63\times W$ to $0.88\times W$, where W is the width of planar channel, the random noise decreased more by 7%. Finally, the wafer-level random telegraph signal (RTS) noise was evaluated and it decreased about 62% compared to the planar one. We expect this result to accelerate the scaling down of a pixel pitch which is crucial for high-resolution image sensors in the future mobile market.

Keywords—CMOS Image Sensors, Vertical gate transistors, Source follower amplifiers, Bending transistor, Random noise, Thermal noise, Flicker noise, Temporal noise, Random Telegraph Signal Noise, RTS

I. INTRODUCTION

CMOS image sensor (CIS) industry have moved fast toward small-pitch and high-resolution sensors due to strong demand from growing mobile markets for the past several years. To make pixel pitch smaller, transistors in each pixel have been rapidly scaled down as well [1, 2]. However, such scaling of in-pixel transistors inevitably deteriorates their own electrical characteristics, such as trans-conductance (g_m) and leakage current, which leads to deterioration in image quality of CISs [3, 4]. In particular, a source follower (SF) amplifier transistor is of utmost importance as it determines several important characteristics of sensor including linearity and noise performances. For instance, as the channel length of SF transistor decreases, the short channel effect, i.e. drain-induced barrier lowering *(DIBL)*, results in non-linear SF gain in dynamic light range. In addition, the smaller the SF channel area is, the more severe temporal signal fluctuation becomes as it originates from the interface traps at the SF channel area. Therefore, there have been consistent efforts to maximize the effective channel area of SF in a given pixel area [5, 6].

In this work, we firstly demonstrated 3-D bending SF transistors in a *0.5 μm* pitched *64 Mega-pixels'* image sensor. By adopting a bending SF rather than a conventional straight SF, the longer effective channel length (L_{eff}) was achieved in a same footprint. Then, to maximize the effective channel width (W_{eff}), a 3-D vertical gate structure was introduced to a bending transistor. In particular, a 3-D gate structure was needed to be considerately optimized for a bending SF as the current path in bending SF is not uniform like that in the conventional straight SF.

II. DEVICE FABRICATION

We fabricated a 4-transistor active pixel sensor (4-T APS) as shown in Figure 1(a). In order to maximize the SF area within the limited pixel pitch, a bending SF was adopted instead of a conventional straight SF. By adopting a bending SF, the longer effective channel length ($L_{Bending}$) was achieved compared to that of the conventional straight SF ($L_{Straight}$) in a same foot-print as shown in Figure 1(b).

Then, to maximize the effective channel width (W_{eff}), a 3-D gate structure was adopted to a bending SF transistor. The 3-D gate structure was simply formed by replacing a field oxide near the channel to a vertical gate stack. A fabrication processes added from a planar SF, to form a 3-D gate, are illustrated in Figure 1(c). First, the p-type doped active Si was defined by the shallow trench isolation (STI) for a channel of SF. Then, a hard

mask and a photoresist are patterned by a photolithography to define a 3-D vertical gate region. To recess a field oxide in a vertical gate region, dry etching process was conducted followed by removal of hard mask and photoresist. Then, a gate oxide was grown by a thermal oxidation for both regions of vertical gate and planar gate. Finally, a Poly-Si was deposited and patterned followed by metallization.

In particular, a considerate 3-D gate structure was needed to maximize its effective channel area, as the current density in bending SF is not uniform like in conventional straight SF. We carefully optimized a 3-D gate layout considering the current path in bending SF. First, we found that a Bi-gate structure, shown in Figure 1(d), is more efficient to maximize the effective channel area in bending SF than a Tri-gate structure. Then, we further optimized the Bi-gate layout precisely for a bending SF. Three different vertical gate layouts of bending 3D-SF (1), (2) and (3) were fabricated and evaluated in terms of noise performances. Also, a depth of vertical gate was investigated in an optimized bending 3D-SF layout.

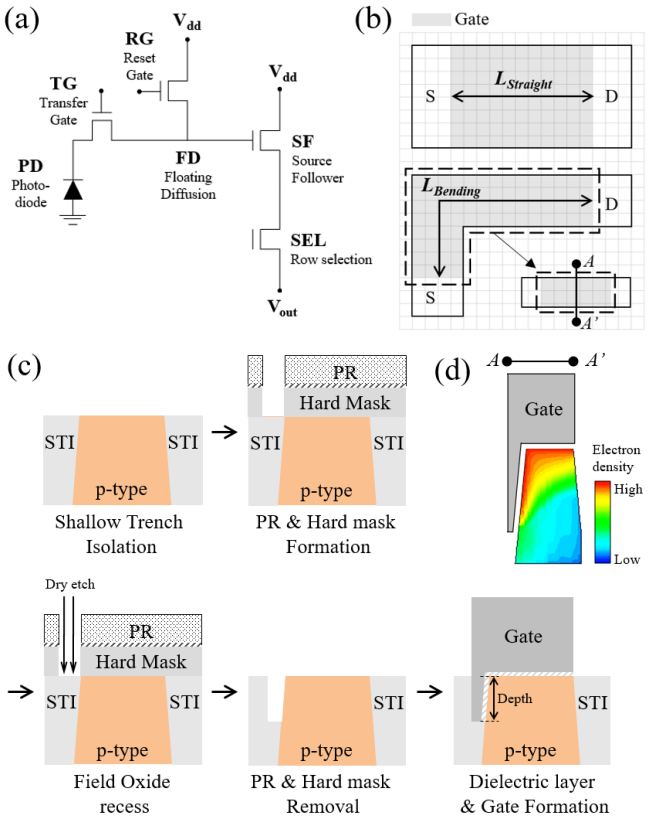

Figure 1. A schematic illustration of (a) pixel representation, (b) straight and bending in-pixel source follower (SF) transistor. (c) The fabrication process to form a 3-D gate structure into a bending SF. (d) The schematic illustration of a Bi-gate 3-D bending SF at A-A' cross-section with an electron density.

III. Results and Discussion

The fabricated 3-D bending SFs were electrically characterized by the test element structures, which are placed adjacently to the actual pixel arrays. Typical transistor performance metrics, such as threshold voltage, sub-threshold swing and DIBL, show that the gate-controllability of 3-D bending SF was much improved than a planar one. However, the trans-conductance (g_m) at the actual pixel operation conditions was more importantly considered in terms of pixel linearity and noise performances of sensors considering that SF amplifiers are operated at saturation mode,

In Figure 2(a), the fabricated bending SFs, 3D-SF (1), (2) and (3), were compared in terms of g_m with a fixed depth of vertical gate as $0.63\times W$, where W is the channel width of planar SF. It shows that the g_m in 3D-SF (3) was most improved up to 9% compared to the planar one. On the other hand, the 3D-SF (1) shows rather decreased g_m compared the planar one by 13% and the 3D-SF (2) shows comparable g_m to the planar one.

Then, the effective channel width, W_{eff}, was also estimated by using the Equation (1).

$$W_{eff} = \frac{L\cdot(g_m{}^2)}{2\mu C_{ox} I_{bias}} \qquad (1)$$

Assuming the channel length is constant in all structures, approximately ~20% of W_{eff} was improved in 3D-SF (3) compared to the planar one in Figure 2(a).

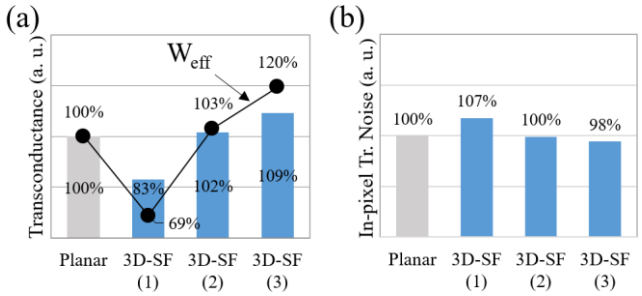

Figure 2. Comparison of (a) trans-conductance (g_m) and (b) total in-pixel transistor temporal noise between planar bending SF and 3D-bending SF (1)~(3) with a vertical channel depth of $0.63\times W$.

This result led to the improvements in noise performances. In Figure 2(b), only 3D-SF (3) shows ~2% of reduction of in-pixel transistor temporal noise. Meanwhile, other structures show comparable or rather increased noise level compared to the planar one. For the details, in 3D-SF (3), ~2% of thermal noise and ~1% of flicker noise were reduced compared to the planar one. Generally, the thermal noise and flicker noise are mainly

governed by g_m ($\propto \sim g_m$) [7] and area *(~1/(W×L))* [7] of channel, respectively. Even though, the g_m and W_{eff} in test element above cannot be exactly same in actual pixel operation, this improvement is mainly understood by the improvement in g_m and W_{eff}. It implies that an appropriate gate structure, i.e. like 3D-SF (3), is needed to improve g_m the noise performance in bending SF.

The effective channel length (L_{eff}) and the consequential effective channel area also can be changed depending on the gate structure. However, considering a not uniform bending current density, it is hard to evaluate accurate values of them.

By using the optimized layout of 3D-SF (3), we further investigated the noise performance by increasing a depth of vertical gate. As the depth increase from *0.63× W* to *0.88× W*, the thermal noise and flicker noise were decreased by ~9% and ~4%, respectively, in Figure 3(a) and Figure 3(b). The total in-pixel temporal transistor noise was reduced approximately ~7% as the depth increase.

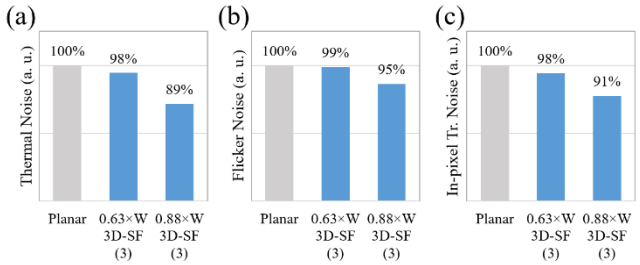

Figure 3. Comparison of (a) thermal noise, (b) flicker (*1/f*) noise, (c)) total in-pixel transistor temporal noise between planar bending-SF and 3D-bending SF (3) with a vertical gate depth of *0.63× W* and *0.88× W*.

These results are also shown in the distribution of pixel-by-pixel random noise in Figure 4 (a). The body of the pixel distribution is slightly narrower in *0.63× W* 3D-SF (3) than planar one. Then, it becomes narrower in *0.88× W* 3D-SF (3) and slightly left-shifted than planar one, which indicates the reduction of thermal noise. The tails of distribution also descend further as the depth increase, which suggest the flicker noise components are decreased.

The random telegraph signal (RTS) noise are also evaluated. Two consecutive frames of images were taken at a dark condition and the pixel-by-pixel output differences were plotted in histogram Figure 4 (b). First, the distributions near the zero difference was slightly reduced in 3D-SF (3) compared to planar one. And the slope of tails also becomes steeper in 3D-SF (3) than planar one, which means that the temporal current fluctuations have been lowered in 3D-SF (3). This can be understood by a general explanation of RTS *(~1/(W×L))* [8] and it corresponds to the improvement in flicker noise above.

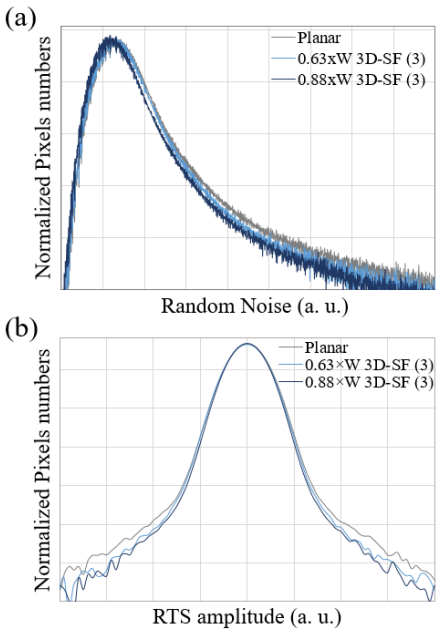

Figure 4. The distribution of pixel-by-pixel (a) temporal random noise (R.N.) and (b) Random telegraph signal (RTS) noise in comparison with planar bending-SF and 3D-bending SF (3) with a vertical gate depth of *0.63×W* and *0.88×W*.

In addition, we also evaluated the RTS noise in the wafer-level tests. In Figure 5, the RTS in y-axis represents the counted number of pixels in a chip that showed higher output differences than a certain criterion. In a wafer, the RTS of a considerable number of chips were obtained and the median value of them are presented in Figure 5.

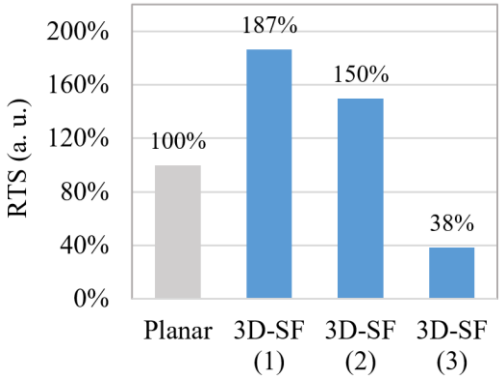

Figure 5. The wafer-level testing results of the Random telegraph signal (RTS) noise between planar bending-SF and 3D-bending SF (1)~(3) with a vertical gate depth of *0.63× W*.

In Figure 5(a), 3D-SF (3) shows ~38% of RTS value compared to the planar one. Meanwhile, 3D-SF (1) and (2) show much increased value. This dramatic result implies that 3D-SF (3) is promising option for a mass production of CIS chips.

IV. CONCLUSION

We firstly demonstrated a 3-D bending in-pixel SF transistor integrated into the submicron 4-T APS chip. By optimizing a 3-D gate structure suitable for a bending SF, the effective channel width of the SF transistor is maximized resulting in improved pixel noise characteristics without adversely affecting other pixel performance. This achievement may allow further scaling down of pixel pitch for the future image sensors of high-resolution applications without the inevitable deterioration of noise performance in a minimized SF area.

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