A 3.0µm-pixels and 1.5µm-pixels combined CMOS Image Sensor for Viewing and Sensing Applications with 106dB Dynamic Range, High-Sensitivity, LED-Flicker Mitigation and Motion Blur-less

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***Abstract*— We propose a new concept image sensor suitable for viewing and sensing applications. This is a report of a CMOS image sensor with Ta-Kuchi pixel architecture consisting of a 1.5µm pixel with four shared pixel structures and a 3.0µm pixel with in-pixel-capacitor. They are arranged in a staggered pitch. This architecture achieves both a High Dynamic Range (HDR) of 106dB and LED Flicker Mitigation (LFM) as well as Motion Artifact Free, and Motion blur less. As a result, moving subjects can be accurately recognized and detected with good color reproducibility in any lighting environment. This allows a single sensor to deliver the performance required for viewing and sensing applications.**

Keywords—CMOS Image Sensor, Automotive, HDR, LFM, Motion Artifact, Motion blur, Ta-Kuchi Pixel.

I. INTRODUCTION

Sensing and Viewing, especially in the automotive sector, must accurately perceive moving objects and obstacles and detect them with high color fidelity in all lighting conditions. For example, in order to recognize people, objects, and features even in dark places, it is necessary to sample images with high sensitivity and low noise. Also, Light Emitting Diode (LED) traffic lights should always appear to be on in the image, even if they are actually blinking. Extending the exposure time to catch flicker tends to saturate the signal, losing luminance and color information within the pixel. To solve these problems, several HDR techniques have been proposed that extend the exposure time to capture the flicker signal but do not saturate the signal.[1-4] However, extending the exposure time causes motion blur, which causes misrecognition. Based on these considerations, we propose an image sensor that is optimal for viewing and sensing, which combines color reproducibility and high dynamic range while maintaining sufficient resolution and eliminating the causes of misrecognition.

II. SENSOR ARCHITECTURE

A. New Concept

There are the following features for sensing and viewing applications. In dark, low-light, and high light environments, the signal is only needed to detect the presence or absence of objects, not the color information. And it is necessary to acquire the signal without saturating the signal even if the exposure time is extended enough for the flickering LED. Taking advantage of the difference in information required for luminance and color, we propose the Ta-Kuchi pixel shown in Figure 1. Incidentally, in Japanese Kanji, Ta-Kuchi is written 田口.So we named this structure Ta-Kuchi pixel because the shape of the pixel resembles 田-口.

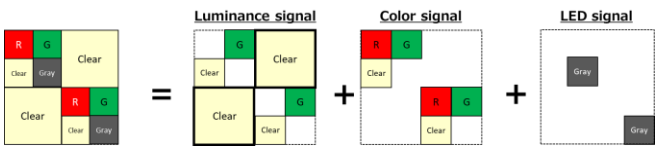


Fig. 1. Pixel configuration that realizes the concept

The color filter of the Ta-pixel consists of Green, Red, Clear, and Gray, and the color filter of the Kuchi-pixel consists of Clear. It specializes in acquiring luminance signals by using high sensitivity Green and Clear pixels in dark or low-light environments. In scenes that require color recognition in

medium illumination, the signals of the red, green, and clear pixels of the pixel are used. For LED signal acquisition, low sensitivity gray filter pixel signals that are difficult to saturate even with long exposure are used.

B. Sensor Configuration

The Ta-Kuchi pixel arrangement method is a staggered pitch arrangement as shown in Figure 2. The number of pixels is 4.61Mpixel for Ta pixels and 1.15Mpixel for Kuchi pixels. This makes it possible to obtain twice the resolution in color and luminance information compared to the 2.2Mpixel of the usual 3μm pitch pixel array.

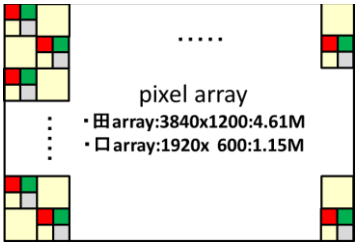


Fig. 2. Pixel array

A Ta-Kchi pixel is a combination of a 1.5μm pixel with a 4-pixel sharing configuration and a Kuchi pixel of a 3μm pixel with in-pixel Floating Capacitor(FC). Figure 3 shows a cross-sectional view of a Ta-Kuchi pixel. The shape of on-chip micro lens (OCL) is arranged in the same shape with Ta-Kuchi pixels. The light attenuation rate of gray pixels is controlled by the thickness of the gray filter and the opening width of the Light Shielding layer. In a Kuchi pixel, the area of photodiode (PD) and the FC are the same.

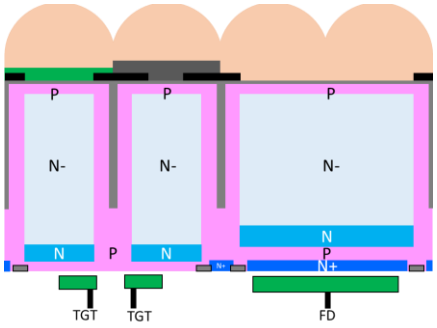


Fig. 3. Cross-Section of Ta-Kuchi Pixel

C. Pixel Circuit

Figure 4 shows the pixel circuit.

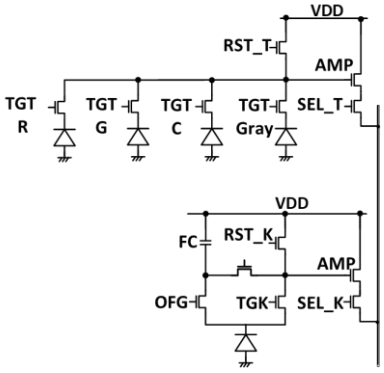


Fig. 4. Pixel Circuit

A Ta pixel consists of four photodiodes, four transfer transistors (TGT), a reset transistor (RST_T), a selection transistor (SEL_T), and a source follower amplification transistor (AMP). Four pixels are connected to one FD. A Kuchi pixel consists of one photodiode, a transfer transistor (TGK), an overflow gate (OFG), a reset transistor (RST_K), a selection transistor (SEL_K), a source follower amplification transistor (AMP) and in-pixel floating capacitor (FC).These drive lines are connected in a zigzag pitch from the vertical scan drive circuit for the Ta pixels and the Kuchi pixels.

D. Pixel Read-out Method

Figure 5 shows the read timing sequence. The signals of the Kuchi pixels and the signals of the Ta pixels are read out continuously. The Kuchi pixel signal has two modes: a mode for reading out the charge of the photodiode with low noise due to its high conversion gain, and a mode for reading out the charge overflowing from the charge of the PD and the charge of the FC. Two rows are read out with 8AD in a 1H period by combining long exposure time readout and additionally short exposure time readout.

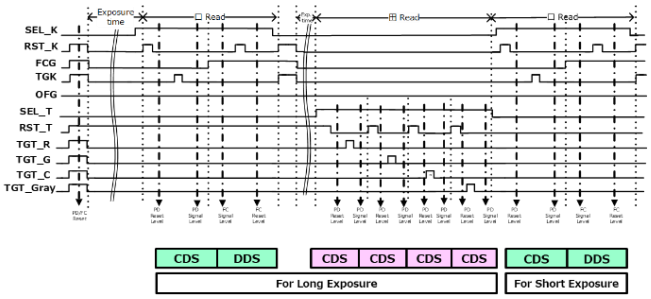


Fig. 5. Timing Sequence

In Kuchi Pixel, two types of signals are read-out in a single exposure. First, an exposure of Kuchi PD and FC begins by the reset of PD and FC. Then, Kuchi PD reset level is sampled and next the PD signal level is sampled. By performing correlated double sampling (CDS) for reset and signal level, signal are read-out. Subsequently, the signal that comes from FC is read-out by performing delta reset sampling (DRS): FC, in which the signal level is sampled first, followed by the reset level . Because the signal charges are accumulated in FD, FD cannot be reset prior to sampling the signal level. The flaw of DRS is that kTC noise cannot be removed; however, it can be suppressed by securing the capacitance of FC sufficiently. Subsequently, the Ta pixels Red, Gray, Green, and Clear are sequentially read out. Finally, read out the Kuchi pixels accumulated for short exposure again.

III. SENSOR CHARACTERISTICS

A. Ta Pixel Characterristics

Fig. 6 shows the output against the light intensity of the Ta pixel.

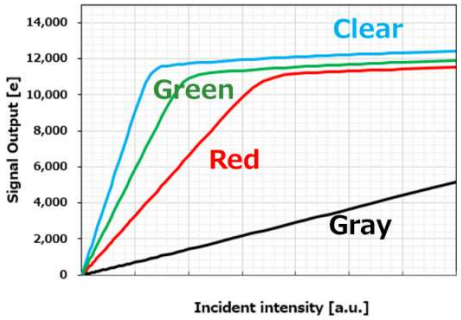


Fig. 6. Photo response of Ta pixels

Ideal linearity is achieved with respect to the amount of light for all colors. Minimum linear full-well capacity (FWC) is 9400e-, and random noise (RN) is 1.4e-.

FIG. 7 shows the quantum efficiency for each wavelength of clear pixels, green pixels, red pixels, and gray pixels. Clear pixels show up to 82%. Fig. 8 shows a Macbeth chart taken using this pixel with a light source of 6500K. Exhibits high color reproducibility. Also, the sensitivity of the gray pixel for LED is 550e-/lux·sec, which is 1/20 of the clear pixel sensitivity of 10800e-/lux·sec. As a result, the Dynamic Range for Gray pixels is 103 dB, and the illuminance saturation is 5600 cd/m2 after 11 msec accumulation. It is said that it takes 10msec or more to capture the flicker signal of the LED, and the saturation illuminance is said to be 4000cd/m2 or more, which are sufficiently high values. In addition, constant and stable quantum efficiency is obtained for wavelengths in the visible light region.

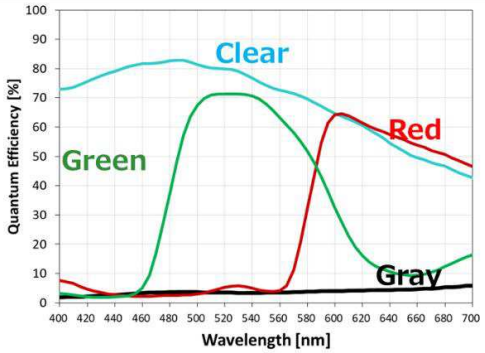


Fig. 7. Quantum efficiency (Ta Pixel)

Fig. 8. Macbeth chart

B. Kuchi Pixel Characterristics

FIG. 9 shows a cross-sectional view of a portion of a Kuchi pixel having a pixel transistor.

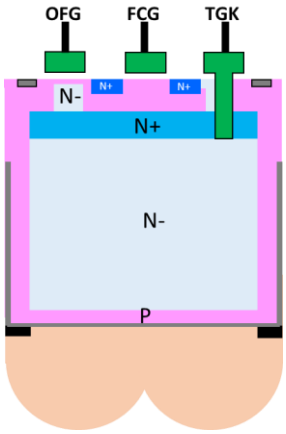


Fig. 9. Cross-Section of Kuchi Pixel

The PD signal transfer electrode TGK is a vertical Transfer Gate(VTG), and the overflow electrode to FC is a planar gate. By arranging VTG on the TGK side, it is possible to collect the charge generated in the photoelectric conversion area efficiently, which is almost the entire area of 3μm square area. The OFG side is a planar type so that the saturation charge can surely overflow to FC while minimizing the dark current generated in the PD and FC.

As shown in FIG. 10, PD saturation and Photo Response Non-Uniformity (PRNU) of FC have a trade-off relationship depending on the OFG voltage. As the OFG applied voltage increases, the PD saturation decreases, and overflow to FC becomes easier, so PRNU decreases. By setting it to -0.5V, sufficient saturation and PRNU reduction are achieved. The dark current can be sufficiently suppressed without depending on the OFG voltage.

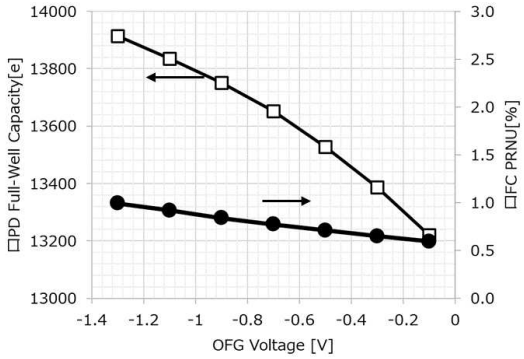


Fig. 10. OFG dependency FWC and PRNU

Fig. 11 shows the output against the light intensity of the Kuchi PD and Kuchi FC. The sensitivity is 40400e-/lx·s, the PD saturation is 13500e, and the PD+FC saturation is 280000e. Since RN is 1.4e, Dynamic Range is 106dB.

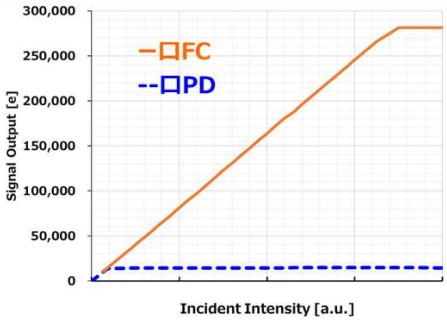


Fig. 11. Photo response of Kuchi pixels

Fig. 12 shows the illuminance vs. Signal to Noise ratio (SNR) when combining two types of signals with 10 msec accumulation and two types of signals with 0.16 msec accumulation.

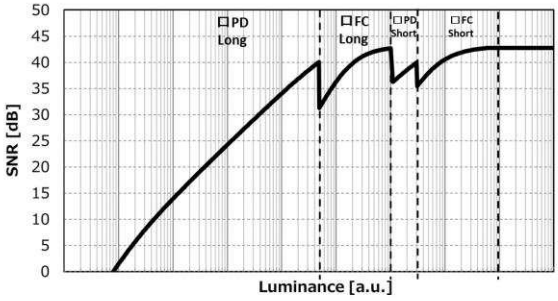


Fig. 12. SNR curve of synthesized signal

The high conversion gain signal is used in the low illumination area, and the PD+FC signal is used in the high illumination area. The SNR drop amount when connecting from the Kuchi PD to the Kuchi FC also maintains 30 dB at 85°C. The dynamic range from the SNR graph is 138dB when combined with 0.16msec short exposure.

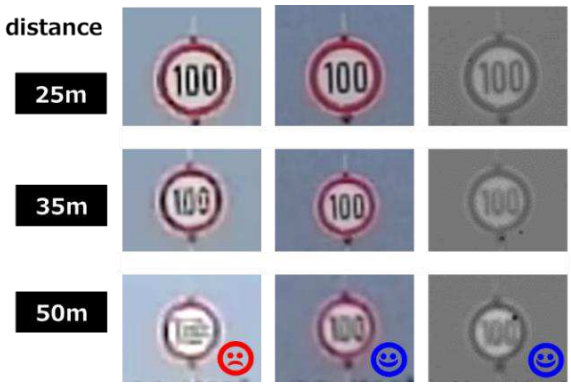
C. Synthesized Image

FIG. 13 shows an image of a moving object. In (a) is an image of one shot HDR in long exposure for LFM. Motion Blur occurs during exposure. In (b) is an image of Digital Overlap (DOL) HDR synthesis with time-division exposure, and motion artifact occurs. In (c) is an image of using Ta-Kuchi architecture. Motion Artifact Free and Motion Blur less are realized because it includes long exposure and short exposures with Kuchi pixel. This work uses motion detection. Each signals of the long exposure and the short exposure are compared for each pixel to determine whether there is a signal difference. At this time, the short accumulation Kuchi signal is multiplied by the exposure ratio gain for comparison. If there is a difference, the short exposure signal is selected, and if there is no difference, the long exposure signal with low noise is selected. In this way, motion detection is performed for each pixel and synthesized.

(a)one shot HDR (b)DOL HDR (c)This work

Fig. 13. Image of a moving object

Figure 14 shows the road signs captured at 25m, 35m, and 50m distances.



(a)3µm pixel Bayer (b)2.25µm pixel Bayer (c)This work

Fig. 14. Image of a road sign

(a) shows image captured using a Bayer array with 3um pixel, and cannot read numerical values 50m away. (b) shows image captured using a Bayer array with 2.25µm pixel. With this pitch, the numerical value 50m ahead can be read. (C) shows image captured using a Ta-Kuchi architecture. This performance equivalent to the 2.25µm Bayer array. In principle, interpolation with a Bayer array has limits on the performance of demosaic processing. A direction detection error occurs every frame. In this work, thanks to the array of 1.5µm pixels, there are clear pixels in all pixels within the 3µm pitch. Horizontal, vertical, and diagonal edge detection is easier than the 3µm pitch Bayer array, and aliasing is improved. This also improves resolution.

FIG. 15 shows a composite image of Ta-Kuchi pixels at 22 msec exposure. (a) is an image in which green, red, and clear pixels of Ta pixel are used as color signals and clear pixels as luminance signals. Ideal image quality without line defects due to complicated drive lines. The resolution is high enough to read numbers.(b) is an image of Gray Filter. Image quality without unevenness is obtained.

(a)口 PD+FC+田 RGC Image (b)田 Gray Image

Fig. 15. Synthesized Image

IV. CONCLUSIONS

TABLE1 shows pixel performance.

TABLE1 Pixel performance

		Unit	Ta 田	Kuchi 口
Power Supply		V	2.9/1.8/1.2	
Process Technology		-	90nm 4Cu 1AL	
Pixel pitch		µm	1.5	3.0
Pixel Array		pixel	4.61M	1.15M
Color		-	Red,Green,Clear,Gray	Clear
HDR Technology	Sensitivity ratio	times	20(Gray)	non
	in-pixel capacitor	-	Non	MOS
Random noise@RT		e- rms	1.4	1.4
Sensitivity(3200K with IR cutfilter)		e-/lx·s	10800 (Clear)	40400
Full-well Capacity		e-	9.4K	280K
Real-Full-well Capacity		e-	188k(Gray)	280K
Dynamic Range(SingleExp.)		dB	103(Gray)	106

We have developed a new image sensor using new concept 田口 pixel architecture for Viewing and Sensing applications with 106dB DR, LFM, Motion Artifact Free and Motion Blur-less.

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Automotive CMOS Image Sensor Family with 2.1µm LFM Pixel, 150 dB Dynamic Range and High Temperature Stability

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This paper presents an image sensor family for automotive applications. The sensors have a 2.1 µm pixel with overflow to a low gain capacitor, a triple gain readout and light flicker mitigation (LFM). The single exposure (flicker free) dynamic range is 110 dB and the SNR stays above 25 dB at each of the transition points up to 125°C. By adding a second exposure the dynamic range reaches up to 150 dB. The family currently consists of an 8.3 MP and a 3 MP sensor. More resolutions will be added.

Motivation

The most common techniques for extending the dynamic range of an image sensor are multiple exposure [1-3], dual photo diode [4-6] and overflow [7-11] or a combination of these. Multi exposure combines images with different integration times which causes artefacts on moving objects or pulsed light sources. The case with pulsed light sources is of particular interest for automotive applications as traffic signs and taillights of cars often use pulsed LEDs. The dual photo diode approach allows for a high flicker free dynamic range but loses sensitivity on the large photo diode, does not scale well to a smaller pitch and the consistency of color and MTF between the diodes is an issue. Therefore, our sensors use overflow from a single photo diode onto a very large capacitor. The sensors aim at automotive applications both in pixel specifications and in sensor features. A high single exposure dynamic range and good performance at high temperature are two key elements. A second short integration time can increase the dynamic range up to 150 dB. Flickering light sources will no longer cause artefacts when the long integration time has sufficient dynamic range to capture them unsaturated. 110 dB covers almost all use cases.

Test chip characterization data and initial data from the 8.3 MP product were presented in [11]. This paper presents characterization data over temperature from the product and focusses on one particularly challenging aspect: the trade off between DSNU, full well charge and blooming at high temperature.

Pixel design, operation, and performance

Figure 1 shows the pixel schematic. It is an overflow pixel with an additional dual conversion gain (DCG) transistor for a medium gain. The pixel combines overflow to a low gain capacitor with a triple gain readout. The low gain capacitor is a trench MiM that allows for a full well charge of 600 ke⁻. This high capacitance results in a substantial read noise due to its kT/C noise and a degraded input referred read noise because of the low charge to voltage conversion gain. This read noise is the dominant noise contribution on the low gain read up to high temperature. The floating diffusion DSNU is highly optimized and at 10 ms integration time it only dominates over the read noise at the 125 °C data point.

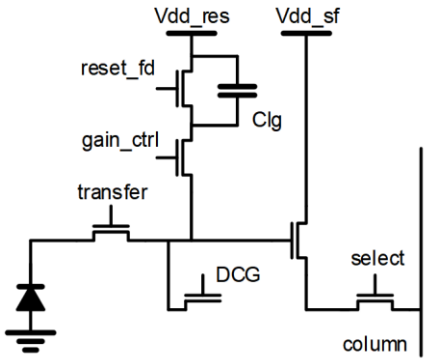

Figure 1: Schematic of the pixel. Clg is an MiM overflow capacitor. The dual conversion gain transistor (DCG) can add capacitance to the FD for the medium gain.

Figure 2 shows a simplified timing diagram for the operation with a triple gain T1 read and a low gain T2 read. Each of the three T1 reads has a response starting from the origin. Signal charge is not reset in between the reads. The gain is lowered going to the next read and more signal charge is added. Eventually the low gain read contains all charge from the PD and the overflow capacitor. The high gain PD read uses correlated double sampling and 4x analog gain to minimize noise. The other reads are double sampling reads.

Figure 3 shows the measured SNR for multiple temperatures. The transition SNRt stays around 30 dB at each of the transitions up to 100°C. At 125 °C the SNRt at the transition between the PD and the overflow read still maintains a level around 25 dB. The SNRt at the transition between the T1 overflow read and T2 does not change significantly with temperature. It is mainly a function of the integration time ratio. This ratio can be chosen at runtime and trades SNRt for total DR. The figure shows the curves for a ratio of 70 which results in an SNRt slightly below 30 dB and a total DR of 146 dB. When the focus is on higher SNRt a ratio of e.g. 44 results in an SRNt of 32 dB and a total DR of 143 dB. With focus on higher DR e.g. a ratio of 100 results in an SNRt of 26 dB and a total DR of 150 dB.

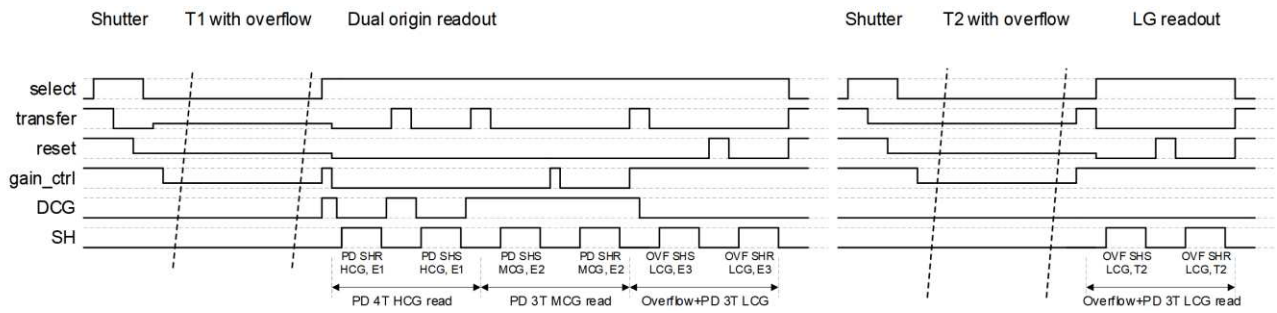

Figure 2: Timing diagram of the overflow T1 with triple gain origin mode read and overflow T2 with low gain read. The overflow T1 is also referred to as a "Super-Exposure" (SE) as it combines signals from multiple in pixel readout gains and covers a very wide DR.

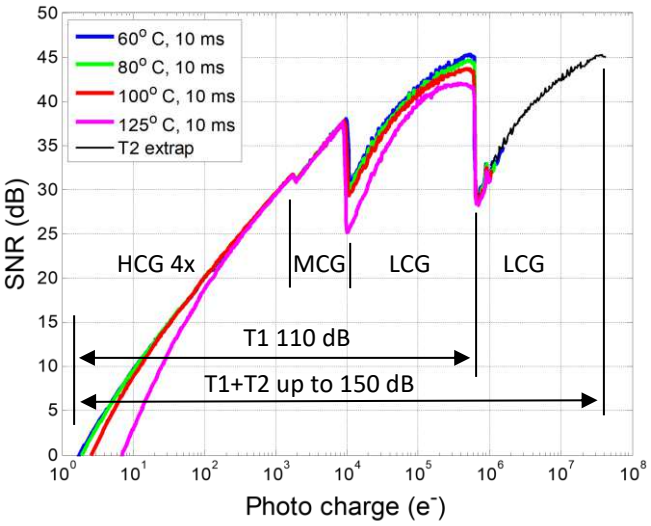

Figure 3: Measured SNR of the 8.3 MP sensor as a function of exposure. Clear pixel, red light spectrum. Super-Exposure T1 and low gain T2, T1/T2=70. The T2 range beyond the maximum power of the available light source is extrapolated form the T1 overflow measurement.

These SNR curves show that these devices are designed for high temperature operation. The performance at 60 °C and 80 °C is almost indistinguishable and at 100 °C there is only a minor degradation of SNR1. At 125 °C the SNR1 degrades noticeable due to increased PD DSNU but is on par with our same pixel size multi-exposure sensor which is state of the art and has a much simpler pixel operation. The PD DSNU has improved from the early samples by finetuning the blooming prevention mechanism. This has a trade-off that shows at the high end of the T1 overflow read where the peak SNR is a little lower at 125 °C. This is not due to DSNU as that would have no impact at such large signals. At very high temperature the sensor operates at the onset of blooming which results in increased PRNU. This is not an issue as the SNR is still over 40 dB. Also, the SNRt is hardly changing with temperature up to 100 °C since it is read noise dominated. Only at 125 °C FD DSNU dominates over the read noise.

Blooming optimization

The optimization for blooming free operation at high temperature was a very challenging aspect of this development. The pixel is processed with a partial backside deep-trench isolation (BDTI). This improves the optical properties, but unlike a full DTI does not prevent blooming between pixels. Blooming is controlled by a sufficiently conductive overflow path.

Usually blooming occurs when the photo diode is full and additional photo generated charge spills over to a neighboring pixel. In an overflow pixel charge overflows to the low gain capacitor at this point. This is normal operation. When the overflow capacitor also saturates charge must overflow over the reset_fd device to the supply. This proved to be the most critical condition for the optimization. A "waterfall" must be created from the PD to the FD, Clg and Vdd_res. Setting the low-level voltages on transfer, gain_ctrl or reset_fd higher than strictly needed will reduce the available swing (full well charge) and increase DSNU at the respective location. Similarly, a higher Vdd_res can reduce blooming and increase available swing but will also increase DSNU. The transfer gate turned out to be the most critical location for controlling the blooming even though the blooming only occurs when Clg saturates.

In the early samples the blooming was controlled by pixel timing and increased low level voltages. That works well to control the blooming, but it increases the PD DNSU which is a problem at high temperature. This was improved by optimizing the layout and implant scheme of the buried channel "anti-blooming" overflow path under the transfer gate such that it conducts sufficiently while keeping the transfer gate in the "off" state. Figure 4 shows a drawing of the buried channel path under the transfer gate which can be thought off as a grounded JFET in parallel to the transfer gate. The operation depends on the sub-threshold current of the device which turned out to be very sensitive to layout, not only of the transfer gate itself, but also nearby implants like isolations. Maximizing the width of the anti-bloom path and removing neighboring isolation implants maximized the current handling without sacrificing too much PD full well charge.

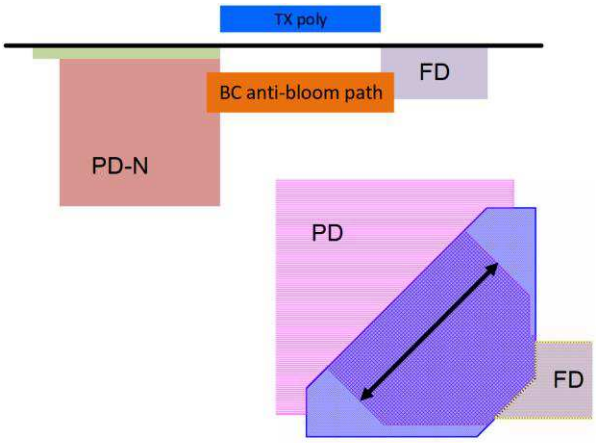

Figure 4: Concept drawing of the buried channel anti-bloom path. This path allows charge to overflow from the photo diode to the floating diffusion while the transfer gate is kept in the "off" state. The arrow in the layout view indicates the width of the anti-bloom path under the transfer gate.

Blooming PRNU metric

The trade-off between full well charge, DNSU and blooming requires a good way to quantify blooming. This led to the introduction of a new metric for blooming in the overflow regime: blooming PRNU

Traditionally, blooming is quantified by a slope change in the response of the slow color channel after saturation of the dominant color channel. However, this metric does not correlate well with image quality. Even without a slope change the image quality can be degraded by outlier pixels that are already blooming and can show up as colored spots. Therefor we introduce a new metric for blooming based on fixed pattern noise: blooming PRNU. Blooming PRNU quantifies how the fixed pattern noise in the slow channel scales with the illumination of the dominant channel.

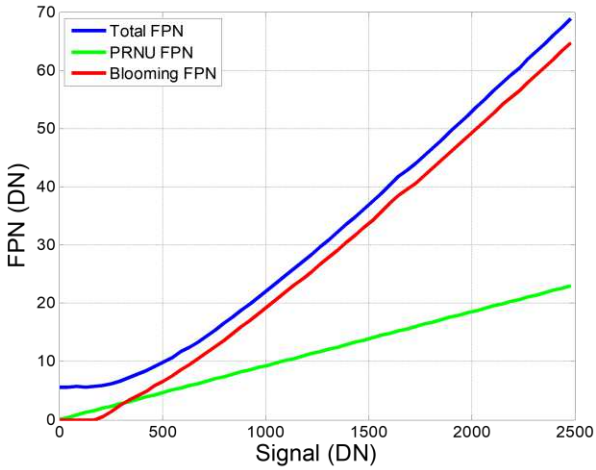

Figure 5: FPN contributions on the slow color channel (red pixel, cyan light spectrum, RGGB CFA) as a function of slow channel signal. Example sensor with blooming at 125 °C. The red curve is the blooming FPN which scales with the (extrapolated) dominant channel signal (green pixel).

There are a few caveats: not all fixed pattern noise in the slow channel is due to blooming and the dominant color channel is saturated in the region of interest so an extrapolated value must be used. The fixed pattern noise in the slow channel is the sum of the dark FPN (including dark current non-uniformity), the PRNU of the response of the slow channel itself and the "blooming FPN". Figure 5 shows an example of the FPN contributions of the slow channel for a sensor with some blooming. Blooming is measured with cyan light to excite the blue, green and/or clear color channels. The red color channel is the victim in which blooming is measured. These measurements are done at 125 °C since this is the worst case.

The blooming FPN of the slow channel scales with the (extrapolated) response of the dominant color channel. Hence, the blooming PRNU is given by:

$$Blooming\ PRNU = \frac{\sqrt{FPN^2 - (dark\ FPN)^2 - PRNU^2}}{extrapolated\ dominant\ channel\ response}$$

Figure 6 shows the blooming PRNU for several test chip and product samples with two types of CFA. The blooming PRNU threshold for excellent image quality is around 1%. The product is with both types of CFA well below this 1% at 125 °C.

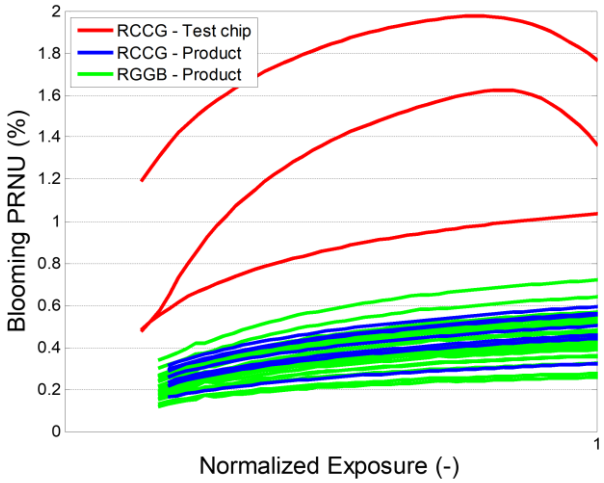

Figure 6: Blooming PRNU at 125 °C as a function of normalized exposure for some example pixel types from the test chip and multiple samples of the product. The exposure is normalized to the maximum cyan output power of the light source. This oversaturates the dominant channel by 4-6x depending on the CFA.

Discussion

The sensors provide 110 dB of single exposure dynamic range and up to 150 dB of total dynamic range with two exposures. The single exposure dynamic range is covered by a long T1 integration time of e.g. 10 ms. It has some motion blur which is inevitable with a long integration time, but it does not have motion artefacts due to combining data from several time shifted integration times. More importantly, in case of

flickering light sources like LED's, the long integration time will capture at least one light pulse so that light source is never perceived as "off" [10]. At an integration time of 10 ms, the 600 ke⁻ FWC is sufficient to capture almost all automotive LED flickering sources without saturation. This is important for correctly capturing traffic signs and traffic lights. The dynamic range between 110 dB and 150 dB is covered by a second (very short) integration time. This T2 in the sub-millisecond range will mainly capture non flickering highlights like the sun and its specular reflections.

The total dynamic range of 150 dB is sufficient to simplify the camera exposure control. In most practical situations the integration time can be fixed. This reduces the system latency since the exposure control does not need to settle after a change in the scene.

The sensors have dual outputs with windowing and scaling. This allows combining an advanced driver-assistance system (ADAS) camera and viewing camera into one device, reducing system cost. A typical use case for the 8.3 MP sensor is the output of a full resolution 8.3 MP image for ADAS combined with a lower resolution (e.g. 2 MP) for viewing applications.

Table I summarizes the sensor properties and finally figure 7 illustrates the image quality in two extreme illumination cases.

Optical format	1/3.7" (3 MP), 1/1.8" (8.3 MP)
Pixel array	1920 (H) x 1536 (V) = 3 MP 3840 (H) x 2160 (V) = 8.3 MP
Color Filter Array	RGGB, RCCB, RYYCy
Pixel pitch	2.1 µm
Linear Full well	1.5 ke⁻ (E1 at 4x gain), 10 ke⁻ (E2), 600 ke⁻ (E3)
Read noise @ 80ºC	180 µV (E1), 2 mV (E2), 520 µV (E3)
Single exposure DR	110 dB (SNR1 based at 80 °C)
Total DR (T1+T2)	150 dB (for T1/T2=100)
Transition SNRt	30 dB at 80°C, 25 dB at 125°C
Max frame rate (8.3 MP)	45 fps T1+T2 at 26 bit companded to 16 60 fps T1 at 20 bit companded
Supply voltage	2.8 V, 1.8 V

Table I. Sensor properties and performance

Conclusion

Every aspect of this sensor family is designed with automotive applications in mind. Both the feature set and pixel performance aim at reducing the system complexity. Good high temperature performance and an extended flicker free and total dynamic range are key for obtaining high safety levels.

Up to 80°C the performance is almost indistinguishable from room temperature and at 100°C there is only a very minor increase of SNR1. Even at 125°C, which most competitors don't report, good image quality is maintained with an SNRt above 25 dB at each of the transitions.

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Figure 7: Outdoor images with local tone mapping of the 3MP sensor.
Left: 2 ms integration time with direct sun light. Right: 30 ms integration time on a moonless night.

Automotive 2.1 μm Full-Depth Deep Trench Isolation CMOS Image Sensor with a Single-Exposure Dynamic-Range of 120 dB

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***Abstract*— An automotive 2.1 μm single exposure CMOS image sensor has been developed with a full-depth deep trench isolation and an advanced current readout circuit technology. To achieve a high dynamic range, we employ a sub-pixel structure featuring a high conversion gain of a large photodiode, and lateral overflow of small photodiode connected to in-pixel storage capacitors. The expanded dynamic range could reach 120 dB at 85 °C by realizing low random noise of 0.83 e- and high overflow capacity of 210 ke-. Over 25 dB signal-to-noise ratio is achieved at the transition point by increasing the full-well capacity of the small photodiode of up to 10,000 e- and suppressing the floating diffusion leakage at 105 °C.**

Keywords—Automotive, HDR, F-DTI, sub-pixel structure.

I. INTRODUCTION

High dynamic range (HDR) is a primary requirement for automotive image sensors to capture not only both bright and dark regions in a single scene, but also the light-emitting diodes (LEDs) lighting signals of transportation environments. One way to expand the dynamic range (DR) is to use the multiple exposure method.[1] However, the sequential image capture causes motion artifacts, and the short integration time results in LED flickering. Thus, a single-exposure with the longer integration time is necessary along with HDR. The lateral overflow integration capacitor (LOFIC) technology can cover the long exposure time by storing the excess photoelectrons in a large in-pixel capacitor.[2-4] The high-capacity MOS and metal-insulator-metal capacitors are widely used, and the unit capacitance of the in-pixel capacitors is known to be around a few 10 fF/μm^2.[1]

The single photodiode (PD) with LOFIC has achieved a single-exposure DR of 110 dB,[3] whereas LOFIC combined with sub-pixel structure can expand DR up to 120 dB in a single exposure.[4] The spatial sampling with a high sensitivity ratio between a single large PD (LPD) and a single small PD (SPD) enables to expand DR. As the pixel size gradually shrinks for higher resolution, this sub-pixel architecture not only faces a critical limit where DR is no longer expanded due to the restricted pixel area for the in-pixel capacitor, but also noticeably deteriorates SNR during the signal transition between the two PDs. The high-density in-pixel capacitor approach could overcome the former restriction.[3, 6] However, such scaling makes the SNR degradation as a result of a small full-well capacity (FWC) of the PDs.

Despite the restrictions, here, we have developed a 2.1 μm CMOS image sensor incorporated with a sub-pixel structure by applying the full-depth deep trench isolation (F-DTI) technology. A 120 dB single-exposure DR is achieved at 85 °C by using a storage capacitor in a pixel. By increasing the FWC of the SPD and reducing the floating diffusion (FD) leakage current, the minimum signal-to-noise ratio (SNR) at the transition point is improved up to 25 dB at a junction temperature (T_j) of 105 °C. We believe that the integration of the F-DTI process into a pixel array accelerates reduction of the pixel pitch with the competitive HDR performance in the automotive image sensor technology.

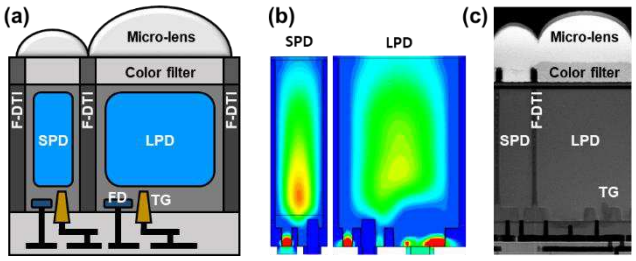

Figure 1. Cross-sectional views of (a) a 2.1 um sub-pixel structure, (b) simulated electrostatic potential profiles, and (C) a SEM image.

II. PIXEL DEISGN AND OPERATION

A. 2.1 μm F-DTI pixel

In general, the sub-pixel structure with the high sensitivity of an LPD and the low sensitivity of an SPD is fabricated to cover a wide range of light levels from the dark to the bright environments. As the pixel size shrinks, the conventional back-side deep trench isolation (B-DTI) process is restrictive when applied to the sub-pixel structure due to the limitation of forming potential barriers between the PDs. Therefore, the larger FWC of the PDs with no blooming is not feasible; it is difficult to scale down with B-DTI pixel structure. In this work, however, F-DTI process was utilized to develop a physically isolated sub-pixel structure as shown in Fig. 1(a). The merits of the F-DTI are to prevent optical and electrical crosstalk, and to maximize the FWC of PDs without blooming.

A fully-depleted region of the F-DTI pixel can be extended to the deep-level of the silicon via high-energy n-type implantation, and the larger FWC of a SPD is demonstrated through the device simulation as shown in Fig. 1(b). On the front side of silicon surface, the transistors and FDs are separated by an additional p-well implantation, further enlarging the FWC of the buried PDs. The scanning electron microscope (SEM) image of the cross-sectional view for the

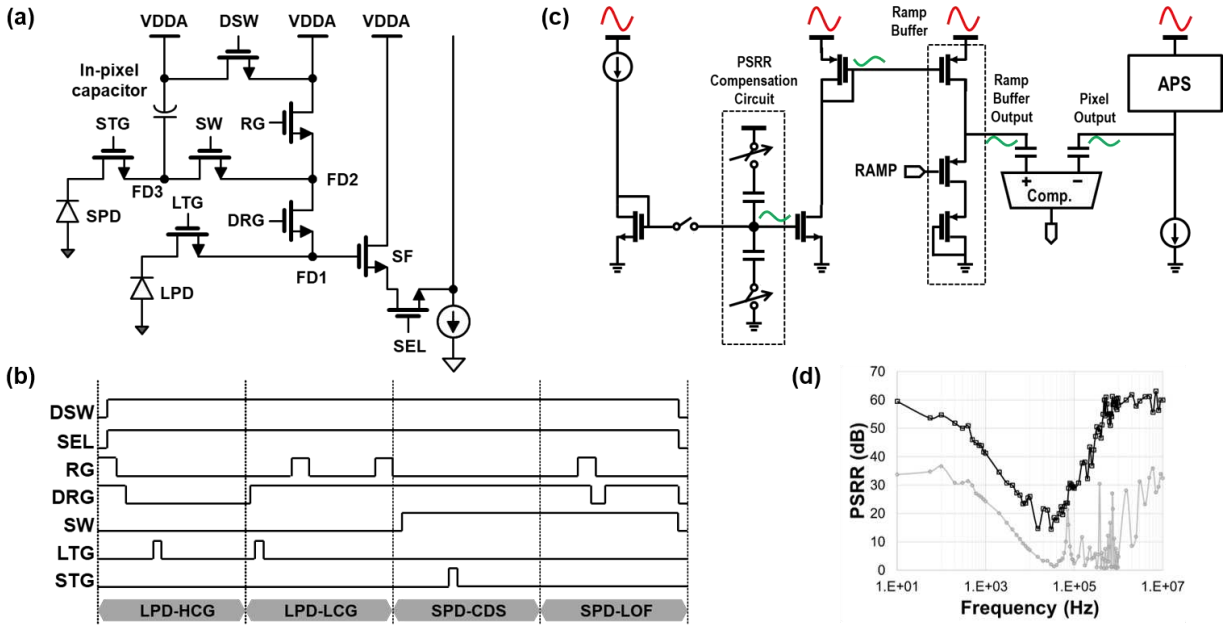

Figure 2. The proposed pixel circuit with readout timing: (a) a pixel schematic of the 2.1 µm F-DTI sub-pixel structure with in-pixel storage capacitor, (b) four readout timing diagram, (c) PSRR compensation concept diagram, and (d) the measured results before (gray) and after (black) applying PSRR compensation scheme.

2.1 µm F-DTI sub-pixel structure is shown in Fig. 1(c). With the vertical transfer gate (VTG) and the buried PDs, the FWC of SPD as high as 10,000 e- is realized in order to improve the SNR. The F-DTI pixel capped with a storage capacitor allows us to expand DR with lateral overflow operation. The capacitance of the overflow capacitor is more than 34 fF per pixel, allowing more than 210 ke- to be accumulated in a single exposure.

B. Pixel circuit and operation

Fig. 2(a) shows the pixel schematic of the 2.1 µm F-DTI pixel, consisting of two PDs, three FDs, eight transistors, and one storage capacitor. Using a DRG transistor, the LPD supports a dual conversion gain (CG) readout, and a low CG of SPD due to the capacitor can be switched by a SW transistor. When all transistors are turned on, every FD node is connected to the gate of a source follower (SF) amplifier, and then the circuit can operate in the readout mode of LOFIC signals. A DSW transistor is added to reduce the discharge time of the storage capacitor during the reset operation of the LOFIC signals. We implement a four-readout scheme: correlated double sampling (CDS) and incomplete CDS for both LPD and SPD. A simplified timing diagram is shown in Fig. 2(b). During the operation, the sequential readouts are performed with LPD-HCG (LPD with high CG readout), LPD-LCG (LPD with low CG readout), SPD-CDS (SPD with CDS readout), and SPD-LOF (SPD with LOFIC readout). CDS is applied to LPD-HCG and SPD-CDS, while incomplete CDS is applied to LPD-LCG and SPD-LOF.

Initially, LPD is reset by shutter operation and photoelectrons are generated in LPD during an integration time of 11 ms. After the integration time, RG and DRG turn off and the reset level is sampled to FD1. After that, when LTG is turned on, the electrons are transferred to FD1 and a signal level is sampled, so that complete CDS operation is done for LPD-HCG. More photoelectrons can be stored in the additional capacitance of FD2 by turning DRG on. The LPD-LCG with incomplete CDS readout starts after the LPD-HCG by sampling a signal level. To apply CDS to both HCG and LCG signals in the LPD, additional sampling capacitors and comparator circuits are required to store the LCG reset voltage.[4] Without a spatial cost, we adopt a single readout circuit for complete CDS of HCG and incomplete CDS of LCG. Side effects from the incomplete CDS such as a power supply reject ratio (PSRR) will be mitigated by PSRR compensation circuit techniques. Because the reset readout is performed after the signal readout during incomplete CDS operation, the power supply noise has no correlation between the reset and signal readouts. Thus, the incomplete CDS readout has a lower PSRR than complete CDS. To improve the power-supply noise immunity, internal voltage regulators are implemented and a PSRR compensation circuit is used as shown in Fig. 2(c). The improved PSRR performance is shown in Fig. 2(d).

After the LPD readouts, FD3, FD2, and FD1 are successively connected together by turning on SW and DRG, and the voltage level of FD1 becomes the reset level of SPD-CDS. After STG is turned on, photoelectrons from SPD are transferred and sampled to FD1, so that the complete CDS is done for SPD-CDS. Continuously, the signal level of the overflow photoelectrons generated at high illuminance are firstly read out as they have already accumulated in the in-pixel storage capacitor. After DRG is turned off and SW and RG are turned on, the in-pixel capacitor is discharged to the reset level. The reset level is sampled at FD1 by turning DRG on again. Consequently, this operation becomes the incomplete CDS of the SPD-LOF.

Since a large number of electrons can be stored in the in-pixel capacitor, the DSW transistor enables fast discharge by shortening the discharge path of the capacitor. In Fig. 3(a), the simulation results show that the reset settling time of 1 µs is achieved by adding DSW, to support higher frame rate. The simulation result is verified by the measurement results as shown in Fig. 3(b). The reset settling has been measured; the average output code of SPD-LOF is set to 2000 LSB, and if reset sampling is incomplete, the output code will be less than

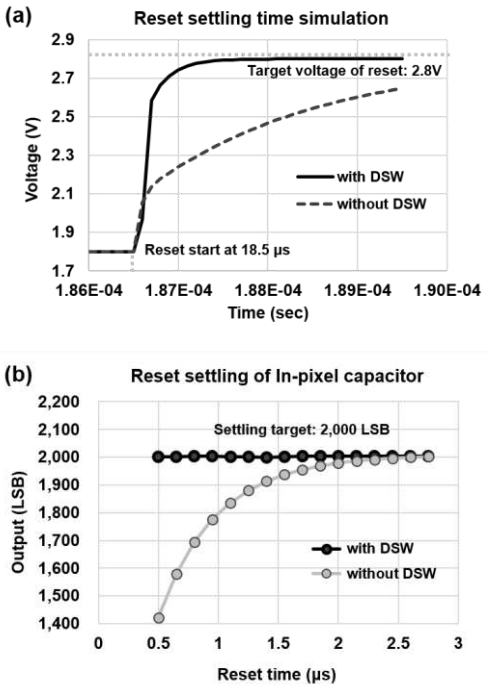

Figure 3. In-pixel capacitor reset settling comparison: (a) simulation results of reset settling at FD3 in SPD and (b) the measured results of SPD-LOF outputs with and without DSW.

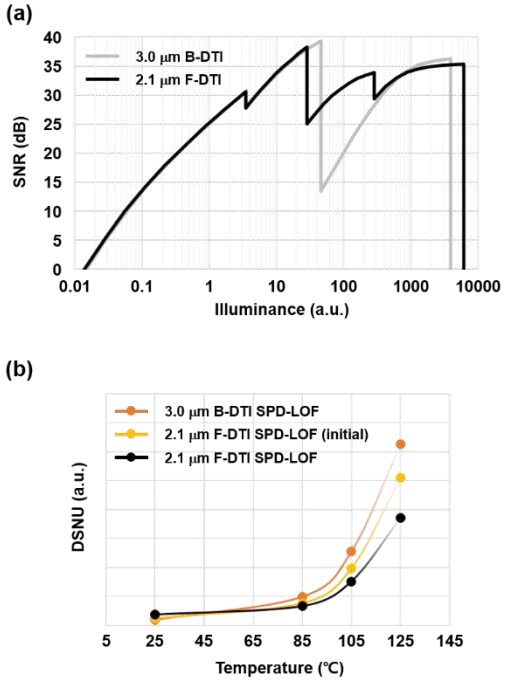

Figure 4. (a) SNR curve (at Tj 105 °C) estimated by the measured parameters during 11 ms integration time of both LPD and SPD, and (b) DSNU of SPD-LOF. The initial indicates before surface curing.

2000 LSB. The result confirms that we have achieved the settling time of less than 1 µs with DSW.

III. Result and Discussion

A. HDR charateristics at high temperature

Based on DR defined as the ratio between the exposure level at 0-dB (SNR1) and the saturation exposure level, dark random noise (RN) and dark signal non-uniformity (DSNU) are expected to be major degradation sources of DR and SNR at high temperature. To reduce RN, the width and length of the SF were optimized and high CG of 185 µV/e- was achieved by reducing the FD capacitance of the LPD. As a result, the input-referred RN of 0.83 e- was measured. At Tj 85 °C, a single-exposure DR of 120 dB was obtained by the aid of the in-pixel storage capacitor with four-readout scheme.

In Fig. 4 (a), the estimated SNR curve of the 2.1 µm F-DTI pixel is compared with that of a 3.0 µm B-DTI pixel at Tj 105 °C. The example of a 3.0 µm B-DTI pixel operates with three-readout scheme; LPD-HCG, LPD-LCG, and SPD-LOF. A large SNR drop has been found during the transition to SPD-LOF for the 3.0 µm B-DTI pixel. The DSNU of SPD-LOF dominantly degrades the SNR level with only three-readout; this can be improved by adding the SPD-CDS mode in the 2.1 µm F-DTI pixel. We maximize the FWC of SPD up to 10,000 e- to further improve the SNR during the transitions from LPD to SPD. Nevertheless, the SNR is still deteriorated by DSNU in SPD-LOF at high temperature.

Since the main source of the fixed pattern noise is the dark current generation in FD3. We found that the DSNU of the 3.0 µm B-DTI pixel is greater than that of the initial version of the 2.1 µm F-DTI pixel due to the larger FD leakage. The reduction of DSNU is contributed to the surface curing process at the initial 2.1 µm F-DTI pixel. As the temperature increases, the DSNU of SPD-LOF shows exponential behavior as shown in Fig. 4(b). By applying additional defect curing process, only for the F-DTI process, the DSNU of the 2.1 µm F-DTI pixel exhibits the extra reduction. With the merits of the F-DTI, the increase in SPD FWC and the decrease in DSNU enable to improve the SNR during the LOFIC operation. We finally achieve the minimum SNR more than 25 dB at high temperature.

B. Sensor characteristics

The 2.1 µm F-DTI pixel is fabricated and the sensor performance is summarized in Table 1. The FWC of SPD reaches 10,000 e- for SNR improvement and the high density storage capacitor is employed to achieve a single exposure DR of 120 dB at high temperature.

Table 1. Chip characteristics.

Characteristics	2.1 µm F-DTI
Process	Pixel 65 nm / Logic 28 nm, stacked BSI
Power supply	2.8 V / 1.8 V / 1.05 V
Pixel array (H x V)	3840 x 2160
Max frame rate	36 fps @ 12 bit
FWC (LPD, SPD, in-pixel capacitor)	10 ke-, 10 ke-, 210 ke-
Sensitivity	32000 e-/lux.sec (RCCB)
Sensitivity ratio	10
Conversion gain (HCG, LOFIC)	185 µV/e-, 4.2 µV/e-
Read noise (HGC) @ 85°C	0.83 e-
Single exposure DR @ 85°C	120 dB
Transition SNR @ 105°C	25 dB
Color filter array	RCCB (RGGB, RCCG, RYYCy support)

Figure 5. Chip micrograph.

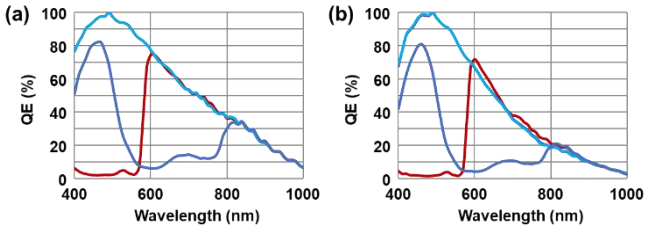

Figure 6. Relative quantum efficiency (QE) of (a) LPD and (b) SPD of RCCB color filter array.

Along with the very competitive HDR characteristics, our 2.1 µm F-DTI pixel supports various color filter arrays; RCCB, RCCG, RGGB, and RYYCy, and the relative QE of RCCB is shown in Fig. 7. Finally, the representative HDR features compared with the previous works are summarized in Table 2.

Table 2. HDR performance comparison.

HDR characteristics	This work (F-DTI)	IEDM 2022 [6]	IEDM 2021 [3]	ISSCC 2020 [4]	IISW 2019 [2]
Pixel pitch	2.1 µm	2.1 µm	2.1 µm	3.0 µm	3.0 µm
HDR Technology	Sub-pixel, LOFIC	Sub-pixel, LOFIC	LOFIC	Sub-pixel, LOFIC	LOFIC
FWC (LPD / LOFIC)	10 ke- 210 ke-	10 ke- 1.8 Me-	10 ke- 600 ke-	12.8 ke- 166 ke-	20 ke- 175 ke-
Single exposure DR (based on total noises)	120 dB	140 dB	110 dB	121 dB	96 dB
Min. SNR @transition	25 dB @ 105°C	23 dB @ 105°C	25 dB @ 125°C	25 dB @ 100°C	25 dB @ 100°C

IV. Conclusion

We have developed a 2.1 µm F-DTI pixel with LED flicker mitigation for automotive applications. A single exposure DR of 120 dB is achieved by employing sub-pixel architecture capped with an in-pixel storage capacitor. The capacitor can enormously extend charge-accumulating capability of the pixel supported by DSW transistor. Minimum SNR stays over 25 dB by increasing FWC of SPD and reducing DSNU of SPD-LOF with the merits of F-DTI process and four-readout scheme.

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110dB High Dynamic Range Continuous Non-Uniform TTS and Linear ADC Scheme Using A 4.6 µm Stacked Digital Pixel Sensor

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1. Introduction

Demands for the global shutter (GS) image sensor with low power consumption, small chip size, and wide dynamic range (DR) are increasing for always-on, buttery-powered wearable AR/VR devices. The digital pixel sensor (DPS) is one of the solutions to realize such devices [1][2], and the authors have reported two DPS's. One is a 512 × 512 pixel sensor with a 4.6µm pixel [3][4], and the other is a 1024 × 832 pixel sensor with a 4.0µm pixel [5].

The 4.6µm pixel DPS operates in a triple quantization (3Q) scheme to enhance DR and achieves 127 dB DR with a power consumption of 5.75 mW at 30 fps. In the 3Q operation, a time-to-saturation (TTS) quantization is performed during the exposure time, followed by the two linear quantizations using single-slope analog-to-digital conversion (ADC). The first quantization has a high conversion gain (CG) signal, called "PD ADC", and the other has a low CG signal, called "FD ADC". Its initial version and the improved version were reported in [3][4] and [6], respectively.

In addition to the 3Q scheme offering ultra-high DR capability with a signal-to-noise ratio (SNR) drop at the mode-junction points, the stacked DPS in [3][4][6] can operate in other quantization schemes utilizing its in-pixel time-to-digital and ADC functions by modifying pixel signals and reference voltages.

One of such schemes is the dual quantization (2Q) scheme that combines a time-stamp (TS) quantization and a single-gain linear ADC modes [5]. Hereinafter, we call it "TS-Linear" scheme. While the maximum DR is reduced to 107dB, this scheme has an advantage of reducing SNR drop at the mode-junction point. It is because this scheme does not involve the low CG ADC mode that does not allow correlated double sampling (CDS) operation. It also has the advantage of possible simplification of the pixel circuit due to the single-gain ADC mode. On the other hand, TS-Linear scheme may suffer SNR drop degradation due to the PD FWC variation.

In this paper, we apply another 2Q scheme that combines TTS quantization and a single-gain linear ADC mode that we call "TTS-Linear" scheme [7]. In this scheme, PD FWC variation does not affect the SNR drop at the junction point. Pixel can be simplified the most among three schemes presented so far, which suggests pixel-size and power-consumption reductions are possible. To overcome its disadvantage of the lowest DR (103dB) among the three schemes, we demonstrated a DR-enhancement capability up to 110dB by introducing a nonuniform TTS operation, whose details are described in the following section.

2. Sensor Operations

We used the stacked DPS in [6] to compare the three quantization schemes in the previous section. It was fabricated by a 45 nm CIS and 65 nm logic stacked sensor process. These two layers are connected by pixel-level interconnects using the Cu-to-Cu hybrid bonding (HB) technology [8]. It has a 512 × 512 pixel array with a 4.6µm pixel pitch and is implemented in a 4mm ×

4mm die.

Table 1 compares equivalent pixel circuit diagrams, signal timing diagrams, and performance score boards of the three quantization schemes.

3Q pixel in (a) is based on a dual conversion-gain (DCG) CIS pixel circuit with anti-blooming (AB) gate and in-pixel bias-current source (Vbn) in the top layer. The ADC circuit on the bottom layer includes the coupling capacitor (Cc) and a voltage comparator with the reset switch (Comp_RST) for analog CDS operation. The quantization result is stored in the 10-bit SRAM that is driven by ADC codes distributed to the whole pixel array. The state latch and control logic circuit manage the automatic signal selection of the 3Q signals. The comparator is biased in the sub-threshold region for low power operation.

TS-Linear pixel (b) does not require DCG. The signal-selection logic can be simplified, too.

TTS-Linear pixel (c) does not need the selection logic and Comp_CHK signal.

Timing diagrams of 3Q and TS-Linear schemes in Table 1 are from the previous reports [5] [6].

In 3Q scheme, low CG is chosen by connecting FD node to the storage capacitor, C_S, in TTS and FD ADC modes. PD ADC is performed with high CG. Auto-zeroing operation is done before every quantization mode by pulsing the comparator reset signal, Comp_RST. Signal charge transfer is done by TG pulse just before PD ADC mode.

In TS-Linear scheme, the comparator reference signal, VRAMP, ramps up during the integration period for TS operation. Auto-zeroing operation is done before both quantization modes by pulsing the comparator reset signal, Comp_RST

In both 3Q and TS-Linear schemes, the TG pulse potential is optimized for a complete PD charge transfer.

A timing diagram for the newly proposed TTS-Linear operation is also shown in Table 1 (c). First, PD is reset using AB gate. Then, integration starts when AB gate turns off. Before cutting RST and Comp_RST that have performed auto-zeroing operation, TG bias is raised to a particular level between PD Vpin and the FD reset level. Then, photo current starts pulling down FD potential. When FD potential goes low enough for the comparator input to go below the reference voltage, VRAMP, the comparator flips to latch the quantization code on the SRAM. The integration (TTS operation) is ended when AB is turned on to reset PD again. At the same time, linear ADC is done to digitize low-light signal which TTS has not detected. Digital counts 0-511 (9b) are reserved for the linear ADC and 512 - 767 (8b) for the TTS operation.

3. Non-uniform TTS

The proposed 2Q TTS-Linear operation achieves 103 dB DR. To recover its lower DR than those with the previous operation modes, non-uniform TTS scheme is introduced where non-linear ramp operation was used to reduce the conversion time [9][10].

Fig. 1 shows a conceptual timing diagram of the non-uniform TTS scheme together with that of the conventional uniform TTS scheme. Seven different TTS clock widths are assigned within the 8bit TTS period. The shortest clock width is assigned for the highest light portion, followed by longer-width clocks toward the end of the TTS period. The shorter clock width can detect higher light levels than with the longer clock widths in the uniform TTS scheme. Thus, this non-uniform TTS scheme can extend the DR. Also, it can suppress the oscillation in the SNR plot that is seen in the linearized photo-response curve with the previous operations [4].

4. Characterization

A linearized pixel photo response curve (PRC) and a SNR curve with external FPN correction, and a magnified photo-response curve in the low-light region are shown in Fig. 2 (a) and (b), respectively. Good low light linearity and SNR of 32 dB at the junction point

between the TTS and the linear quantization have been obtained. Also, DR of 110dB has been achieved, thanks to the nonuniform TTS with the oscillation in the SNR at high light portions suppressed.

Table. 2 summarizes measured performances of the three quantization schemes. The proposed 2Q TTS-linear scheme features the best SNR characteristic and potentially smaller pixel size and lower power consumption among the three schemes. On the other hand, the previously reported 3Q scheme provides the best DR and low-light noise performance, and 2Q TS-Linear scheme offers a balanced performance.

5. Summary

This paper presents a new non-uniform TTS-Linear ADC operation scheme and its characteristics using the 4.6µm 512 × 512 pixel DPS. It has been confirmed that the TTS-Linear ADC operation generates no large SNR drop at the mode junction point and achieves single exposure 110dB DR. Also, it is expected that the pixel size and power consumption become smaller with this operation, due to its simpler circuit configuration.

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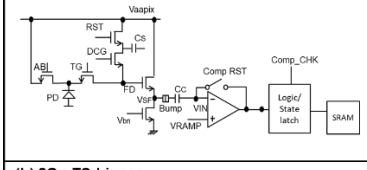
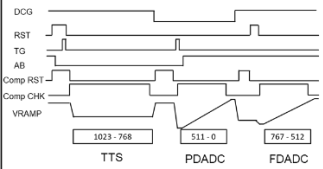
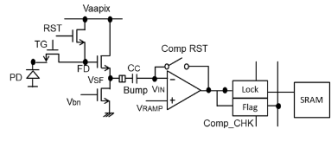
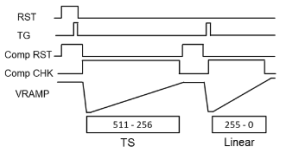
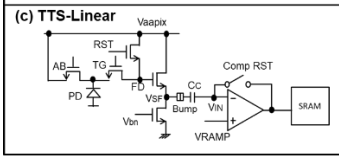
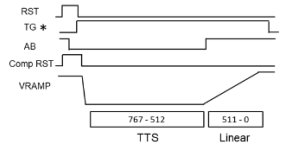
Table 1. Equivalent circuit and timing diagram of 3Q, 2Q and TTS-Linear scheme.

Equivalent circuit	Timing diagram	Dynamic range	Dark Noise	SNR drop	Pixel size	Power consumption
(a) 3Q : TTS-PDADC-FDADC 		Best	Best	Worse	Better	Better
(b) 2Q : TS-Linear 		Better	** Best	Better	Better	Better
(c) TTS-Linear 		Better	Better	Best	Best	Best

* TG is moderately ON to allow charges to flow from PD to FD. ** Although dark noise of 2Q is worse than other operations in Table 2, dark noise of the 2Q operation should be the same as that of the 3Q mode in principle.

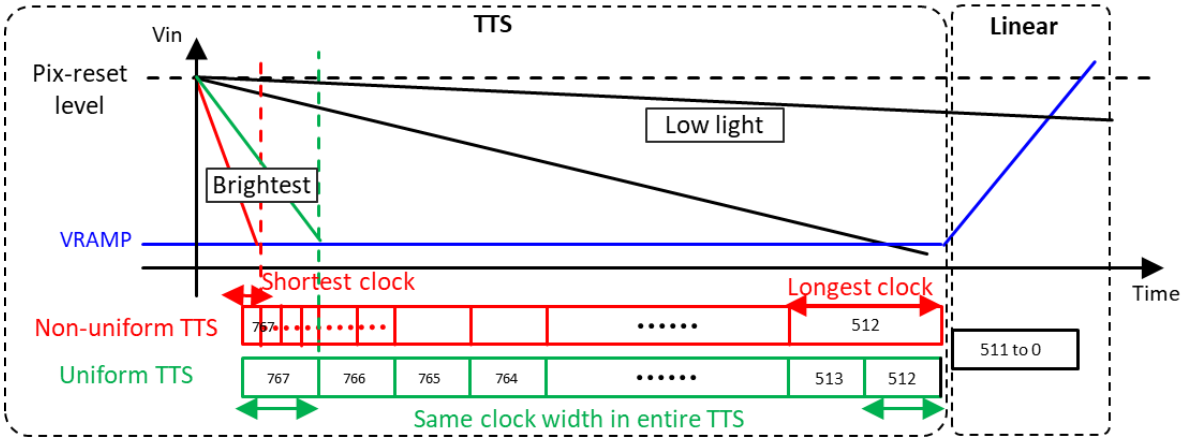


Fig 1. Conceptual timing diagram of non-uniform TTS and uniform TTS. Non-uniform TTS enhances the resolution in bright light region than uniform TTS and suppresses SNR oscillation there [4].

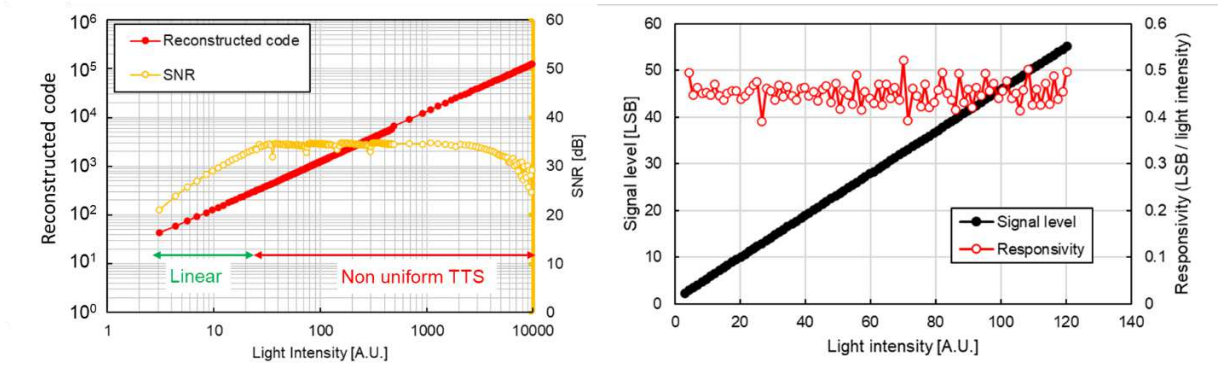


Fig 2. Linearized photo-response curve and SNR plot using non-uniform TTS (Left)

Magnified photo-response curve in low light region showing a good linearity (Right)

Table 2. Summary of 3 quantization schems (integration time = 1ms)

Specification	This work	Ikeno IISW 2023 [6]	Mori IEEE 2022 [5]
Pixel size	4.6 um	4.6 um	4.0 um
Pixel array	512 x 512	512 x 512	1024 x 832
In pixel Memory bit#	10 bit	10 bit	9 bit
ADC resolution	8bit(TTS) + 9bit(Linear)	8bit(TTS) + 9bit(PD) +8bit(FD)	8bit(TS) + 8bit(Linear)
Dynamic Range	110 dB (Non-uniform TTS)	127 dB	107 dB
Temporal noise (dark)	5.6 e-	4.0 e-	8.3 e-
FPN rms (dark)	35 e-	27 e-	64 e-
Conversion gain	170uV /e-	170uV /e- (HCG), 12.5uV/ e- (LCG)	150uV /e-
SNR at junction	TTS to Linear : 32dB	PD to FD : 27dB, FD to TTS : 35dB	TS to Linear : 23dB
Power	5.8 mW (30 fps)	5.8 mW (30 fps)	NA

FPN : without external FPN correction

A 5MPixel Image Sensor with a 3.45µm Dual Storage Global Shutter Back-Side Illuminated Pixel with 90dB DR

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OMNIVISION

Abstract - **While Rolling Shutter sensors with High Dynamic Range (HDR) performance have been commonplace for many years, Global Shutter (GS) sensors have been lagging behind in demonstrating HDR capabilities. The combination with small pixel pitches and back-side illumination (BSI) has been particularly rare. This paper presents a back-side illuminated, 3.45µm HDR GS pixel making use of a dual storage Voltage Domain Global Shutter (VDGS) pixel, achieving up to 90dB Dynamic Range.**

INTRODUCTION

In recent years, the industry has seen several examples of image sensors supporting Dual Conversion Gain (DCG), Overflow or Multiple-Exposure HDR techniques [1-8]. Besides implementations for scientific and niche applications, BSI global shutter pixels have been introduced mostly recently [4, 9, 10, 11]. Amongst those, [11] stands out as a solution that combines HDR and BSI in a small pixel pitch.

This work introduces a 5 Megapixel Global Shutter sensor with 3.45µm dual storage pixels. The back-side illuminated, VDGS pixel uses a Stacked Pixel Level Connection (SPLC) and full Deep Trench Isolation (DTI). The sensor supports a single capture (linear) and two dual capture (HDR) modes: Dual Conversion Gain (DCG) and Dual Exposure (DEXP).

Taking advantage of these recent technology advances illustrated in Figure 1, the performance demonstrated in [11] has been substantially improved. Noise levels lower than 2e- can be achieved at high gain.

In DCG mode, a 2.7e- noise level can be combined with a full well capacity of >20000 electrons, resulting in a Dynamic Range (DR) of 77dB. In DEXP mode, up to 90dB DR has been demonstrated.

With Nyxel technology, a QE of >40% at 940nm, and a peak green QE of 84% was achieved. Thanks to the SPLC and storage on High Density MiM capacitor in a separate wafer, the pixel has a Global Shutter Efficiency (GSE) well below -100dB.

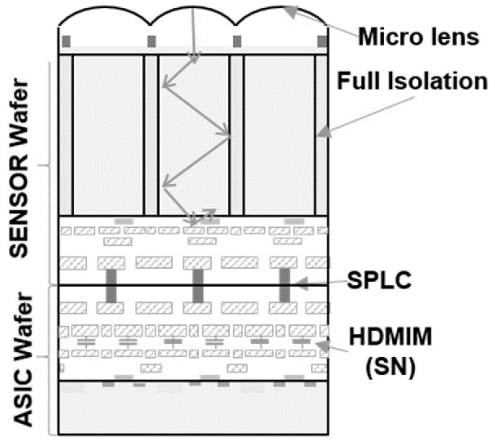

Figure 1 Process Configuration of the VDGS Pixel

Aside from the highly competitive performance at 3.45µm, the technology offers great promise to further shrink HDR global shutter pixels in the future.

The 5 Megapixel sensor operates at up to 120fps in linear mode (10-bit or 12-bit output) and 60fps in the dual capture modes (12-bit, 14-bit or 16-bit output). The on-chip HDR recombined signal is transmitted off the sensor by means of a 4-lane MIPI D-PHY or a 4- or 8-lane sub-LVDS interface. Furthermore the sensor supports various trigger modes (in linear and HDR modes) and a background subtraction mode.

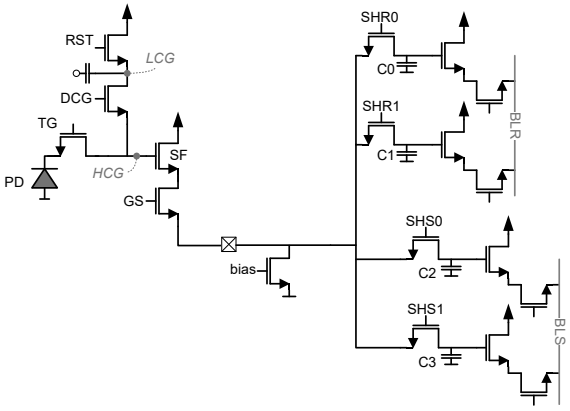

Figure 2: Pixel Schematic of the dual storage VDGS pixel

(1) previously with OMNIVISION

PIXEL CIRCUIT

The dual storage pixel architecture is shown in Figure 2. It builds on the differential pixel topology introduced in [9] but adds a second set of capacitors which may be utilized to store the dual capture signals (DCG or DEXP) in the HDR modes.

DUAL CONVERSION GAIN OPERATION

The operation of the DCG is similar to [12, 13] but now being applied to a Global Shutter Sensor with the timing sequence shown in Figure 3. The CDS (SHR, SHS) voltages for both HCG and LCG signals are stored on the two sets of capacitors. Using this technique, the dynamic range, 64dB in linear mode, is extended to 77dB.

This dynamic range is achieved by making use of an analog gain 7x on the HCG channel. The analog gain is chosen to optimize the noise while keeping the SNR at the transition between the gain channels (SNR_tran) above 26 dB as seen from the measurement results in Figure 4.

The main contributors to the SNR drop for this operating mode are the higher read-noise and fixed-pattern-noise in the LCG channel due to leakage variation on the storage node from pixel to pixel.

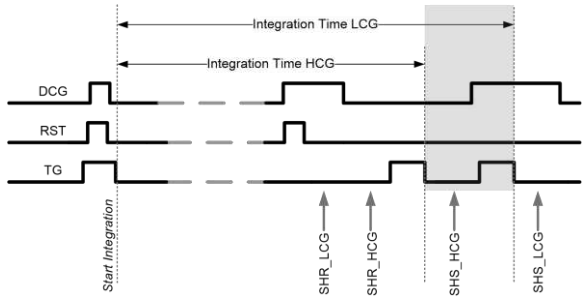

Figure 3 DCG Timing Diagram

From the timing diagram, it is clear that the HCG and LCG signals do not have the exact same exposure time due to the second transfer operation. As a result the gain ratio between these two captures varies with the integration time.

This effect will be particularly pronounced for shorter integration times. To accommodate this, the sensor adjusts the gain ratio in the 2D HDR Combine ISP (Figure 5) adaptively as the integration time changes. This ensured that the combined HDR signal remains linear all the way down to the minimum exposure time.

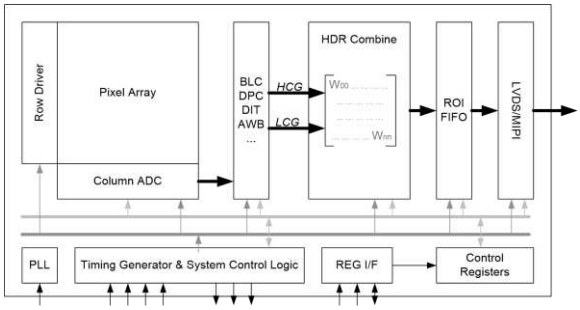

Figure 5: Top Level Block Diagram highlighting the HDR combine function

DUAL EXPOSURE OPERATION

Alternatively, the sensor supports a dual exposure HDR scheme [6, 11]. The long exposure is captured on the HCG channel while the short exposure is captured on the LCG channel.

With the HCG channel at an analog gain of 1x and while applying an exposure ratio of 7x, a dynamic range of 90dB can be achieved. A higher dynamic range may be achieved by applying a larger exposure ratio or higher gain for HCG, but in that case the SNR (Measurement results shown in Figure 6) at the transition point would drop below acceptable levels.

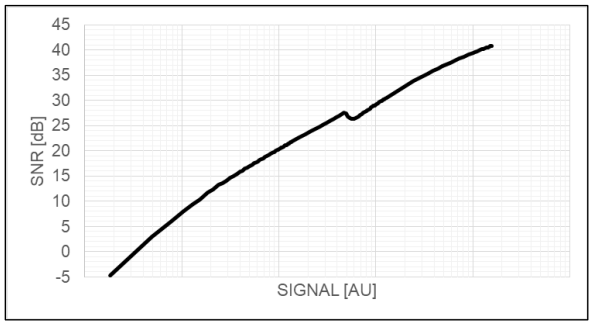

Figure 4: Dual Conversion Gain SNR

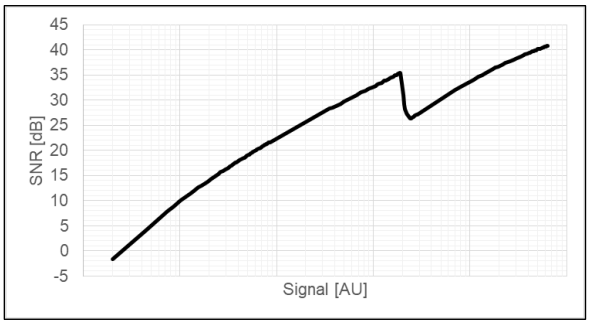

Figure 6: Dual Exposure SNR

FUTURE WORK: VDGS EXPOSURE TIME CHALLENGES

Taking a closer look at the timing diagram for the linear mode (Figure 7), it is clear that the finite time it takes to sample the Reset and Signal values, has an impact on the exposure time control of the sensor as was already clear from the HCG/LCG exposure time difference raised earlier.

In a linear mode of operation with a single readout, the time it takes to reset the photodiode and the floating diffusion and the time it takes to sample the reset value, puts a lower limit on the integration time that can be supported. Due to the fact that these are global operations, they add in additional requirements for the on-chip charge pumps, the row drivers and the power supply network. The pixel timing needs to be carefully tuned to minimize the minimum exposure time achievable without introducing any artefacts.

A relatively straightforward solution to this problem may be to introduce an additional "photodiode reset gate" as is common for charge domain global shutter pixels e.g. [6].

However, while certainly reasonable in a 3.45µm pitch, this additional gate would eventually limit the scaling potential to pixel sizes approaching 1µm. Future innovations are expected to be necessary to reduce the sampling time as resolutions grow larger, pixel sizes smaller and capacitor density increases [14].

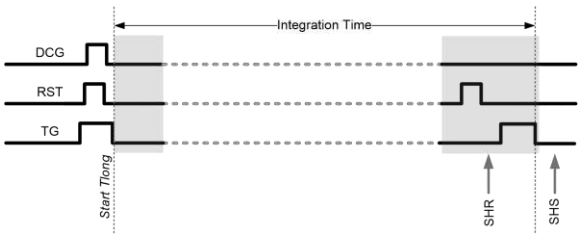

Figure 7: Single Capture (linear) Timing Diagram

CONCLUSION

This paper presented silicon results of a 5 Megapixel Global Shutter imager supporting two HDR modes. As shown in Table 1, this product advances the state-of-the-art in small pixel Global Shutter HDR performance combining low light performance with high dynamic range, while maintaining a high SNR at the transition point. An image taken with the sensor is shown in Figure 8.

Figure 8: Image Captured with the sensor

Table 1: Performance Summary & Comparison

Parameter	**This Work (@ 70C)**	**[11]**
Resolution	5 Megapixel	1 Megapixel
Pixel Pitch	3.45µm	3.75µm
GS Architecture	Voltage Domain Global Shutter	Voltage Domain Global Shutter
Full-Well Charge	20.000e-	8100
Temporal Noise Linear	2e- at high gain	8.5e-
Temporal Noise HDR	2.7e- in DCG 4.5e- in DEXP	16.8e-
Fixed Pattern Noise	1.4e-	N/A
HDR Single Exposure	77dB	59dB
HDR Dual Exposure	90dB	102dB
SNR_tran	>26dB	N/A
QE – 940nm	41%	N/A
QE - Green	84%	N/A
GSE	< - 100dB	< - 80dB
Frame Rate	60fps	50fps
Process	BSI 45nm, Pixel Level Stacked	BSI 65nm

The authors like to thank Dietrich Elst, Ivana Sremački, Thomas Cools and Mourad Daoudi for their support in characterization and validation.

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A High Dynamic Range APS-C Sized 8K 120-fps Stacked CMOS Image Sensor

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Introduction

In this paper an APS-C size 43 Mpixel rolling shutter image sensor is presented with multiple techniques of increasing the dynamic range of the sensor. The sensor is targeted for use in cinematographic applications requiring high dynamic range image sensing.

Sensor architecture

The stacked sensor architecture, depicted in Figure 1, consists of a top-side die containing the pixel array with a resolution of 8448 x 5376 pixels, as well as the bonding pads, and a bottom die containing an 8 x 8 array of identical readout circuit blocks (core cells). These core cells consist mainly of column parallel analog-to-digital converters, SRAM memory and pixel control signal drivers. The pixel array is connected to the bottom wafer circuits using Cu-Cu hybrid bonding.

Figure 2 illustrates the data path between pixel and sensor output. Per pixel column, 8 column buses connect via the hybrid bonding to the analog to digital converters in the 8 rows of core cells on the bottom wafer. The 8 selected pixels rows are physically adjacent on the top wafer, which minimizes rolling shutter artefacts. In each row of core cells on the bottom wafer, each column uses a 14-bit ramp ADC to convert the signal on the column bus to a digital value. The digitized outputs are fed to a logic adder which is also connected to part of the SRAM frame buffer. The complete frame buffer memory is distributed across all core cells within the chip. To transmit the data to the sensor output, the adder output is multiplexed over a horizontal digital bus to the data formatting block which is located outside the core cell area. This block re-organizes the data, applies black level correction and formats the data to be sent out over 16 high-speed data output channels.

High dynamic range modes

The 3.2 µm pixel contains a dual conversion gain (DCG) readout architecture [1] providing low-noise readout in dark image regions while also supporting a high full well charge readout. In the dual conversion gain readout mode, a frame rate of up to 60 frames per second can be achieved for the 8K video format. In this mode, the presented sensor achieves a full well charge of 26.5 ke- and a total combined dynamic range of 76.4 dB. The sensor also allows reading out only the low or high gain path in a single conversion gain (SCG) mode at up to 120 frames per second.

To further increase the dynamic range of the sensor, the SRAM frame buffer in the core cells allows for an intermediate pixel readout and storage without interrupting the exposure. Figure 3 shows the conceptual timing of the multiple exposure rolling shutter mechanism, which increases the full well charge of the sensor beyond the limit of the photodiode full well charge. The total exposure time (Texp) is in this case divided in four equal sub-exposure times (Texp0…3). When the first exposure (Texp0) is finished, the pixel is read out in either single or dual conversion gain mode and converted

to a digital value. The result is stored in the frame buffer. During such intermediate readout, the pixel charges are cleared from the pixel's photodiode. After the second exposure (Texp1), the pixel signal is digitized again and the resulting value is added to the value from Texp0. The result of this operation is stored back in the SRAM frame buffer. The same operation is repeated for the third exposure time (Texp2). After completing the fourth sub-exposure, the digitized value is added to the previously stored data, but is now sent directly to the data formatting block and the output interface.

The response measurement and Photon Transfer Curve (PTC) executed with 1, 2 and 4 sub-exposures are plotted in Figure 4. Because of the DCG readout, a high and low gain response and PTC is plotted for each case. The response measurement shows that for the three sub-exposure cases the conversion gains are equal. However, the saturation level is linearly correlated to the number of sub-exposures. The PTC plot shows that also the peak variance, and thus also the full well charge, is linearly correlated to the number of sub-exposures. It increases from 26.5 ke- to 54.3 ke- and 108.6 ke- for the 2-exposure and 4-exposure modes respectively. The dynamic range increases similarly, to 80.1 dB and 83.5 dB respectively. Table 1 summarizes the basic performance parameters of these sensor modes.

It is possible to increase the dynamic range even further by applying non-equal sub-exposure times as shown in figure 5. After each sub-exposure, the converted signal level is digitally clipped to a programmable level before it is added to the previously stored sub-exposure data and written back to the frame buffer. This operation results in a multiple slope response with up to a maximum of 4 slopes. The slope ratios of the multiple slope response are a function of the sub-exposure time ratios, similar to the known multiple slope response when applied in the analog domain [2]. The knee points themselves are accurately controlled by the sub-exposure times and the saturation clipping of the A/D converter. Because in this sensor the clipping occurs in the digital domain, accurate knee point levels can be set and no pixel-to-pixel variation is present. This makes off-chip linearization of such a multiple slope response much more convenient compared to analog domain multiple slope where typically there is a significant pixel-to-pixel variation on the knee point. Measured results of the response curve and linearized response are shown in Figure 6, using 4 sub-exposures with a ratio of 8x, 4x, 2x and 1x for exposures 0, 1, 2 and 3 respectively.

Besides the 8K video format, the sensor supports readout of a 4K binned image at frame rates up to 120 frames per second with a full well charge of >100 ke- and total dynamic range of >81 dB; or 60 frames per second with a full well charge and dynamic range of >200 ke- and >84 dB using the multiple exposure rolling shutter mechanism with 2 sub-exposures.

High-speed data readout

With the use of a custom high-speed 5.25 Gbps interface link, these frame rates can be achieved using only up to 16 channels. The sensor was fabricated using a 65 nm stacked CMOS image sensor process. Figure 6 shows a picture of the fabricated sensor in a 363-pins ceramic LGA package.

References

[1] Wang, X., Wolfs, B., Meynants, G., & Bogaerts, J. (2011, June). An 89dB dynamic range CMOS image sensor with dual transfer gate pixel. In Proc. Int. Image Sensor Workshop (pp. 248-251).

[2] Decker, S., McGrath, D., Brehmer, K., & Sodini, C. G. (1998). A 256/spl times/256 CMOS imaging array with wide dynamic range pixels and column-parallel digital output. IEEE Journal of solid-state circuits, 33(12), 2081-2091.

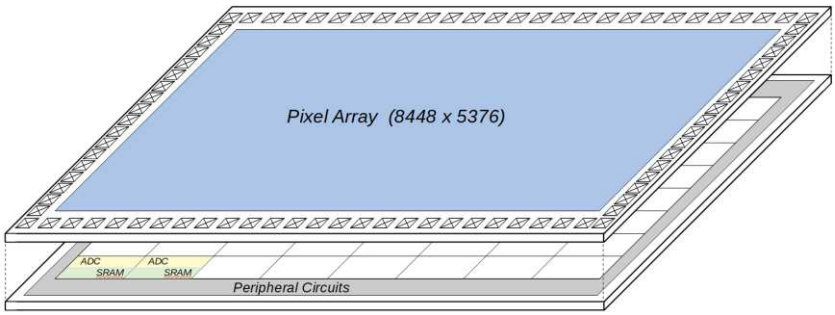

Figure 1 – Stacked sensor architecture.

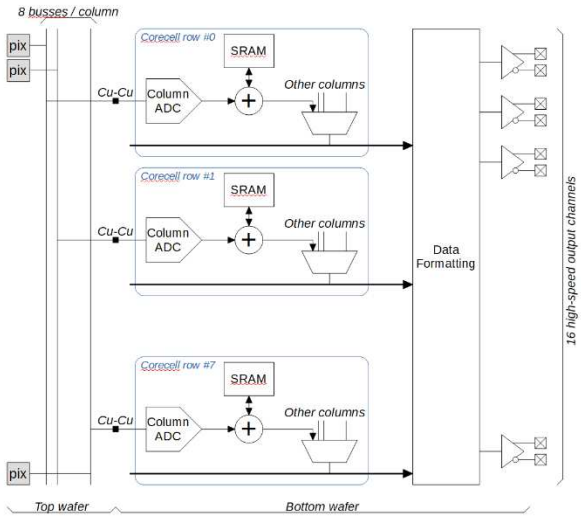

Figure 4 – Data readout path from pixel to sensor output.

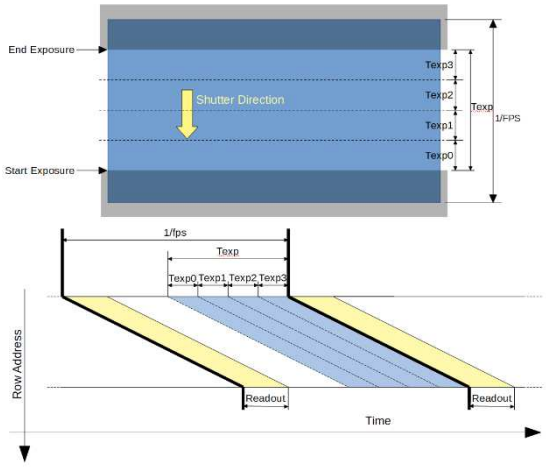

Figure 3 - Multiple exposure rolling shutter mechanism timing (bottom) and position of pointers on the array (top).

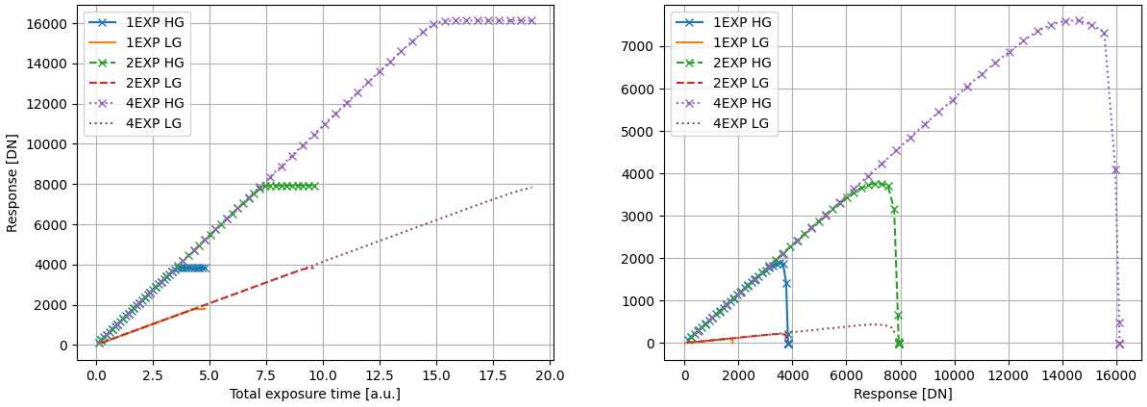

Figure 2 – Response curve (left) and Photon Transfer Curve (right) measurement results of high gain (HG) and low gain (LG) readout path in DCG readout mode, using 1, 2 and 4 sub-exposures (nEXP = 1, 2 and 4).

Table 1 – Summary of sensor performance characteristics in DCG readout mode.

Process	65nm CIS stacked		
Resolution	8448 (H) x 5376 (V)		
Pixel pitch	3.2 µm		
# sub-exposures summed	1	2	4
Full well charge (LG)	26.5 ke-	54.3 ke-	108.6 ke-
Dark temporal noise (HG)	4.0 e-	5.3 e-	7.3 e-
Dynamic range	76.4 dB	80.1 dB	83.5 dB
Maximal frame rate	60 fps (*)	60 fps	30 fps

(*) in high dynamic range dual gain readout mode due to output data rate limitation. A maximal frame rate of 120 frames per second can be achieved when reading only the low-gain or high-gain pixel conversion path.

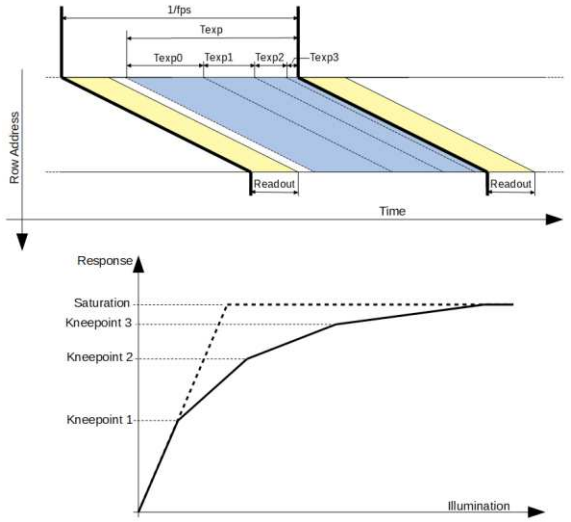

Figure 5 – Timing illustration for the multiple slope HDR expansion (top) and knee points in the response curve (bottom)

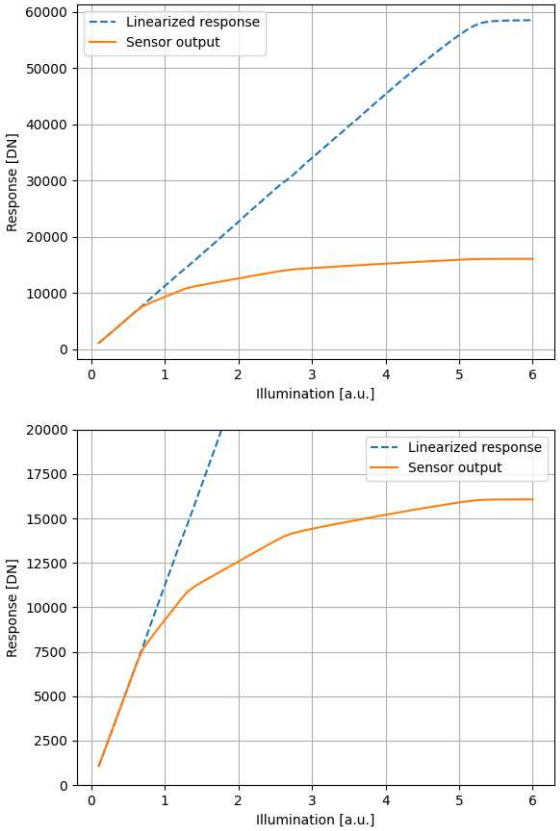

Figure 6 – Measurement results of 4-exposure multiple slope HDR expansion, showing both sensor output and the linearized response (top) and zoomed in on the sensor output response curve (bottom) to better show the knee points

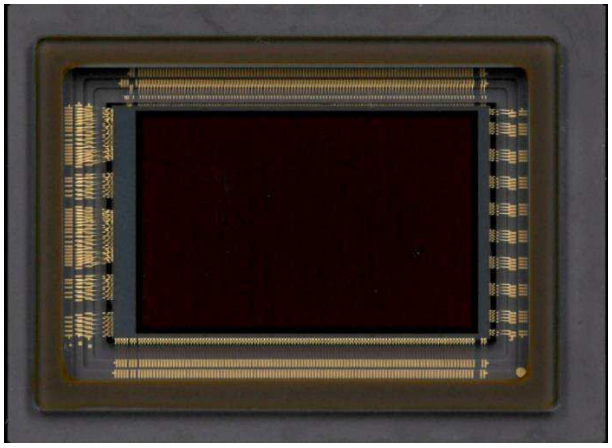

Figure 7 – Fabricated and packaged sensor.