Automotive 2.1 μm Full-Depth Deep Trench Isolation CMOS Image Sensor with a Single-Exposure Dynamic-Range of 120 dB

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***Abstract*— An automotive 2.1 μm single exposure CMOS image sensor has been developed with a full-depth deep trench isolation and an advanced current readout circuit technology. To achieve a high dynamic range, we employ a sub-pixel structure featuring a high conversion gain of a large photodiode, and lateral overflow of small photodiode connected to in-pixel storage capacitors. The expanded dynamic range could reach 120 dB at 85 °C by realizing low random noise of 0.83 e- and high overflow capacity of 210 ke-. Over 25 dB signal-to-noise ratio is achieved at the transition point by increasing the full-well capacity of the small photodiode of up to 10,000 e- and suppressing the floating diffusion leakage at 105 °C.**

Keywords—Automotive, HDR, F-DTI, sub-pixel structure.

I. INTRODUCTION

High dynamic range (HDR) is a primary requirement for automotive image sensors to capture not only both bright and dark regions in a single scene, but also the light-emitting diodes (LEDs) lighting signals of transportation environments. One way to expand the dynamic range (DR) is to use the multiple exposure method.[1] However, the sequential image capture causes motion artifacts, and the short integration time results in LED flickering. Thus, a single-exposure with the longer integration time is necessary along with HDR. The lateral overflow integration capacitor (LOFIC) technology can cover the long exposure time by storing the excess photoelectrons in a large in-pixel capacitor.[2-4] The high-capacity MOS and metal-insulator-metal capacitors are widely used, and the unit capacitance of the in-pixel capacitors is known to be around a few 10 fF/μm^2.[1]

The single photodiode (PD) with LOFIC has achieved a single-exposure DR of 110 dB,[3] whereas LOFIC combined with sub-pixel structure can expand DR up to 120 dB in a single exposure.[4] The spatial sampling with a high sensitivity ratio between a single large PD (LPD) and a single small PD (SPD) enables to expand DR. As the pixel size gradually shrinks for higher resolution, this sub-pixel architecture not only faces a critical limit where DR is no longer expanded due to the restricted pixel area for the in-pixel capacitor, but also noticeably deteriorates SNR during the signal transition between the two PDs. The high-density in-pixel capacitor approach could overcome the former restriction.[3, 6] However, such scaling makes the SNR degradation as a result of a small full-well capacity (FWC) of the PDs.

Despite the restrictions, here, we have developed a 2.1 μm CMOS image sensor incorporated with a sub-pixel structure by applying the full-depth deep trench isolation (F-DTI) technology. A 120 dB single-exposure DR is achieved at 85 °C by using a storage capacitor in a pixel. By increasing the FWC of the SPD and reducing the floating diffusion (FD) leakage current, the minimum signal-to-noise ratio (SNR) at the transition point is improved up to 25 dB at a junction temperature (T_j) of 105 °C. We believe that the integration of the F-DTI process into a pixel array accelerates reduction of the pixel pitch with the competitive HDR performance in the automotive image sensor technology.

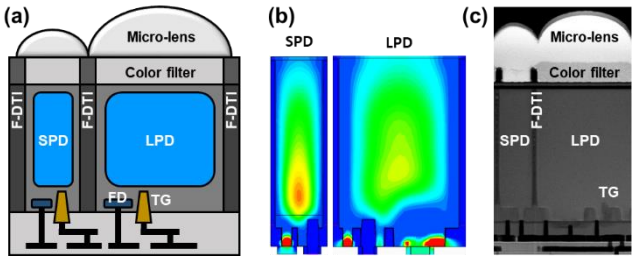

Figure 1. Cross-sectional views of (a) a 2.1 um sub-pixel structure, (b) simulated electrostatic potential profiles, and (C) a SEM image.

II. PIXEL DEISGN AND OPERATION

A. *2.1 μm F-DTI pixel*

In general, the sub-pixel structure with the high sensitivity of an LPD and the low sensitivity of an SPD is fabricated to cover a wide range of light levels from the dark to the bright environments. As the pixel size shrinks, the conventional back-side deep trench isolation (B-DTI) process is restrictive when applied to the sub-pixel structure due to the limitation of forming potential barriers between the PDs. Therefore, the larger FWC of the PDs with no blooming is not feasible; it is difficult to scale down with B-DTI pixel structure. In this work, however, F-DTI process was utilized to develop a physically isolated sub-pixel structure as shown in Fig. 1(a). The merits of the F-DTI are to prevent optical and electrical crosstalk, and to maximize the FWC of PDs without blooming.

A fully-depleted region of the F-DTI pixel can be extended to the deep-level of the silicon via high-energy n-type implantation, and the larger FWC of a SPD is demonstrated through the device simulation as shown in Fig. 1(b). On the front side of silicon surface, the transistors and FDs are separated by an additional p-well implantation, further enlarging the FWC of the buried PDs. The scanning electron microscope (SEM) image of the cross-sectional view for the

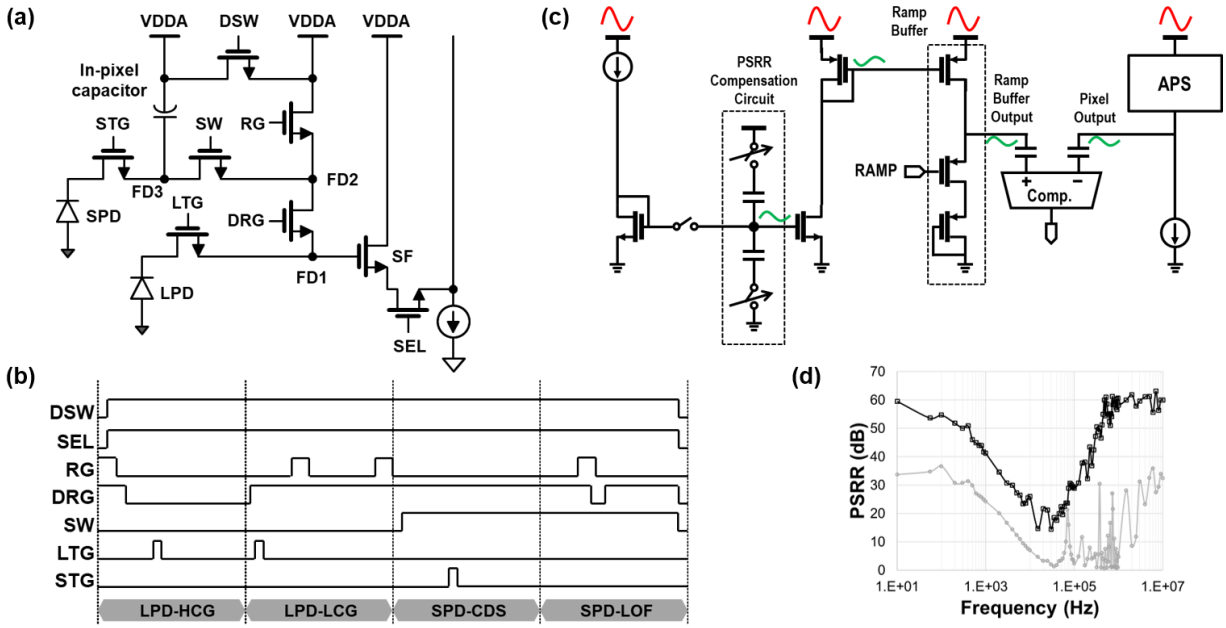

Figure 2. The proposed pixel circuit with readout timing: (a) a pixel schematic of the 2.1 μm F-DTI sub-pixel structure with in-pixel storage capacitor, (b) four readout timing diagram, (c) PSRR compensation concept diagram, and (d) the measured results before (gray) and after (black) applying PSRR compensation scheme.

2.1 μm F-DTI sub-pixel structure is shown in Fig. 1(c). With the vertical transfer gate (VTG) and the buried PDs, the FWC of SPD as high as 10,000 e- is realized in order to improve the SNR. The F-DTI pixel capped with a storage capacitor allows us to expand DR with lateral overflow operation. The capacitance of the overflow capacitor is more than 34 fF per pixel, allowing more than 210 ke- to be accumulated in a single exposure.

B. Pixel circuit and operation

Fig. 2(a) shows the pixel schematic of the 2.1 μm F-DTI pixel, consisting of two PDs, three FDs, eight transistors, and one storage capacitor. Using a DRG transistor, the LPD supports a dual conversion gain (CG) readout, and a low CG of SPD due to the capacitor can be switched by a SW transistor. When all transistors are turned on, every FD node is connected to the gate of a source follower (SF) amplifier, and then the circuit can operate in the readout mode of LOFIC signals. A DSW transistor is added to reduce the discharge time of the storage capacitor during the reset operation of the LOFIC signals. We implement a four-readout scheme: correlated double sampling (CDS) and incomplete CDS for both LPD and SPD. A simplified timing diagram is shown in Fig. 2(b). During the operation, the sequential readouts are performed with LPD-HCG (LPD with high CG readout), LPD-LCG (LPD with low CG readout), SPD-CDS (SPD with CDS readout), and SPD-LOF (SPD with LOFIC readout). CDS is applied to LPD-HCG and SPD-CDS, while incomplete CDS is applied to LPD-LCG and SPD-LOF.

Initially, LPD is reset by shutter operation and photoelectrons are generated in LPD during an integration time of 11 ms. After the integration time, RG and DRG turn off and the reset level is sampled to FD1. After that, when LTG is turned on, the electrons are transferred to FD1 and a signal level is sampled, so that complete CDS operation is done for LPD-HCG. More photoelectrons can be stored in the additional capacitance of FD2 by turning DRG on. The LPD-LCG with incomplete CDS readout starts after the LPD-HCG by sampling a signal level. To apply CDS to both HCG and LCG signals in the LPD, additional sampling capacitors and comparator circuits are required to store the LCG reset voltage.[4] Without a spatial cost, we adopt a single readout circuit for complete CDS of HCG and incomplete CDS of LCG. Side effects from the incomplete CDS such as a power supply reject ratio (PSRR) will be mitigated by PSRR compensation circuit techniques. Because the reset readout is performed after the signal readout during incomplete CDS operation, the power supply noise has no correlation between the reset and signal readouts. Thus, the incomplete CDS readout has a lower PSRR than complete CDS. To improve the power-supply noise immunity, internal voltage regulators are implemented and a PSRR compensation circuit is used as shown in Fig. 2(c). The improved PSRR performance is shown in Fig. 2(d).

After the LPD readouts, FD3, FD2, and FD1 are successively connected together by turning on SW and DRG, and the voltage level of FD1 becomes the reset level of SPD-CDS. After STG is turned on, photoelectrons from SPD are transferred and sampled to FD1, so that the complete CDS is done for SPD-CDS. Continuously, the signal level of the overflow photoelectrons generated at high illuminance are firstly read out as they have already accumulated in the in-pixel storage capacitor. After DRG is turned off and SW and RG are turned on, the in-pixel capacitor is discharged to the reset level. The reset level is sampled at FD1 by turning DRG on again. Consequently, this operation becomes the incomplete CDS of the SPD-LOF.

Since a large number of electrons can be stored in the in-pixel capacitor, the DSW transistor enables fast discharge by shortening the discharge path of the capacitor. In Fig. 3(a), the simulation results show that the reset settling time of 1 μs is achieved by adding DSW, to support higher frame rate. The simulation result is verified by the measurement results as shown in Fig. 3(b). The reset settling has been measured; the average output code of SPD-LOF is set to 2000 LSB, and if reset sampling is incomplete, the output code will be less than

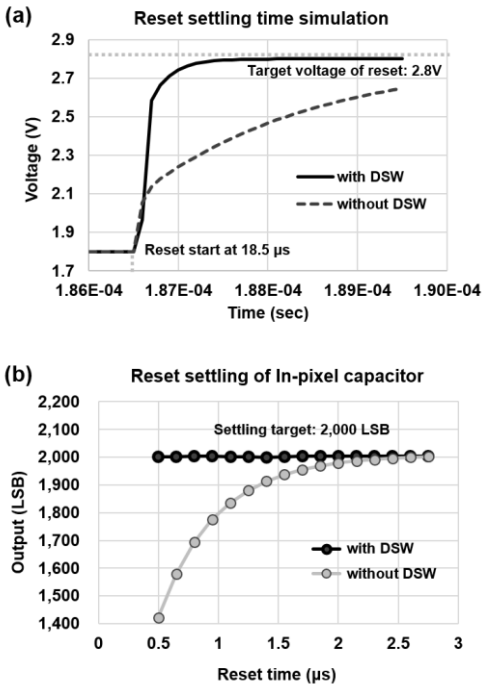

Figure 3. In-pixel capacitor reset settling comparison: (a) simulation results of reset settling at FD3 in SPD and (b) the measured results of SPD-LOF outputs with and without DSW.

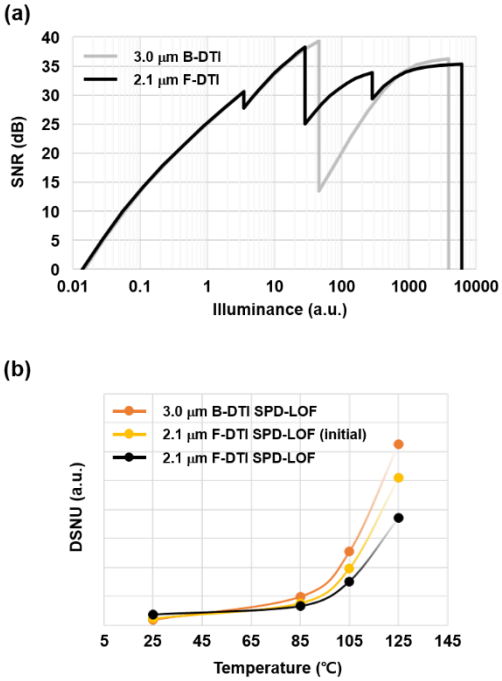

Figure 4. (a) SNR curve (at Tj 105 °C) estimated by the measured parameters during 11 ms integration time of both LPD and SPD, and (b) DSNU of SPD-LOF. The initial indicates before surface curing.

2000 LSB. The result confirms that we have achieved the settling time of less than 1 µs with DSW.

III. Result and Discussion

A. HDR charateristics at high temperature

Based on DR defined as the ratio between the exposure level at 0-dB (SNR1) and the saturation exposure level, dark random noise (RN) and dark signal non-uniformity (DSNU) are expected to be major degradation sources of DR and SNR at high temperature. To reduce RN, the width and length of the SF were optimized and high CG of 185 µV/e- was achieved by reducing the FD capacitance of the LPD. As a result, the input-referred RN of 0.83 e- was measured. At Tj 85 °C, a single-exposure DR of 120 dB was obtained by the aid of the in-pixel storage capacitor with four-readout scheme.

In Fig. 4 (a), the estimated SNR curve of the 2.1 µm F-DTI pixel is compared with that of a 3.0 µm B-DTI pixel at Tj 105 °C. The example of a 3.0 µm B-DTI pixel operates with three-readout scheme; LPD-HCG, LPD-LCG, and SPD-LOF. A large SNR drop has been found during the transition to SPD-LOF for the 3.0 µm B-DTI pixel. The DSNU of SPD-LOF dominantly degrades the SNR level with only three-readout; this can be improved by adding the SPD-CDS mode in the 2.1 µm F-DTI pixel. We maximize the FWC of SPD up to 10,000 e- to further improve the SNR during the transitions from LPD to SPD. Nevertheless, the SNR is still deteriorated by DSNU in SPD-LOF at high temperature.

Since the main source of the fixed pattern noise is the dark current generation in FD3. We found that the DSNU of the 3.0 µm B-DTI pixel is greater than that of the initial version of the 2.1 µm F-DTI pixel due to the larger FD leakage. The reduction of DSNU is contributed to the surface curing process at the initial 2.1 µm F-DTI pixel. As the temperature increases, the DSNU of SPD-LOF shows exponential behavior as shown in Fig. 4(b). By applying additional defect curing process, only for the F-DTI process, the DSNU of the 2.1 µm F-DTI pixel exhibits the extra reduction. With the merits of the F-DTI, the increase in SPD FWC and the decrease in DSNU enable to improve the SNR during the LOFIC operation. We finally achieve the minimum SNR more than 25 dB at high temperature.

B. Sensor characteristics

The 2.1 µm F-DTI pixel is fabricated and the sensor performance is summarized in Table 1. The FWC of SPD reaches 10,000 e- for SNR improvement and the high density storage capacitor is employed to achieve a single exposure DR of 120 dB at high temperature.

Table 1. Chip characteristics.

Characteristics	2.1 µm F-DTI
Process	Pixel 65 nm / Logic 28 nm, stacked BSI
Power supply	2.8 V / 1.8 V / 1.05 V
Pixel array (H x V)	3840 x 2160
Max frame rate	36 fps @ 12 bit
FWC (LPD, SPD, in-pixel capacitor)	10 ke-, 10 ke-, 210 ke-
Sensitivity	32000 e-/lux.sec (RCCB)
Sensitivity ratio	10
Conversion gain (HCG, LOFIC)	185 µV/e-, 4.2 µV/e-
Read noise (HGC) @ 85°C	0.83 e-
Single exposure DR @ 85°C	120 dB
Transition SNR @ 105°C	25 dB
Color filter array	RCCB (RGGB, RCCG, RYYCy support)

Figure 5. Chip micrograph.

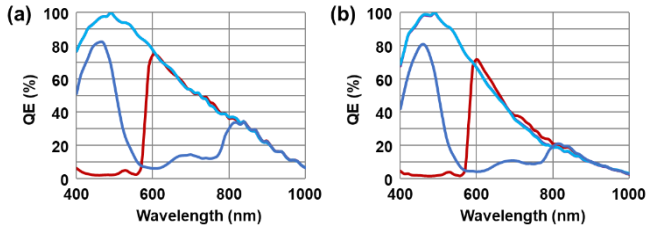

Figure 6. Relative quantum efficiency (QE) of (a) LPD and (b) SPD of RCCB color filter array.

Along with the very competitive HDR characteristics, our 2.1 μm F-DTI pixel supports various color filter arrays; RCCB, RCCG, RGGB, and RYYCy, and the relative QE of RCCB is shown in Fig. 7. Finally, the representative HDR features compared with the previous works are summarized in Table 2.

Table 2. HDR performance comparison.

HDR characteristics	This work (F-DTI)	IEDM 2022 [6]	IEDM 2021 [3]	ISSCC 2020 [4]	IISW 2019 [2]
Pixel pitch	2.1 μm	2.1 μm	2.1 μm	3.0 μm	3.0 μm
HDR Technology	Sub-pixel, LOFIC	Sub-pixel, LOFIC	LOFIC	Sub-pixel, LOFIC	LOFIC
FWC (LPD / LOFIC)	10 ke- 210 ke-	10 ke- 1.8 Me-	10 ke- 600 ke-	12.8 ke- 166 ke-	20 ke- 175 ke-
Single exposure DR (based on total noises)	120 dB	140 dB	110 dB	121 dB	96 dB
Min. SNR @transition	25 dB @ 105°C	23 dB @ 105°C	25 dB @ 125°C	25 dB @ 100°C	25 dB @ 100°C

IV. Conclusion

We have developed a 2.1 μm F-DTI pixel with LED flicker mitigation for automotive applications. A single exposure DR of 120 dB is achieved by employing sub-pixel architecture capped with an in-pixel storage capacitor. The capacitor can enormously extend charge-accumulating capability of the pixel supported by DSW transistor. Minimum SNR stays over 25 dB by increasing FWC of SPD and reducing DSNU of SPD-LOF with the merits of F-DTI process and four-readout scheme.

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