110dB High Dynamic Range Continuous Non-Uniform TTS and Linear ADC Scheme Using A 4.6 µm Stacked Digital Pixel Sensor

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1. Introduction

Demands for the global shutter (GS) image sensor with low power consumption, small chip size, and wide dynamic range (DR) are increasing for always-on, buttery-powered wearable AR/VR devices. The digital pixel sensor (DPS) is one of the solutions to realize such devices [1][2], and the authors have reported two DPS's. One is a 512 × 512 pixel sensor with a 4.6µm pixel [3][4], and the other is a 1024 × 832 pixel sensor with a 4.0µm pixel [5].

The 4.6µm pixel DPS operates in a triple quantization (3Q) scheme to enhance DR and achieves 127 dB DR with a power consumption of 5.75 mW at 30 fps. In the 3Q operation, a time-to-saturation (TTS) quantization is performed during the exposure time, followed by the two linear quantizations using single-slope analog-to-digital conversion (ADC). The first quantization has a high conversion gain (CG) signal, called "PD ADC", and the other has a low CG signal, called "FD ADC". Its initial version and the improved version were reported in [3][4] and [6], respectively.

In addition to the 3Q scheme offering ultra-high DR capability with a signal-to-noise ratio (SNR) drop at the mode-junction points, the stacked DPS in [3][4][6] can operate in other quantization schemes utilizing its in-pixel time-to-digital and ADC functions by modifying pixel signals and reference voltages.

One of such schemes is the dual quantization (2Q) scheme that combines a time-stamp (TS) quantization and a single-gain linear ADC modes [5]. Hereinafter, we call it "TS-Linear" scheme. While the maximum DR is reduced to 107dB, this scheme has an advantage of reducing SNR drop at the mode-junction point. It is because this scheme does not involve the low CG ADC mode that does not allow correlated double sampling (CDS) operation. It also has the advantage of possible simplification of the pixel circuit due to the single-gain ADC mode. On the other hand, TS-Linear scheme may suffer SNR drop degradation due to the PD FWC variation.

In this paper, we apply another 2Q scheme that combines TTS quantization and a single-gain linear ADC mode that we call "TTS-Linear" scheme [7]. In this scheme, PD FWC variation does not affect the SNR drop at the junction point. Pixel can be simplified the most among three schemes presented so far, which suggests pixel-size and power-consumption reductions are possible. To overcome its disadvantage of the lowest DR (103dB) among the three schemes, we demonstrated a DR-enhancement capability up to 110dB by introducing a nonuniform TTS operation, whose details are described in the following section.

2. Sensor Operations

We used the stacked DPS in [6] to compare the three quantization schemes in the previous section. It was fabricated by a 45 nm CIS and 65 nm logic stacked sensor process. These two layers are connected by pixel-level interconnects using the Cu-to-Cu hybrid bonding (HB) technology [8]. It has a 512 × 512 pixel array with a 4.6µm pixel pitch and is implemented in a 4mm ×

4mm die.

Table 1 compares equivalent pixel circuit diagrams, signal timing diagrams, and performance score boards of the three quantization schemes.

3Q pixel in (a) is based on a dual conversion-gain (DCG) CIS pixel circuit with anti-blooming (AB) gate and in-pixel bias-current source (Vbn) in the top layer. The ADC circuit on the bottom layer includes the coupling capacitor (Cc) and a voltage comparator with the reset switch (Comp_RST) for analog CDS operation. The quantization result is stored in the 10-bit SRAM that is driven by ADC codes distributed to the whole pixel array. The state latch and control logic circuit manage the automatic signal selection of the 3Q signals. The comparator is biased in the sub-threshold region for low power operation.

TS-Linear pixel (b) does not require DCG. The signal-selection logic can be simplified, too.

TTS-Linear pixel (c) does not need the selection logic and Comp_CHK signal.

Timing diagrams of 3Q and TS-Linear schemes in Table 1 are from the previous reports [5] [6].

In 3Q scheme, low CG is chosen by connecting FD node to the storage capacitor, C_S, in TTS and FD ADC modes. PD ADC is performed with high CG. Auto-zeroing operation is done before every quantization mode by pulsing the comparator reset signal, Comp_RST. Signal charge transfer is done by TG pulse just before PD ADC mode.

In TS-Linear scheme, the comparator reference signal, VRAMP, ramps up during the integration period for TS operation. Auto-zeroing operation is done before both quantization modes by pulsing the comparator reset signal, Comp_RST

In both 3Q and TS-Linear schemes, the TG pulse potential is optimized for a complete PD charge transfer.

A timing diagram for the newly proposed TTS-Linear operation is also shown in Table 1 (c). First, PD is reset using AB gate. Then, integration starts when AB gate turns off. Before cutting RST and Comp_RST that have performed auto-zeroing operation, TG bias is raised to a particular level between PD Vpin and the FD reset level. Then, photo current starts pulling down FD potential. When FD potential goes low enough for the comparator input to go below the reference voltage, VRAMP, the comparator flips to latch the quantization code on the SRAM. The integration (TTS operation) is ended when AB is turned on to reset PD again. At the same time, linear ADC is done to digitize low-light signal which TTS has not detected. Digital counts 0-511 (9b) are reserved for the linear ADC and 512 - 767 (8b) for the TTS operation.

3. Non-uniform TTS

The proposed 2Q TTS-Linear operation achieves 103 dB DR. To recover its lower DR than those with the previous operation modes, non-uniform TTS scheme is introduced where non-linear ramp operation was used to reduce the conversion time [9][10].

Fig. 1 shows a conceptual timing diagram of the non-uniform TTS scheme together with that of the conventional uniform TTS scheme. Seven different TTS clock widths are assigned within the 8bit TTS period. The shortest clock width is assigned for the highest light portion, followed by longer-width clocks toward the end of the TTS period. The shorter clock width can detect higher light levels than with the longer clock widths in the uniform TTS scheme. Thus, this non-uniform TTS scheme can extend the DR. Also, it can suppress the oscillation in the SNR plot that is seen in the linearized photo-response curve with the previous operations [4].

4. Characterization

A linearized pixel photo response curve (PRC) and a SNR curve with external FPN correction, and a magnified photo-response curve in the low-light region are shown in Fig. 2 (a) and (b), respectively. Good low light linearity and SNR of 32 dB at the junction point

between the TTS and the linear quantization have been obtained. Also, DR of 110dB has been achieved, thanks to the nonuniform TTS with the oscillation in the SNR at high light portions suppressed.

Table. 2 summarizes measured performances of the three quantization schemes. The proposed 2Q TTS-linear scheme features the best SNR characteristic and potentially smaller pixel size and lower power consumption among the three schemes. On the other hand, the previously reported 3Q scheme provides the best DR and low-light noise performance, and 2Q TS-Linear scheme offers a balanced performance.

5. Summary

This paper presents a new non-uniform TTS-Linear ADC operation scheme and its characteristics using the 4.6µm 512 × 512 pixel DPS. It has been confirmed that the TTS-Linear ADC operation generates no large SNR drop at the mode junction point and achieves single exposure 110dB DR. Also, it is expected that the pixel size and power consumption become smaller with this operation, due to its simpler circuit configuration.

References

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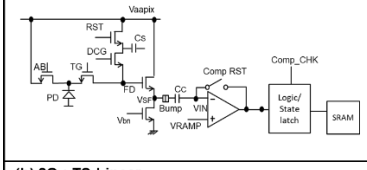
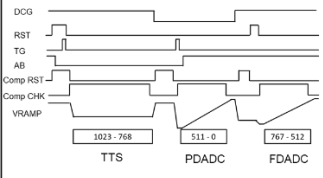
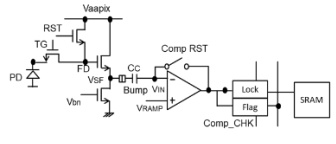
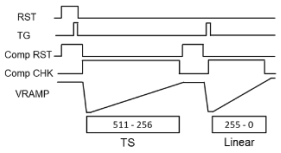
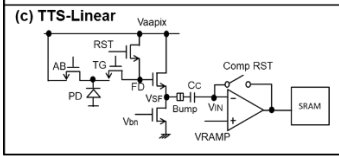
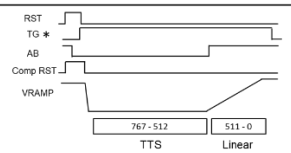
Table 1. Equivalent circuit and timing diagram of 3Q, 2Q and TTS-Linear scheme.

Equivalent circuit	Timing diagram	Dynamic range	Dark Noise	SNR drop	Pixel size	Power consumption
(a) 3Q : TTS-PDADC-FDADC 		Best	Best	Worse	Better	Better
(b) 2Q : TS-Linear 		Better	** Best	Better	Better	Better
(c) TTS-Linear 		Better	Better	Best	Best	Best

* TG is moderately ON to allow charges to flow from PD to FD. ** Although dark noise of 2Q is worse than other operations in Table 2, dark noise of the 2Q operation should be the same as that of the 3Q mode in principle.

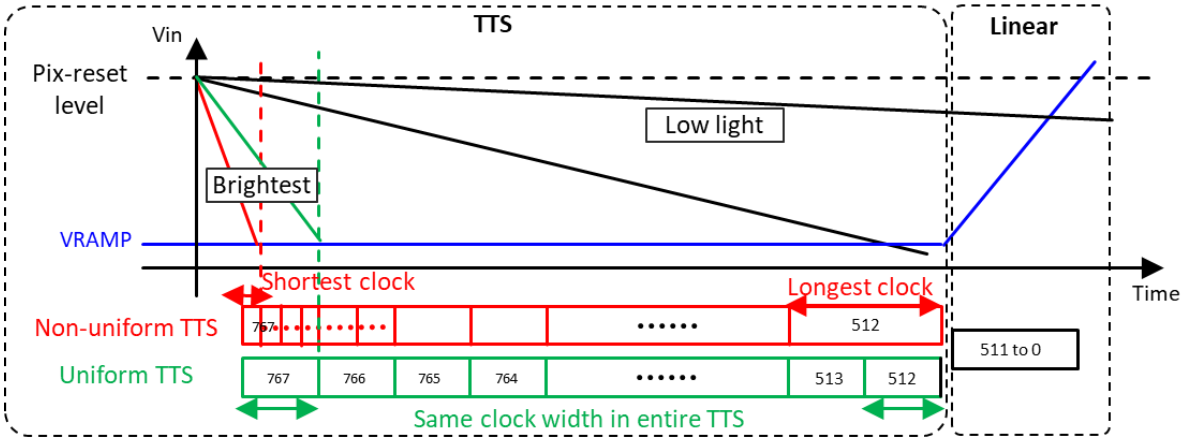


Fig 1. Conceptual timing diagram of non-uniform TTS and uniform TTS. Non-uniform TTS enhances the resolution in bright light region than uniform TTS and suppresses SNR oscillation there [4].

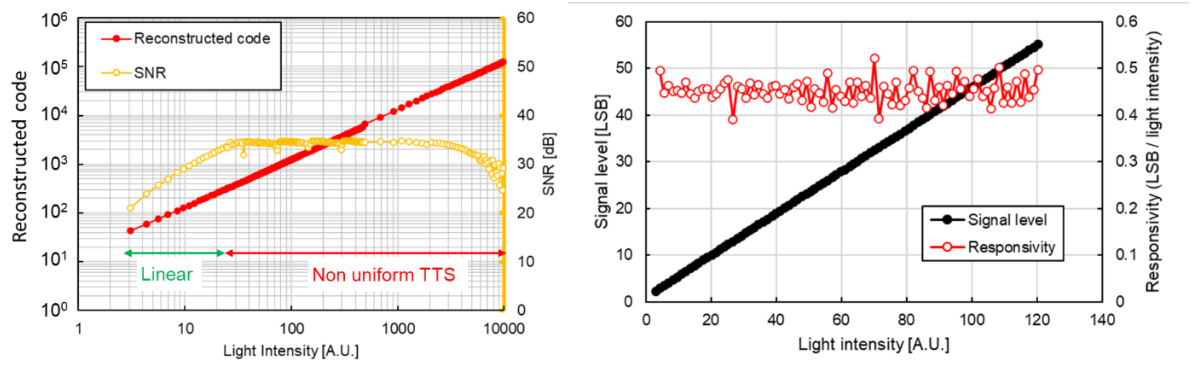


Fig 2. Linearized photo-response curve and SNR plot using non-uniform TTS (Left)

Magnified photo-response curve in low light region showing a good linearity (Right)

Table 2. Summary of 3 quantization schems (integration time = 1ms)

Specification	This work	Ikeno IISW 2023 [6]	Mori IEEE 2022 [5]
Pixel size	4.6 um	4.6 um	4.0 um
Pixel array	512 x 512	512 x 512	1024 x 832
In pixel Memory bit#	10 bit	10 bit	9 bit
ADC resolution	8bit(TTS) + 9bit(Linear)	8bit(TTS) + 9bit(PD) +8bit(FD)	8bit(TS) + 8bit(Linear)
Dynamic Range	110 dB (Non-uniform TTS)	127 dB	107 dB
Temporal noise (dark)	5.6 e-	4.0 e-	8.3 e-
FPN rms (dark)	35 e-	27 e-	64 e-
Conversion gain	170uV /e-	170uV /e- (HCG), 12.5uV/ e- (LCG)	150uV /e-
SNR at junction	TTS to Linear : 32dB	PD to FD : 27dB, FD to TTS : 35dB	TS to Linear : 23dB
Power	5.8 mW (30 fps)	5.8 mW (30 fps)	NA

FPN : without external FPN correction