A 5MPixel Image Sensor with a 3.45µm Dual Storage Global Shutter Back-Side Illuminated Pixel with 90dB DR

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Abstract - **While Rolling Shutter sensors with High Dynamic Range (HDR) performance have been commonplace for many years, Global Shutter (GS) sensors have been lagging behind in demonstrating HDR capabilities. The combination with small pixel pitches and back-side illumination (BSI) has been particularly rare. This paper presents a back-side illuminated, 3.45µm HDR GS pixel making use of a dual storage Voltage Domain Global Shutter (VDGS) pixel, achieving up to 90dB Dynamic Range.**

INTRODUCTION

In recent years, the industry has seen several examples of image sensors supporting Dual Conversion Gain (DCG), Overflow or Multiple-Exposure HDR techniques [1-8]. Besides implementations for scientific and niche applications, BSI global shutter pixels have been introduced mostly recently [4, 9, 10, 11]. Amongst those, [11] stands out as a solution that combines HDR and BSI in a small pixel pitch.

This work introduces a 5 Megapixel Global Shutter sensor with 3.45µm dual storage pixels. The back-side illuminated, VDGS pixel uses a Stacked Pixel Level Connection (SPLC) and full Deep Trench Isolation (DTI). The sensor supports a single capture (linear) and two dual capture (HDR) modes: Dual Conversion Gain (DCG) and Dual Exposure (DEXP).

Taking advantage of these recent technology advances illustrated in Figure 1, the performance demonstrated in [11] has been substantially improved. Noise levels lower than 2e- can be achieved at high gain.

In DCG mode, a 2.7e- noise level can be combined with a full well capacity of >20000 electrons, resulting in a Dynamic Range (DR) of 77dB. In DEXP mode, up to 90dB DR has been demonstrated.

With Nyxel technology, a QE of >40% at 940nm, and a peak green QE of 84% was achieved. Thanks to the SPLC and storage on High Density MiM capacitor in a separate wafer, the pixel has a Global Shutter Efficiency (GSE) well below -100dB.

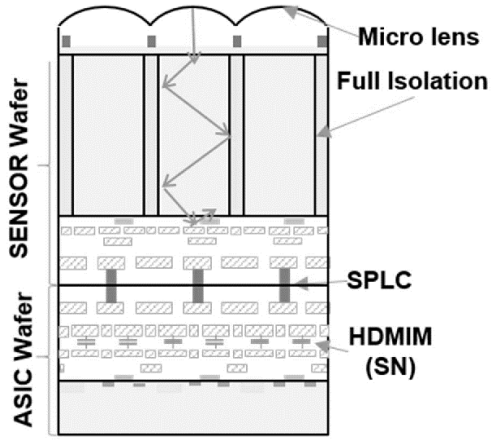

Figure 1 Process Configuration of the VDGS Pixel

Aside from the highly competitive performance at 3.45µm, the technology offers great promise to further shrink HDR global shutter pixels in the future.

The 5 Megapixel sensor operates at up to 120fps in linear mode (10-bit or 12-bit output) and 60fps in the dual capture modes (12-bit, 14-bit or 16-bit output). The on-chip HDR recombined signal is transmitted off the sensor by means of a 4-lane MIPI D-PHY or a 4- or 8-lane sub-LVDS interface. Furthermore the sensor supports various trigger modes (in linear and HDR modes) and a background subtraction mode.

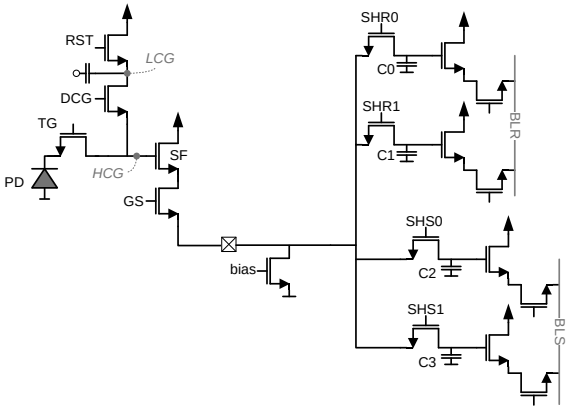

Figure 2: Pixel Schematic of the dual storage VDGS pixel

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PIXEL CIRCUIT

The dual storage pixel architecture is shown in Figure 2. It builds on the differential pixel topology introduced in [9] but adds a second set of capacitors which may be utilized to store the dual capture signals (DCG or DEXP) in the HDR modes.

DUAL CONVERSION GAIN OPERATION

The operation of the DCG is similar to [12, 13] but now being applied to a Global Shutter Sensor with the timing sequence shown in Figure 3. The CDS (SHR, SHS) voltages for both HCG and LCG signals are stored on the two sets of capacitors. Using this technique, the dynamic range, 64dB in linear mode, is extended to 77dB.

This dynamic range is achieved by making use of an analog gain 7x on the HCG channel. The analog gain is chosen to optimize the noise while keeping the SNR at the transition between the gain channels (SNR_tran) above 26 dB as seen from the measurement results in Figure 4.

The main contributors to the SNR drop for this operating mode are the higher read-noise and fixed-pattern-noise in the LCG channel due to leakage variation on the storage node from pixel to pixel.

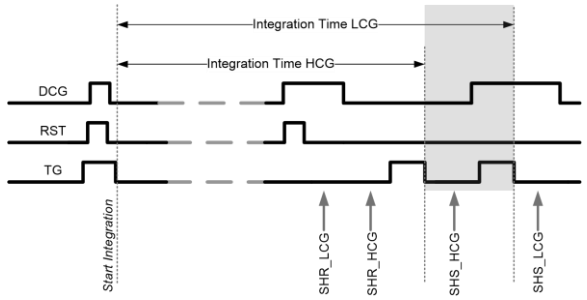

Figure 3 DCG Timing Diagram

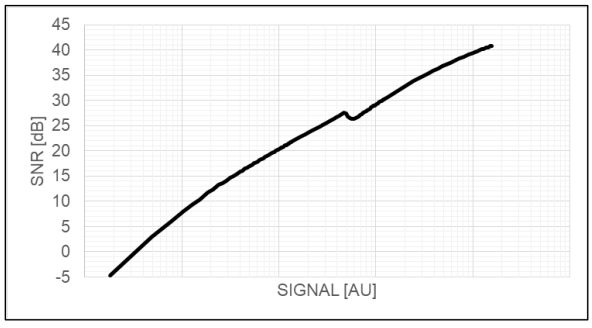

Figure 4: Dual Conversion Gain SNR

From the timing diagram, it is clear that the HCG and LCG signals do not have the exact same exposure time due to the second transfer operation. As a result the gain ratio between these two captures varies with the integration time.

This effect will be particularly pronounced for shorter integration times. To accommodate this, the sensor adjusts the gain ratio in the 2D HDR Combine ISP (Figure 5) adaptively as the integration time changes. This ensured that the combined HDR signal remains linear all the way down to the minimum exposure time.

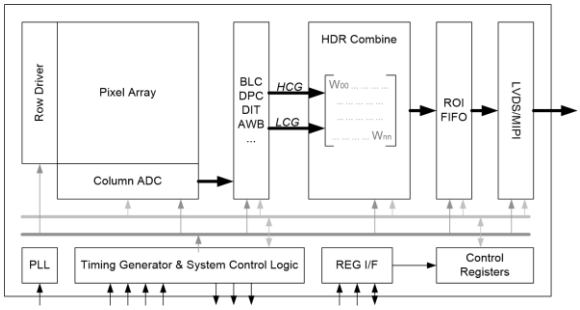

Figure 5: Top Level Block Diagram highlighting the HDR combine function

DUAL EXPOSURE OPERATION

Alternatively, the sensor supports a dual exposure HDR scheme [6, 11]. The long exposure is captured on the HCG channel while the short exposure is captured on the LCG channel.

With the HCG channel at an analog gain of 1x and while applying an exposure ratio of 7x, a dynamic range of 90dB can be achieved. A higher dynamic range may be achieved by applying a larger exposure ratio or higher gain for HCG, but in that case the SNR (Measurement results shown in Figure 6) at the transition point would drop below acceptable levels.

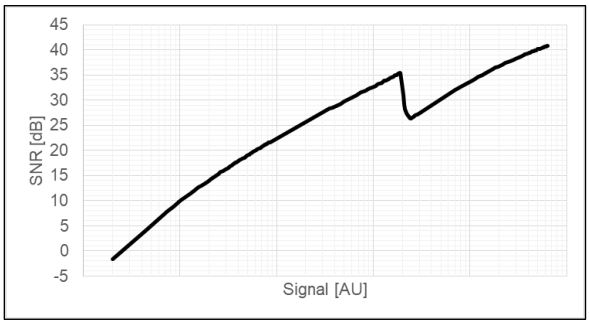

Figure 6: Dual Exposure SNR

FUTURE WORK: VDGS EXPOSURE TIME CHALLENGES

Taking a closer look at the timing diagram for the linear mode (Figure 7), it is clear that the finite time it takes to sample the Reset and Signal values, has an impact on the exposure time control of the sensor as was already clear from the HCG/LCG exposure time difference raised earlier.

In a linear mode of operation with a single readout, the time it takes to reset the photodiode and the floating diffusion and the time it takes to sample the reset value, puts a lower limit on the integration time that can be supported. Due to the fact that these are global operations, they add in additional requirements for the on-chip charge pumps, the row drivers and the power supply network. The pixel timing needs to be carefully tuned to minimize the minimum exposure time achievable without introducing any artefacts.

A relatively straightforward solution to this problem may be to introduce an additional "photodiode reset gate" as is common for charge domain global shutter pixels e.g. [6].

However, while certainly reasonable in a 3.45µm pitch, this additional gate would eventually limit the scaling potential to pixel sizes approaching 1µm. Future innovations are expected to be necessary to reduce the sampling time as resolutions grow larger, pixel sizes smaller and capacitor density increases [14].

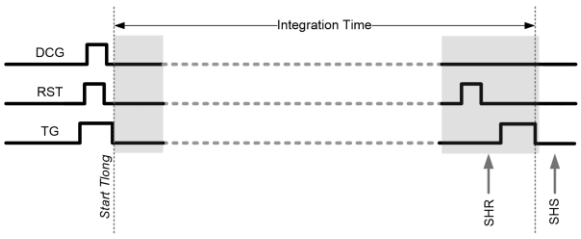

Figure 7: Single Capture (linear) Timing Diagram

CONCLUSION

This paper presented silicon results of a 5 Megapixel Global Shutter imager supporting two HDR modes. As shown in Table 1, this product advances the state-of-the-art in small pixel Global Shutter HDR performance combining low light performance with high dynamic range, while maintaining a high SNR at the transition point. An image taken with the sensor is shown in Figure 8.

Figure 8: Image Captured with the sensor

Table 1: Performance Summary & Comparison

Parameter	**This Work (@ 70C)**	**[11]**
Resolution	5 Megapixel	1 Megapixel
Pixel Pitch	3.45µm	3.75µm
GS Architecture	Voltage Domain Global Shutter	Voltage Domain Global Shutter
Full-Well Charge	20.000e-	8100
Temporal Noise Linear	2e- at high gain	8.5e-
Temporal Noise HDR	2.7e- in DCG 4.5e- in DEXP	16.8e-
Fixed Pattern Noise	1.4e-	N/A
HDR Single Exposure	77dB	59dB
HDR Dual Exposure	90dB	102dB
SNR_tran	>26dB	N/A
QE – 940nm	41%	N/A
QE - Green	84%	N/A
GSE	< - 100dB	< - 80dB
Frame Rate	60fps	50fps
Process	BSI 45nm, Pixel Level Stacked	BSI 65nm

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