# A High Dynamic Range APS-C Sized 8K 120-fps Stacked CMOS Image Sensor

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## Introduction

In this paper an APS-C size 43 Mpixel rolling shutter image sensor is presented with multiple techniques of increasing the dynamic range of the sensor. The sensor is targeted for use in cinematographic applications requiring high dynamic range image sensing.

## Sensor architecture

The stacked sensor architecture, depicted in Figure 1, consists of a top-side die containing the pixel array with a resolution of 8448 x 5376 pixels, as well as the bonding pads, and a bottom die containing an 8 x 8 array of identical readout circuit blocks (core cells). These core cells consist mainly of column parallel analog-to-digital converters, SRAM memory and pixel control signal drivers. The pixel array is connected to the bottom wafer circuits using Cu-Cu hybrid bonding.

Figure 2 illustrates the data path between pixel and sensor output. Per pixel column, 8 column buses connect via the hybrid bonding to the analog to digital converters in the 8 rows of core cells on the bottom wafer. The 8 selected pixels rows are physically adjacent on the top wafer, which minimizes rolling shutter artefacts. In each row of core cells on the bottom wafer, each column uses a 14-bit ramp ADC to convert the signal on the column bus to a digital value. The digitized outputs are fed to a logic adder which is also connected to part of the SRAM frame buffer. The complete frame buffer memory is distributed across all core cells within the chip. To transmit the data to the sensor output, the adder output is multiplexed over a horizontal digital bus to the data formatting block which is located outside the core cell area. This block re-organizes the data, applies black level correction and formats the data to be sent out over 16 high-speed data output channels.

## High dynamic range modes

The 3.2 µm pixel contains a dual conversion gain (DCG) readout architecture [1] providing low-noise readout in dark image regions while also supporting a high full well charge readout. In the dual conversion gain readout mode, a frame rate of up to 60 frames per second can be achieved for the 8K video format. In this mode, the presented sensor achieves a full well charge of 26.5 ke- and a total combined dynamic range of 76.4 dB. The sensor also allows reading out only the low or high gain path in a single conversion gain (SCG) mode at up to 120 frames per second.

To further increase the dynamic range of the sensor, the SRAM frame buffer in the core cells allows for an intermediate pixel readout and storage without interrupting the exposure. Figure 3 shows the conceptual timing of the multiple exposure rolling shutter mechanism, which increases the full well charge of the sensor beyond the limit of the photodiode full well charge. The total exposure time (Texp) is in this case divided in four equal sub-exposure times (Texp0…3). When the first exposure (Texp0) is finished, the pixel is read out in either single or dual conversion gain mode and converted

to a digital value. The result is stored in the frame buffer. During such intermediate readout, the pixel charges are cleared from the pixel's photodiode. After the second exposure (Texp1), the pixel signal is digitized again and the resulting value is added to the value from Texp0. The result of this operation is stored back in the SRAM frame buffer. The same operation is repeated for the third exposure time (Texp2). After completing the fourth sub-exposure, the digitized value is added to the previously stored data, but is now sent directly to the data formatting block and the output interface.

The response measurement and Photon Transfer Curve (PTC) executed with 1, 2 and 4 sub-exposures are plotted in Figure 4. Because of the DCG readout, a high and low gain response and PTC is plotted for each case. The response measurement shows that for the three sub-exposure cases the conversion gains are equal. However, the saturation level is linearly correlated to the number of sub-exposures. The PTC plot shows that also the peak variance, and thus also the full well charge, is linearly correlated to the number of sub-exposures. It increases from 26.5 ke- to 54.3 ke- and 108.6 ke- for the 2-exposure and 4-exposure modes respectively. The dynamic range increases similarly, to 80.1 dB and 83.5 dB respectively. Table 1 summarizes the basic performance parameters of these sensor modes.

It is possible to increase the dynamic range even further by applying non-equal sub-exposure times as shown in figure 5. After each sub-exposure, the converted signal level is digitally clipped to a programmable level before it is added to the previously stored sub-exposure data and written back to the frame buffer. This operation results in a multiple slope response with up to a maximum of 4 slopes. The slope ratios of the multiple slope response are a function of the sub-exposure time ratios, similar to the known multiple slope response when applied in the analog domain [2]. The knee points themselves are accurately controlled by the sub-exposure times and the saturation clipping of the A/D converter. Because in this sensor the clipping occurs in the digital domain, accurate knee point levels can be set and no pixel-to-pixel variation is present. This makes off-chip linearization of such a multiple slope response much more convenient compared to analog domain multiple slope where typically there is a significant pixel-to-pixel variation on the knee point. Measured results of the response curve and linearized response are shown in Figure 6, using 4 sub-exposures with a ratio of 8x, 4x, 2x and 1x for exposures 0, 1, 2 and 3 respectively.

Besides the 8K video format, the sensor supports readout of a 4K binned image at frame rates up to 120 frames per second with a full well charge of >100 ke- and total dynamic range of >81 dB; or 60 frames per second with a full well charge and dynamic range of >200 ke- and >84 dB using the multiple exposure rolling shutter mechanism with 2 sub-exposures.

**High-speed data readout**

With the use of a custom high-speed 5.25 Gbps interface link, these frame rates can be achieved using only up to 16 channels. The sensor was fabricated using a 65 nm stacked CMOS image sensor process. Figure 6 shows a picture of the fabricated sensor in a 363-pins ceramic LGA package.

### *References*

[1] Wang, X., Wolfs, B., Meynants, G., & Bogaerts, J. (2011, June). An 89dB dynamic range CMOS image sensor with dual transfer gate pixel. In Proc. Int. Image Sensor Workshop (pp. 248-251).

[2] Decker, S., McGrath, D., Brehmer, K., & Sodini, C. G. (1998). A 256/spl times/256 CMOS imaging array with wide dynamic range pixels and column-parallel digital output. IEEE Journal of solid-state circuits, 33(12), 2081-2091.

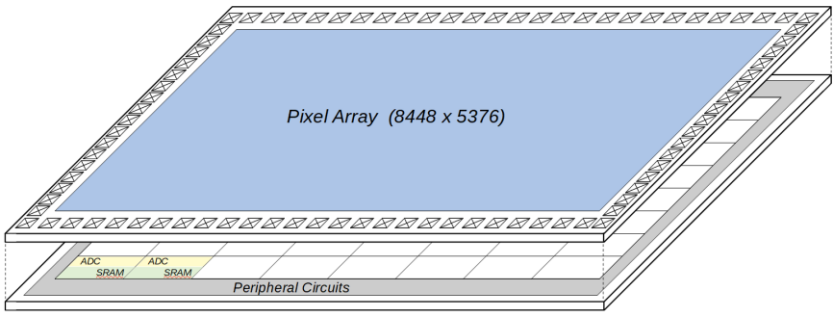


*Figure 1 – Stacked sensor architecture.*

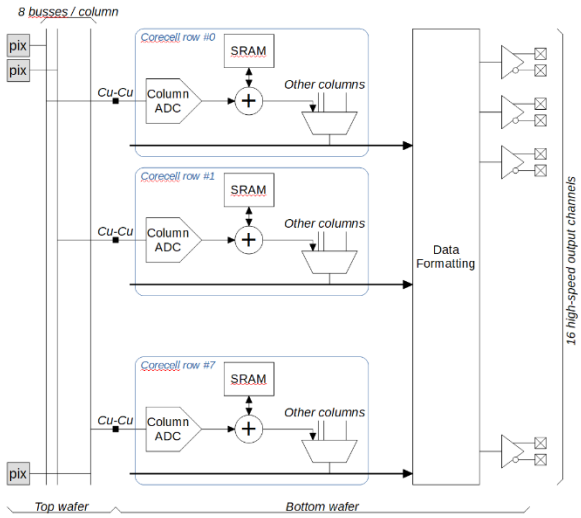


*Figure 4 – Data readout path from pixel to sensor output.*

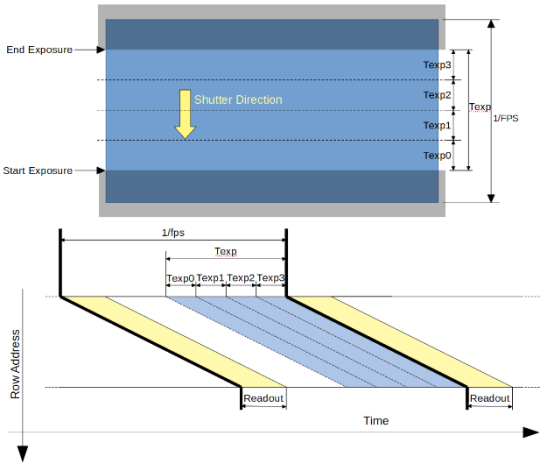


*Figure 3 - Multiple exposure rolling shutter mechanism timing (bottom) and position of pointers on the array (top).*

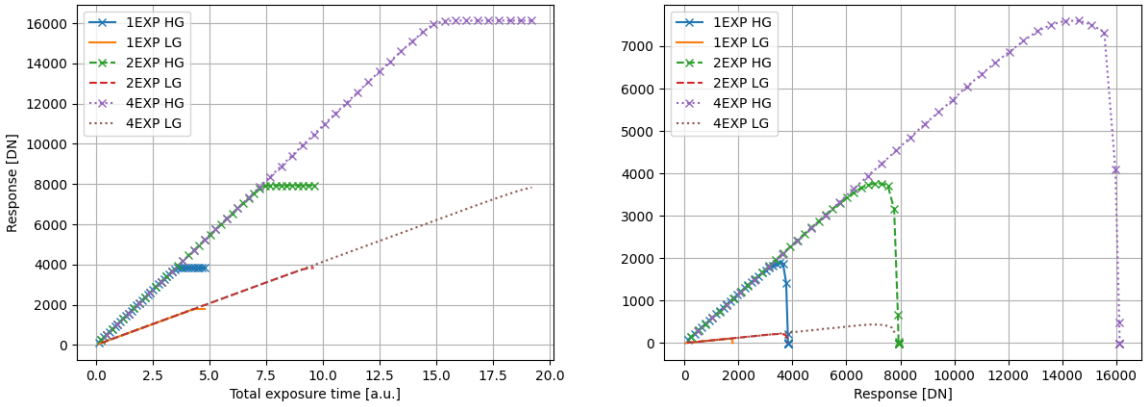


*Figure 2 – Response curve (left) and Photon Transfer Curve (right) measurement results of high gain (HG) and low gain (LG) readout path in DCG readout mode, using 1, 2 and 4 sub-exposures (nEXP = 1, 2 and 4).*

*Table 1 – Summary of sensor performance characteristics in DCG readout mode.*

| **Process** | 65nm CIS stacked | | |
|---|---|---|---|
| **Resolution** | 8448 (H) x 5376 (V) | | |
| **Pixel pitch** | 3.2 µm | | |
| **# sub-exposures summed** | 1 | 2 | 4 |
| **Full well charge (LG)** | 26.5 ke- | 54.3 ke- | 108.6 ke- |
| **Dark temporal noise (HG)** | 4.0 e- | 5.3 e- | 7.3 e- |
| **Dynamic range** | 76.4 dB | 80.1 dB | 83.5 dB |
| **Maximal frame rate** | 60 fps (*) | 60 fps | 30 fps |

(*) in high dynamic range dual gain readout mode due to output data rate limitation. A maximal frame rate of 120 frames per second can be achieved when reading only the low-gain or high-gain pixel conversion path.

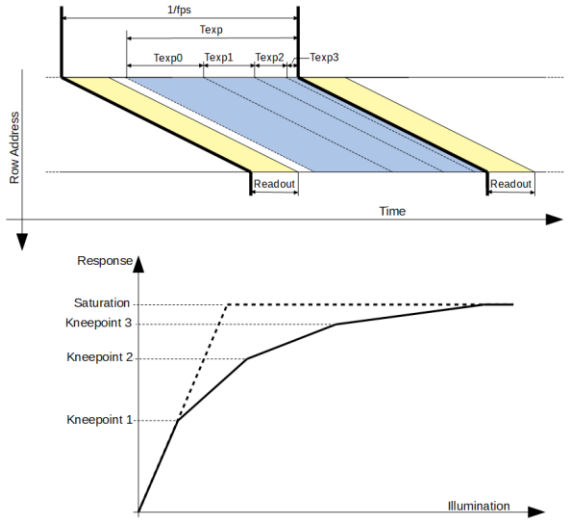


*Figure 5 – Timing illustration for the multiple slope HDR expansion (top) and knee points in the response curve (bottom)*

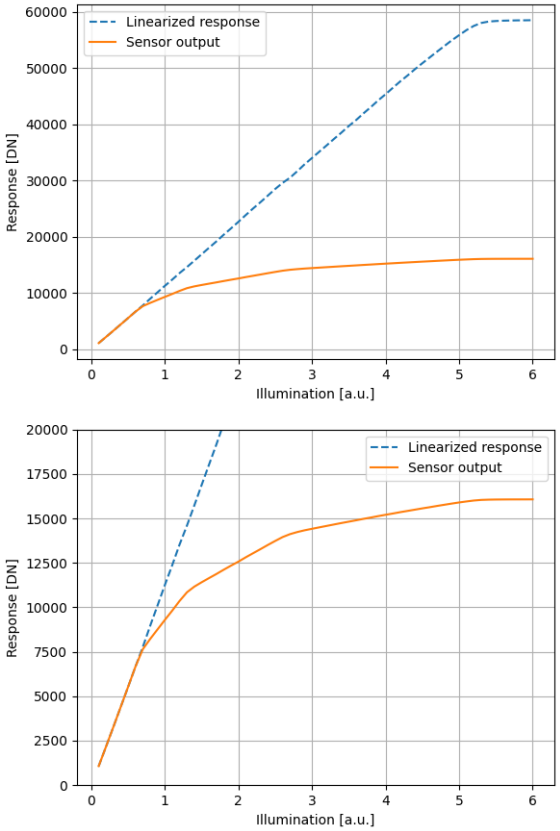


*Figure 6 – Measurement results of 4-exposure multiple slope HDR expansion, showing both sensor output and the linearized response (top) and zoomed in on the sensor output response curve (bottom) to better show the knee points*

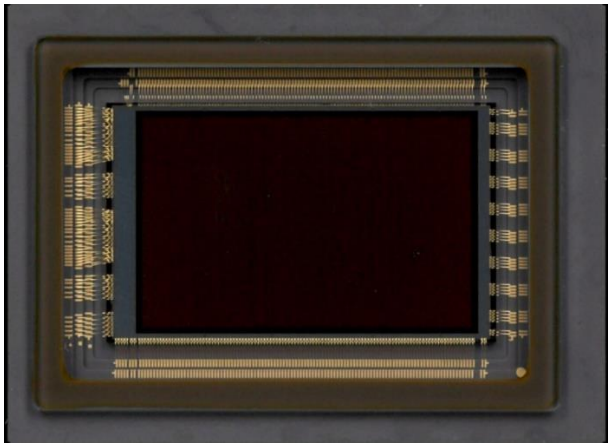

*Figure 7 – Fabricated and packaged sensor.*