A 90dB single-shot HDR, 0.5MP global-shutter image sensor with NIR QE enhancement, 20mW power consumption and smart event detection modes

A. Xhakoni, A. Fekri, P. Francis, S. Melsen, S. Janardhan, B. Hashani, A. Popa, K. Ruythooren, P. De Wit, R. Lafaille, K. Kawamura, A. Jaderi, K. Kimura, K. Ben Ali, R. Brolly, A. Andrade

ams OSRAM, Borsbeeksebrug 36, Antwerp, Belgium

adi.xhakoni@ams-osram.com, +32 3 2868902

1 Introduction

Consumer applications such as AR/VR require global shutter image sensors due to image artifact reduction and due to their capability to sync with a pulsed illuminator. Other key requirements are low system power, (achieved through high QE at NIR and sensor low power operation) and miniaturized silicon size. Furthermore, HDR operation is especially required for world facing cameras.

2 Sensor architecture

To satisfy the needs of consumer applications, we designed a 0.5MP image sensor with 2.79um voltage domain GS pixels with a packaged sensor footprint of only 2.3mm x 2.8mm, with architecture depicted in Fig 1. To meet the challenging requirements of footprint and power, we made extensive use of digital-friendly readout circuits starting with the ramp ADC, which contains minimal analog circuitry. Given the scaled technology node (40nm) of the logic layer, the power of the readout scaled dramatically compared to our previous designs in older technology node. Certain building blocks which were the most power hungry in our previous designs (e.g. ADC counter) experienced an order of magnitude of power consumption improvement. In addition, advanced power down techniques were used for optimizing current consumption by turning on specific blocks only when needed. The above techniques allowed for an allow ultra-low-power operation of the sensor (e.g. 18.5mW at 10bit, 30fps, 0.5MP).

To avoid potential column FPN issues, we decided to keep the ADC pitch same as the pixel pitch. This posed a challenge in the row driver design to keep the sensor footprint within specifications. Improvements in the row driver architecture and the use of 7 metal layers (made possible by the stacked technology) allowed achieving an exceptionally narrow row driver width of only 40um. The row driver was split in 2 parts (left and right of array) to half its width. The improvements in architecture, layout, and the usage of scaled technology node allowed for a sensor footprint which is mostly dominated by the pixel array rather than readout silicon.

3 HDR operation

The HDR technique validated in this sensor is shown in Fig 2. It uses charge-overflow-on-FD technique, with critical improvements over SOA. Overflow operation is done on FD, at a fraction (T1) of low-light exposure time (T0), with DR extended by T0/T1 ratio, with T0 exploiting the entire full well of PD and T1 exploiting the entire full well of FD. The technique makes use of the timing diagram of Fig 2 and works as follows. A) Long exposure T0 starts when TX toggles low. B) TX toggles high to a mid-level. This facilitates charge overflow from PD to FD (hence to reset) in case of medium or high light. C) Short exposure T1 starts when reset switch is turned off. At this point, any overflowing charge is collected on FD node. Since T1 is much shorter than T0 (e.g. 15x shorter), FD leakage affecting T1 and dark current affecting T0 are negligible. D) T1 exposure ends when TX toggles back to the

lowest level. T1 exposure is stored via S1 and S2 in C2. E) Finally, T0 exposure ends when TX toggles high. T0 signal is then stored on C1 via the S1 switch.

Despite storing 2 signal levels in the 2 in-pixel capacitors, CDS is still provided for the low light signal and DDS is provided for high light signal, as follows. Fig 3 shows 3 cases of light conditions (low, medium and high light). In case of low light condition, no overflow occurs. Therefore, T1 exposure stored on C2 is the correlated reset level for long exposure T0, allowing CDS hence low noise (~5e-) and low FPN (~3e-). In case of medium light level, overflow starts happening just after T1 starts (Fig 3, middle plot). To reconstruct the HDR image both CDS (C2-C1 signals) and DDS (C2 signal – dark reference) are needed during mid light. The dark reference to allow for DDS is achieved during row readout, by accessing the reset level of the pixel after reading the C2 and C1 signals. In case of high light (Fig 3, right plot) T0 exposure signal starts overflowing before T1 starts. This means that in case of high light, only T1 signal is used for the HDR reconstruction. Therefore DDS is used, CDS is discarded.

With the technique above, only 2 in-pixel capacitors are necessary for the 4 signals needed for HDR (low light + reset, high light + reset), as compared to the 4 caps needed by e.g. [2]. This method employing only 2 capacitors for 4 signals can be used with many other HDR techniques, including conventional LOFIC, dual exposure, etc. Compared to alternative HDR techniques, the proposed technique doesn't need FPN calibration, and pipeline readout is possible, improving low light performance. Fig 4 shows ~90dB DR with ~27dB at dip point.

4 Event detection mode

The sensor includes an event detection mode for low power operation. As shown in Fig 5, the sensor splits the pixel array into a programmable number of tiles composed of binned and/or subsampled pixels and runs at 1fps with low power (<3mW). A reconfigurable on-chip algorithm processes the variation of signal intensity in each tile and decides if an interesting event has happened. If yes, the sensor switches to a user-defined operation mode (e.g. 120fps, 10bit). This mode is quite useful for sparing system power in a multitude of applications including computing, doorbells, AR/VR, etc.

5 Conclusion

With a 2.3mm x 2.8mm packaged size (Fig. 6), the presented sensor is one of the smallest GS sensors ever reported. Despite its size, it packs 0.5MP, Mipi interface, ultra-low power operation, smart event detection modes and proves single shot HDR concept with pipeline operation. The specialty of the proposed HDR technique is that it reuses the same pixel storage capacitor for both reset level of low light condition and signal level of high light condition. Combined with high QE (~92%@vis, ~38%@940nm) it well compares against great works from the past [1],[2] and it is an ideal candidate for consumer AR/VR devices.

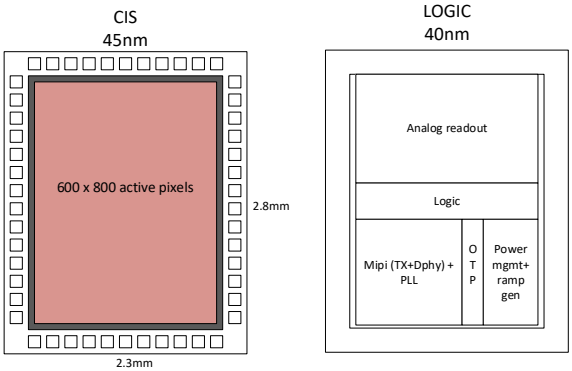


Fig. 1. CIS silicon (left) stacked on top of logic silicon (right) via hybrid bonding interconnect

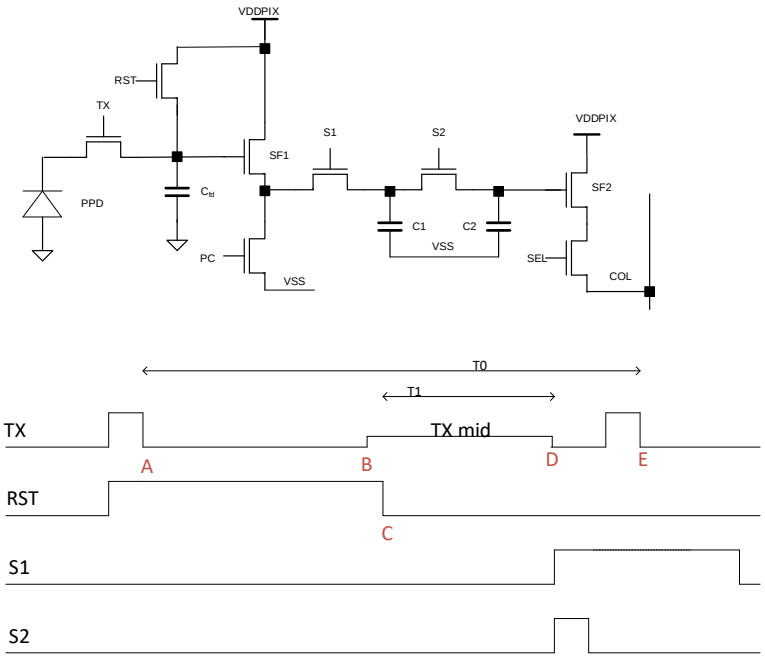


Fig. 2. Voltage domain GS pixel and HDR timing. C2 stores overflow signal (at high light) or reset signal (at low light). Reset level of overflow is read during row readout time. Only 2 capacitors are then needed to store reset low light, low light signal, overflow signal and reset of overflow. Overflow happens during short T1 at FD, avoiding need for large overflow cap and reducing DSNU and dark current.

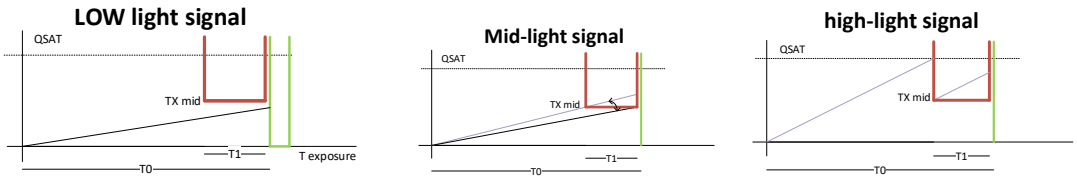


Fig. 3. During low light conditions (left plot) no signal overflows during T1. During mid light conditions (mid plot) overflow happens just after T1 starts. During high light conditions overflow happens before T1 starts.

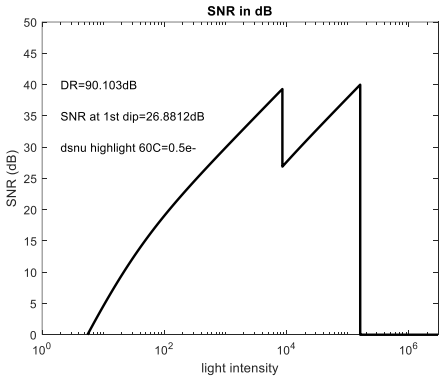
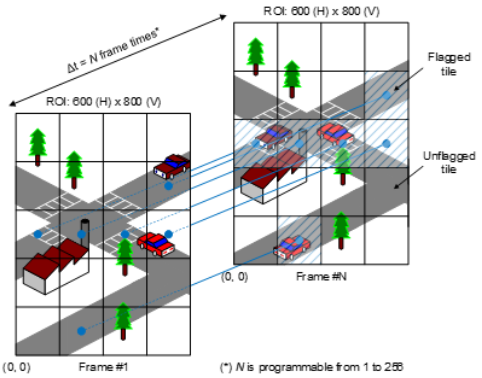


Fig. 4. ~90 dB DR is achieved with T0/T1=16x. Larger DR is possible by trading off with SNR dip. Part of data from the plot is simulated as full char report is not yet available at the moment of the writing of the text.



Parameter	Event Detect. Example	Normal Mode
Frame Rate	1 fps	120 fps
Power	3 mW	48 mW
Resolution	Programmable	600x800

Fig. 5. User programmable event detection mode operating at 1fps. When event is detected, the sensor switches to another user defined mode (e.g. 120fps, 10bit, 0.5MP)

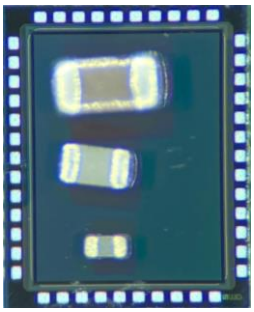


Fig. 6. 2.3mm x 2.8mm CSP version

Parameter	[1]	[2]	**This work**
technology	stacked 45nm-65nm	stacked 45nm-65nm	**stacked 45nm + 40nm**
Pixel pitch (um)	2.2	4	**2.79**
Resolution	640 x 480	1024 x 832	**600 x 800**
Shutter	Global VD	Global VD	**Global VD**
DR (dB)	61	90	**90**
Noise (e-)	2.3 (HCG mode)	4	**5 (LCG mode)**
Power (mW)	139	-	**20mW @10b, 30fps, 60mW @120fps**
Footprint (mm x mm)	2.6 x 2.95	8 x 8	**2.3 x 2.8**
QE 940nm (%)	38	40	**36**

Fig. 7. Comparison table

6 References

[1] Park et al. “A 2.2μm stacked back side illuminated voltage domain global shutter CMOS image sensor”, IEDM19.

[2] Miyauchi et al. “4.0μm Stacked Voltage Mode Global Shutter Pixels with A BSI LOFIC and A PDAF Capability”, IISW21