Fabrication Of Small Pitch InGaAs Photodiodes Using In-Situ Doping And Shallow Mesa Architecture For SWIR Sensing

Jules Tillement[a,b,c], Cyril Cervera[b], Jacques Baylet[b], Christophe Jany[b], François Nardelli[b], Quentin Lalauze[b], Thomas Di Rito[b], Romain Paquet[b], Olivier Saxod[b], Norbert Moussy[b], Olivier Gravrand[b],Virginie Beugin[b], Sylvain Georges[a], Thierry Baron[c], François Roy[a], Frédéric Boeuf[a]

[a] STMicroelectronics, 850 rue Jean Monnet, Crolles, 38926, France – email: jules.tillement@st.com

[b] Minatec Campus, Leti, CEA, Grenoble, 38054, France

[c] Université Grenoble Alpes, CNRS, CEA/LETI Minatec, LTM, Grenoble, 38054, France

***Abstract*—This paper presents the complete design, fabrication, and characterization of a shallow mesa architecture for SWIR sensor. We characterized and demonstrated working photodiodes collecting 1.55 µm photons. The best measured dark current density for a 5 µm pixel pitch reaches 60 nA/cm² at -0.1V and at room temperature. 3 µm pixel pitch photodiodes are also demonstrated with higher dark current density and different strategies to lower it are discussed. The main contributors responsible for the dark current are investigated with perimetric contribution analysis and temperature measurements.**

Keywords—InGaAs, Mesa, SWIR, sensor, photodiode

I. Introduction

The development of short-wave infra-red (SWIR) sensors is led by the growing demand in various fields such as security, automotive, industry or agriculture. In the SWIR range between 1 and 2.5 µm, silicon is transparent ($\lambda_{cut,Si} = 1.1\ \mu m$) which leads to different material alternatives for the photon absorption. The main candidates are quantum films [1], $In_{0.53}Ga_{0.47}As$ [2]–[5] or Ge on Si [6].

$In_{0.53}Ga_{0.47}As$ (cut-off wavelength $\lambda_C = 1.7\ \mu m$) is latticed-matched to InP and has a lower band gap (0.74 eV at room temperature [7]) than Si suitable for SWIR collection. The state-of-the-art for InGaAs imager on Si read-out integrated circuit (ROIC) is a 5 µm pixel pitch with quantum efficiency (QE) greater than 75% at 1.2 µm. The dark current is reported to be as low as 2 nA/cm² at -0.1V and at 23°C [2]. The standard structure for an InGaAs-based SWIR sensor is a thick low doped n-InGaAs absorption layer epitaxied on an InP substrate. The small gap InGaAs layer is protected by an InP cap layer with a larger band gap (E_g = 1.34 eV at 25°C [8]). This way, InP is used as a first passivation layer to prevent the generation of dark current from InGaAs. Indeed, small band gap material such as InGaAs can easily generate dark current at room temperature. It is thus a priority to have the InGaAs absorption layer with the lowest possible defect density at interfaces and in the bulk. The crucial process step is the definition of each pixel by the creation of a p/n junction. Literature reports different alternatives for this purpose such as Zn diffusion [2], [3], [9], Be implantation [10], [11] or shallow mesa-type architecture [12], [13].

Today, the standard process to create the p/n junction is done by Zn diffusion. First, the dielectric is opened on top of the epitaxial stack, then Zn is diffused from this hole and reaches the InGaAs absorption layer to create the p^+-type region. The left-hand side of Fig. 1 shows the schematic cross section of the photodiode after the diffusion process. The isotropic behavior of the diffusion is a clear issue as the target of this work is to reduce the pixel pitch. In addition to this isotropic diffusion, it has been shown that Zn diffuses faster at the InP/InGaAs interface [14] i.e. laterally. Therefore, the diffusion process might be an issue to reduce the pitch because of its acceleration in the lateral direction which might result in a unique p-type region for all the neighboring pixels.

Be implantation could be an interesting solution to overcome the issue of lateral diffusion. Implantation is commonly used in the Si processes to precisely locate the dopants in the structure. The main drawback of the implantation is the introduction of many defects in the structure. It is mandatory to cure as many defects as possible during the anneal to avoid the generation of dark current. Curing defects in InP/InGaAs is not easy and the published dark current is at best in the range of µA/cm². This is a path we study but out of the scope of this paper [11].

The shallow mesa-type architecture could be a solution to reduce the pixel pitch and to target state of the art performance in terms of dark current and QE. Only a few groups report the study of shallow mesa architecture [12], [13], [15]. In this manufacturing method, the structure is doped in-situ during the epitaxy of the stack and the p/n junction definition is done by etching the top p-type layer between the pixels. Unlike other processes for mesa-type device fabrication, our etching step only removes the p-doped region from the top stack. The final schematic structure is presented on the right-hand side of Fig. 1 and referred as shallow mesa architecture. The pixel pitch is thus limited by the lithography and etching tools used in the process. The stack must be carefully designed to allow the collection of photo-carriers generated in the InGaAs absorption layer (color: light blue in Fig. 1). In addition, this alternative is a low thermal budget process which is an asset for the full integration on Si ROIC.

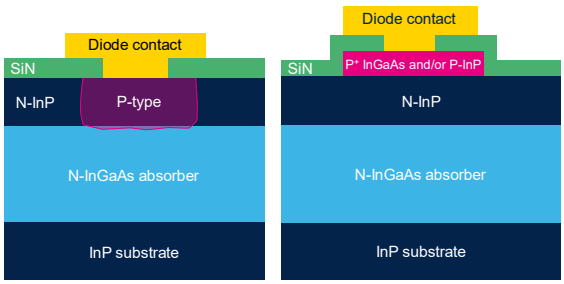


Fig. 1. Schematic cross section of the photodiode after different processes. On the left-hand side, the photodiode after the Zn diffusion or Be implantation processes. On the right-hand side, the photodiode after the shallow mesa-type process

II. Design

The goal of the designed structure is to collect the photo-carriers from the InGaAs absorption layer through the heterojunction created by the n-InGaAs on n-InP. This n-InP cap passivates the small gap layer as explained before, but the heterojunction introduces an unfavorable barrier to the hole collection as it is represented on the band diagram Fig. 2. The challenge is to tune three key parameters to design a structure that collects photogenerated holes at the p-type contact layer (left side of the band diagram on Fig. 2). These parameters are the doping and thickness of the barrier n-InP layer and the doping concentration of the contact layer. It allows to monitor the electric field applied to the device to collect the carriers through the heterojunction.

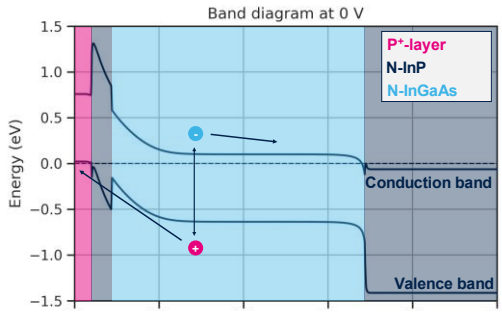


Fig. 2. Band diagram of simulated structure at equilibrium with the photogenerated pair schematicaly represented and their path of collection

The targeted structure should collect the carrier from InGaAs at low reverse bias. The dark blue curve on Fig. 3 shows a well-designed structure where the current from InGaAs is collected at quasi null voltage. If the n-InP barrier layer is too thick (left-hand side in pink) or too doped (right-hand side in pink), it increases the electrostatic barrier and blocks the carrier at low bias. On the other hand, if the n-InP cap is too thin to minimize the electrostatic barrier, it infers process constraints during the p-layer etching process that is difficult to control uniformly on the wafer.

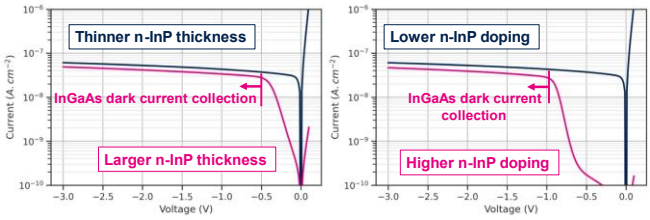


Fig. 3. Effect of barrier thickness and doping on the simulated dark current

Intrinsic material parameters are based on the literature [16], [17] and quality related parameters are fitted on photodiode measurements. This theoretical study allowed us to find a set of doping concentrations and thicknesses parameters that suppresses the barrier for hole collection.

III. Fabrication

The schematic and simplified process of the shallow mesa-type photodiode is represented on Fig. 4. All layers with their final doping and thickness are epitaxied on a 3'' InP substrate. Then, pixel definition is performed by etching the p-type layer. After that, the device is passivated with a dielectric. The final step is the fabrication of both contacts.

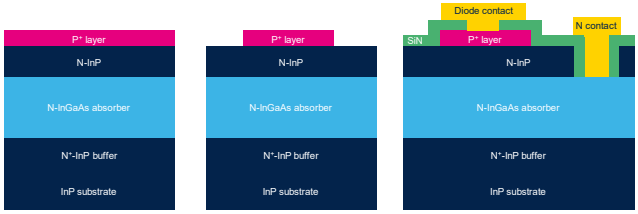


Fig. 4. Simplified schematic process flow of the shallow mesa-type process

This paper investigates the crucial process step of passivation with a first structure using a p-InP layer as the contact layer (referred as processes A1 and A2). Each process has a different nitride deposited with a different gas flow ratio. These dielectrics will have a great impact on the dark current. Then, we will analyze a second structure using a dual layer of p^+-InGaAs on p-InP as the contact layer (referred as process B). The additional p-InGaAs layer in process B allows a better diode contact than p-InP layer. Fig. 5 is a SEM view of the top of the structure. It is clearly visible that the pixels are defined by etching the p contact layer.

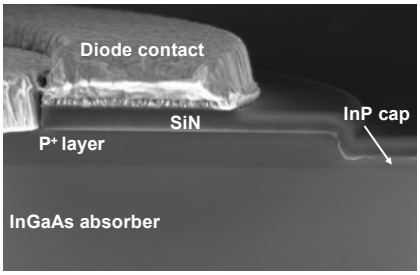


Fig. 5. SEM view after the whole process

IV. Characterization

A. Impact of passivation on dark current

Two different processes are compared here to define the best dielectric for the realization of small pitch photodiode with the lowest dark current possible. If we focus on the dark current measurement presented Fig. 6, we see a different evolution with reverse bias directly related to the different passivation. This difference could indicate different dark current sources. At -0.5V and at room temperature, the dark current for process A1 reaches $5 \cdot 10^{-13}$ A and for process A2, it reaches $2.8 \cdot 10^{-13}$ A.

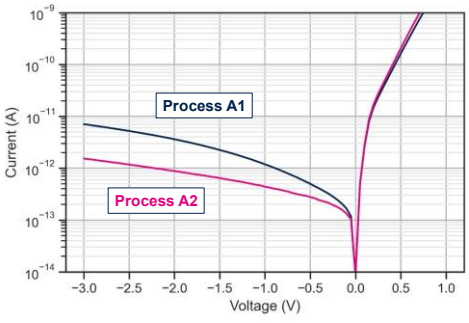


Fig. 6. Dark current measurement on 15 µm pitch in-array photodiodes. The curve is the median of more than 100 diodes measured

Diodes of different sizes ranging from 10 µm to 120 µm were measured to characterize contributions from the bulk (J_b) and from the periphery (J_p) based on the following equation.

$$I_{total} = A * J_b + P * J_P \quad (1)$$

A is the area of the diode defined by its p-layer diameter and P is the perimeter of the diode defined by the perimeter of the p-layer (see cut in Fig. 4). Measured photodiodes have different P/A ratio leading to plot I/A = f(P/A) and discriminate J_b and J_p with a simple linear regression. In our case, Fig. 7 shows the very different value of J_p for the two cases. As our goal is to reduce the pixel pitch, the contribution from the perimeter over the one from bulk is more and more important. Here, the bulk contribution is even for the two processes as $J_b = 2 \cdot 10^{-11} A/cm^2$ in both cases. For the perimetric one, in process A1, $J_P = 8 \cdot 10^{-11} A/cm$ and for process A2, $J_P = 4 \cdot 10^{-13} A/cm$. The perimetric contribution is drastically reduced in process A2 which infers that process A2 is much more suitable for small pixel pitch fabrication.

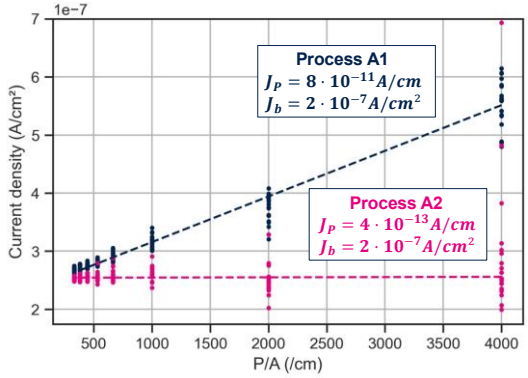
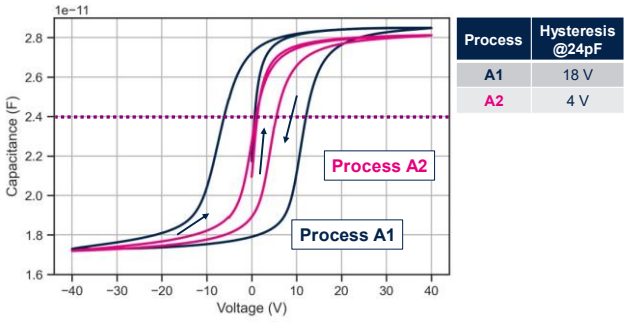


Fig. 7. Perimetric and bulk contribution to the global dark current from measurements performed on diodes with diameter ranging from 10 to 120 µm

Capacitance measurements were also carried out on metal – insulator – semiconductor (MIS) structures to compare the two dielectrics. What is visible on Fig. 8 is the difference between the two hysteresis after the same ramp of polarization. The hysteresis is directly proportional to the charge trapped in the dielectric [18]. Relatively, the passivation of process A2 traps less charges than process A1. As these charges could alter the device's performance, it is thus very important to minimize the effect of trapping in the final device.



Process	Hysteresis @24pF
A1	18 V
A2	4 V

Fig. 8. Capacitance measurement on metal – insulator – semiconductor structure. The MIS structure is a 300µm diameter circle. The measurement starts at 0V then ramp to +40V then goes to -40V and ends at +40V. The hysteresis in V given in the table is computed as the absolute difference between extrema at $2.4 \cdot 10^{-11}$ F.

The deposited nitride in process A2 will now be integrated on the second structure i.e., process B. Performances of this process are investigated in the following part.

B. *Characterization of SWIR photodiodes*

The collection of SWIR photons can be verified at wafer level. In the measurement set-up, a 1.55 µm led is embedded inside the prober and it is possible to switch it on or off. The result of the measurements on bundles of one hundred 3 µm pixel pitch photodiodes are presented Fig. 9 and show the collection of the photons at 0V. This indicates that there is no electrostatic barrier for the carriers generated in the InGaAs layer. These tests demonstrate the fabrication of working InGaAs SWIR photodiodes with such small pitch.

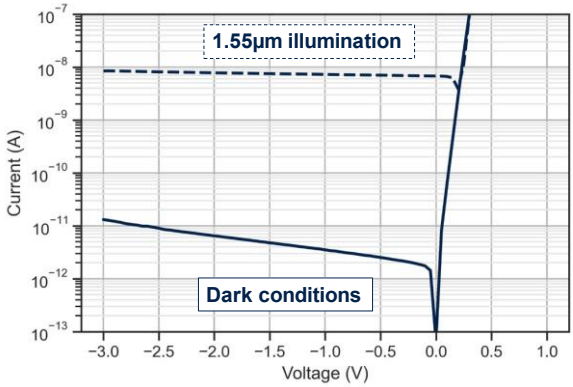


Fig. 9. Median current measurement for bundles of one hundred 3 µm pixel pitch photodiode under dark and SWIR illumination. The solid lines represent the dark current and the dotted lines current under 1.55 µm illumination

The current is measured on bundles of multiple diodes because the dark current from a single diode is too low. Here we measure 1.75pA at -0.1V and at room temperature.

C. *Dark current analysis*

Dark current is a very important figure of merit for photodiodes. Improving it allows to increase the signal over noise ratio which leads to a detection of better quality.

Fig. 9 presents the dark current at room temperature (solid line) for a 3µm pixel pitch. For a deeper understanding of the dark current generating phenomena occurring in the different devices, we performed temperature measurements. The hypothesis done here is that all current coming from InP are negligible as its band gap is around twice the one from InGaAs. When the dark current is limited by Shockley-Read-Hall (SRH) generation-recombination (GR), the current is proportional to $T^{3/2}\exp(E_{g,InGaAs}/2kT)$. If the dark current is limited by the diffusion, the current is proportional to $T^3\exp(E_{g,InGaAs}/kT)$. Dotted lines in Fig. 10 are the evolution of the current with temperature if it is purely limited by diffusion (light blue) or by GR (pink) in the InGaAs absorption layer. These tests were done on bundle of a hundred 5 µm pitch diodes and the results are presented Fig. 10. The evolution of the current with the temperature is presented for two different reverse biases.

For both polarizations and high temperatures, the dark current must be limited by the diffusion in the InGaAs absorption layer whereas for lower temperatures, the limiting dark current phenomenon seems to depend on the polarization. For high reverse bias of -1.5V, the evolution

of the dark current follows the pink dotted line which indicates a GR limitation whereas for low reverse bias, it is a mix of both diffusion and GR.

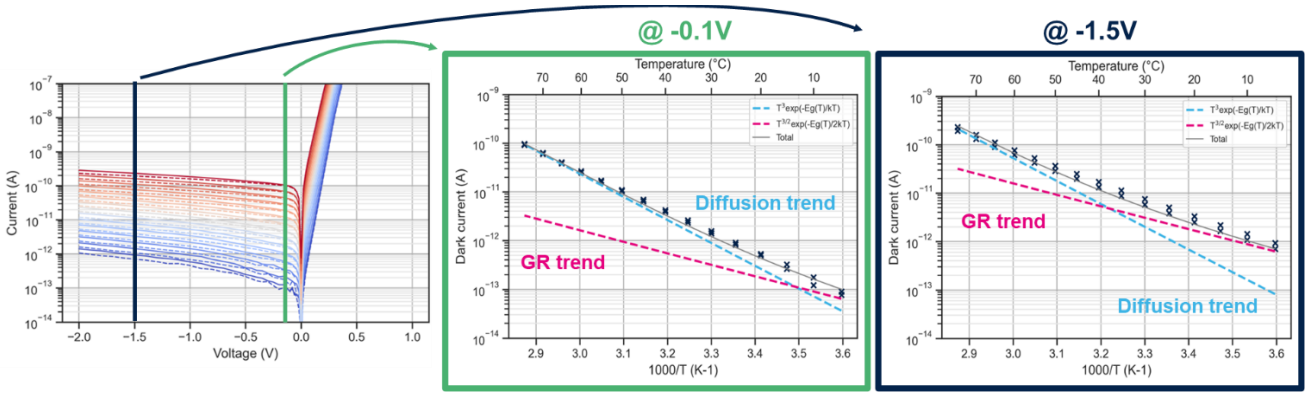


Fig. 10. Temperature measurement on a bundle of one hundred 5 µm pixel pitch diodes. On the right-hand side, we compare the evolution of the measured dark current with the theoretical evolution of the current lilmited by diffusion (light blue dotted line) or generation recombination (pink dotted line) for two polarizations: -0.1V and -1.5V.

As an overall comparison, we gathered the best results measured and compared it to all the different alternatives for the fabrication of InGaAs photodiodes on Fig. 11. Zn diffused diodes in pink is the standard process for InGaAs photodiode fabrication and reaches 2 nA/cm² for the best case at 5 µm pixel pitch [2]. In pink, Be implantation process shows the highest dark current for the fabrication of the photodiodes [11]. Our shallow mesa photodiodes have a lower dark current than the InGaAs mesa/shallow mesa state-of-the-art but around one decade higher than the state-of-the-art for 5 µm pixel pitch. From 15 to 5 µm pixel pitch, our diodes show a flat dark current density of about 60 nA/cm². The measurement for 3 µm pixel pitch is the first published for a pitch that small with a dark current density of 200 nA/cm². This increasing dark current density when the pitch reduces is still under investigation. The impact of charges in the dielectric or traps at the dielectric/cap interface could have great impact on the dark current and is a clear way to improve the dark current density of the small pitch photodiodes.

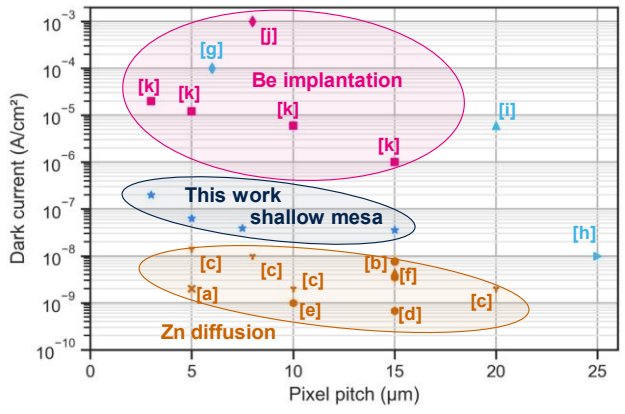


Fig. 11. Comparison of the different alternatives for the fabrication of InGaAs photodiodes. References on the graph give the condition of the measurement if found and the article it comes from: [a] 23°C @-0.1V article: [2] - [b] 30°C @-0.2V article: [3] - [c] 22°C @-0.1V article: [5] - [d] 20°C article: [4] - [e] 20°C article: [19] - [f] RT @-0.3V article: [9] - [g] RT @-1V article: [12] - [h] 22°C @-0.1V article: [15] - [i] RT @-1V article: [20] - [j] @-1V article: [10] - [k] RT @-1V article: [11]

V. Conclusion

We demonstrated InGaAs photodiodes with this very promising innovative shallow mesa-type architecture. We reached dark current as low as 60 nA/cm² at -0.1V at room temperature for 5 µm pixel pitch. For lower pitch down to 3 µm, the dark current density increases to 200 nA/cm² but many improving path have been identified. Further investigations with simulations and capacitive measurements will continue to quantify the impact of the charge in the dielectric and the interface with the top layer. This promising architecture is now under study to be part in a complete integration in a CMOS fab.

References

[1] J. S. Steckel, A. G. Pattantyus-Abraham, E. Josse, E. Mazaleyrat, and K. Rochereau, *Dig. Tech. Pap. - SID Int. Symp.*, 2021

[2] S. Manda *et al.*, *Tech. Dig. - Int. Electron Devices Meet. IEDM*, 2019

[3] A. Rouvié *et al.*, *Infrared Technol. Appl. XLI, SPIE*, 2015

[4] R. Fraenkel *et al.*, *Infrared Technol. Appl. XLIII*, 2017

[5] H. Yuan, M. Meixell, J. Zhang, P. Bey, J. Kimchi, and L. C. Kilmer, *Infrared Technol. Appl. XXXVIII*, 2012

[6] A. Aliane, W. Ludurczak, L. André, and H. Kaya, *Semiconductor Science and Technology* 2020.

[7] S. Paul, J. B. Roy, and P. K. Basu, *J. Appl. Phys.*, 1991

[8] Z. Hang, H. Shen, and F. Pollak, *Solid State Commun*, 1990

[9] M. H. Dolas, O. Atesal, M. D. Caliskan, A. Bek, and E. Ozbay, *Infrared Sensors, Devices, Appl. IX*, 2019

[10] C. L. Chen *et al.*, *IEEE Int. Conf. 3D Syst. Integr. 3DIC, 2009*

[11] J. Tillement *et al.*, *Solid State Devices and Materials*, 2022.

[12] C. L. Chen *et al.*, *Microelectron. Eng.*, 2011

[13] M. H. Dolas, K. Circir, and S. Kocaman, *Image Sens. Technol. Mater. Devices, Syst. Appl. IV*, 2017

[14] A. Djedidi, A. Rouvie, J. Reverchon, M. Pires, N. Chevalier, and D. Mariolle, *Conf. Proc. - Int. Conf. Indium Phosphide Relat. Mater.*, 2012

[15] J. F. Klem, J. K. Kim, M. J. Cich, G. A. Keeler, S. D. Hawkins, and T. R. Fortune, *Appl. Phys. Lett.*, 2009

[16] R. K. Ahrenkiel, R. Ellingson, S. Johnston, and M. Wanlass, *Appl. Phys. Lett.*, 1998

[17] D. Vignaud, J. F. Lampin, E. Lefebvre, M. Zaknoune, and F. Mollot, *Appl. Phys. Lett.*, 2002

[18] D. Schroder, Semiconductor material and device characterization, 2006

[19] R. Fraenkel *et al.*, *Infrared Technology and Applications XLII*, 2016

[20] K. Circir, M. H. Dolas, and S. Kocaman, *Infrared Phys. Technol.* 2019