A Thin-Film Pinned-Photodiode Imager Pixel with Fully Monolithic Fabrication and beyond 1Me- Full Well Capacity

Joo Hyoung Kim[1], Francois Berghmans[1], Abu Bakar Siddik[1,2], Irem Sutcu[1, 2], Isabel Pintor Monroy[1], Jehyeok Yu[1,3], Tristan Weydts[1], Epimitheas Georgitzikis[1], Jubin Kang[1,4], Yannick Baines[1], Yannick Hermans[1], Naresh Chandrasekaran[1], Florian De Roose[1], Griet Uytterhoeven[1], Renaud Puybaret[1], Yunlong Li[1], Itai Lieberman[1], Gauri Karve[1], David Cheyns[1], Jan Genoe[1,2], Paweł E. Malinowski[1], Paul Heremans[1,2], Kris Myny[1,2], Nikolas Papadopoulos[1], and Jiwon Lee[1,5]

[1]imec, Kapeldreef 75, 3001 Leuven, Belgium
[2]KU Leuven, 3001 Leuven, Belgium
[3]SKKU, 16419 Korea
[4]UNIST, 44919 Ulsan, Korea
[5]Hanyang University, 15495 Ansan, Korea

Email: Joo.Hyoung.Kim@imec.be, Tel.: +32 476 804194

Abstract – **Thin-Film Photodiodes (TFPD) monolithically integrated on the Si Read-Out Integrated Circuitry (ROIC), are promising imaging platforms when beyond-silicon optoelectronic properties are required. Although TFPD device performance has improved significantly, the pixel development has been limited in terms of noise characteristics compared to the Si-based image sensors. Here, a thin-film based pinned photodiode (TF-PPD) structure is presented, showing reduced kTC noise and dark current, accompanied with the high conversion gain (CG). Indium-gallium-zinc oxide (IGZO) thin-film transistor and quantum dot photodiode are integrated sequentially on the Si ROIC in a fully monolithic scheme with the introduction of photogate (PG) to achieve PPD operation. This PG brings not only the low noise performance, but also high full well capacity (FWC) coming from the large capacitance of its metal-oxide-semiconductor (MOS). Hence, the FWC of the pixel is boosted up to 1.37 Me- with the 5 μm pixel pitch which is 8.3 times larger than the TFPD junction capacitor can store. This large FWC, along with the inherent low noise characteristics of the TF-PPD, leads to the 3-digit dynamic range (DR) of 100 dB. We expect that this novel 4T pixel architecture can accelerate the deployment of monolithic TFPD imaging technology as it has served for CMOS Image sensors (CIS).**

Monolithically processed Thin-Filme Photodiodes (TFPDs) on the Si ROIC (Read-Out Integrated Circuitry) are attractive imaging platforms when beyond-silicon optoelectronic properties [1, 2]. They can sense photons with energy smaller than the Si bandgap (1.12 eV) or can absorb light more efficiently leading to much reduced active layer thickness [3-7]. Despite these appealing features, the signal-to-noise ratio (SNR) of the TFPD imager pixel output is limited by the kTC noise, high dark current, and low Conversion Gain (CG), compared to the conventional Complementary Metal Oxide Semiconductor (CMOS) Image sensor (CIS). For the Si-based image sensors, a Pinned Photodiode (PPD) pixel architecture was introduced to address issues above [8, 9]. It was designed to single out the kTC noise by pinning the maximum potential of the integration node when it is reset. The photoelectrons are collected in the photodiode during the integration time and these signal charges are transferred to the floating diffusion (FD) to suppress dark current and elevate CG. To implement the Si PPD operation, Thin-Film Pinned Photodiode (TF-PPD) pixel architecture was demonstrated with the typical low-noise readout operation [10]. The TF-PPD structure is realized by inserting a Thin-film transistor (TFT) module based on oxide semiconductor (here, Indium-gallium-zinc oxide: IGZO) between the Si ROIC and the TFPD (Fig. 1). Photogate (PG) fixes the PD reset level, whereas the transfer gate (TG) enables the charge integration and transfer operation. In this paper, a large full well capacity (FWC) exceeding 1 Mega electrons of the proposed pixel (pitch 5 μm) is highlighted, relying on the fact that PG is a MOS capacitor, which serves as an integration node. It is found that the high-k material boosts its FWC as a gate dielectric.

TF-PPD pixel is built in a fully monolithic scheme on a custom-made Si ROIC (Fig. 1(b)). First, Si ROIC is fabricated with the 130 nm CMOS process exposing PG, TG and FD electrodes on the top surface. A 10 nm Al_2O_3 gate dielectric is deposited by atomic layer

deposition followed by sputtering of 12 nm thick IGZO. TG/PG electrodes, Al_2O_3 and IGZO layers constitute a back-gated TFT structure, while the FD connects the TFT to Si ROIC. Colloidal quantum dot (CQD) light-absorbing layer, hole transport layer, and the top transparent contact (ITO: Indium tin oxide) are layered sequentially, with the IGZO TFT channel simultaneously acting as an electron transport layer (ETL) at the bottom. The dark and photocurrent characteristics of the PD test structure are given in Fig. 2(a). IGZO is chosen due to its low leakage, high mobility, and compatibility with the CQD PD as an ETL [10, 11]. The fabricated IGZO TFT shows I-V characteristics with an on/off ratio larger than 105 and a V_{th} of -2 V (Fig. 2(b)).

Various designs of passive TF-PPD pixels, each with more than 500 parallel-connected arrays, are fabricated as described above and then characterized with a custom-made printed circuit board (PCB) probe card (Fig. 2(c), and (d)). The PCB is integrated with an off-the-shelf CTIA (Texas Instruments ACF2101) for the signal charge-to-voltage conversion and the field-programmable gate array (Xilinx Artix-7) for generation of control signals. The output of the CTIA is recorded by a DSOX3014 oscilloscope. The TF-PPD pixels are illuminated by a ThorLabs M530L4 530 nm LED, which is modulated by a ThorLabs DC2200 LED driver. Integration capacitance for the CTIA is increased by adding discrete capacitors after the capacitances are measured by a HM8118 LCR bridge to handle the large FWC of the TF-PPD pixels.

By changing the PG or TG bias, the signal charge generation, and the transfer of it can be controlled (Fig. 3). First, with the fixed TG on bias of -1 V, V_{PG} is swept from -4 V to-1 V, where the FD reset voltage is set to 0 V by CTIA and TG off value is -6.5 V. When V_{PG} is set to -4 V, which is the same bias with V_{anode}, meaning a limited reverse bias of PD, suppressed signal output is found (Fig 3. (a)). As the V_{PG} increases, implying a larger reverse bias within PD, more photocurrent conducts, which is expected from Figure 2(a) (Fig. 3(a)). In other words, by controlling V_{PG}, the sensitivity of the PD can be controlled.

V_{TG} sweep measurements are done with the fixed V_{PG} of -2 V. V_{TG} is scanned from -6.5 V to -1 V, showing the limited signal output when V_{TG} is -6.5 V (Fig. 3(b)). According to the TFT I-V curve given in Fig. 2(b), TG begins to be turned on after -2 V. As V_{TG} increases, more charge transfer becomes available, showing a larger photocurrent for higher V_{TG} (Fig. 3(b)). However, substantial charge transfer is observed before V_{TG} -2 V, which can be explained by the V_{th} nonuniformity within the passive pixel array (data not shown).

PPD concept offers inherent low noise, where the recent PPD-based CIS pixels have a few electrons of read noise level [12, 13]. In addition, the active area of the TF-PPD pixel is de-fined by the PG, thus generated signal charges are collected at the MOS capacitor, rather than the PD junction capacitor [14]. For the proposed pixel architecture, the FWC is described by the capacitor equation of Q=CV, where $C=\varepsilon A/d$ (Q: charge stored at the MOS capacitor, V: PD voltage swing, ε: dielectric permittivity, A: capacitor area, d: gate dielectric thickness). By choosing high-k material as the gate dielectric and thinning the layer, the FWC of the TF-PPD can be boosted. Thanks to this PG structure, FWC is estimated to be up to 1.1 Me- with the 5 μm pixel pitch and 81% fill factor, followed by 1.4 Me- of measured FWC (Table 1, and Fig. 5(b), 1.5 V of PD voltage swing assumed by simulation, ε_r=9 for AlO_x [15, 16]). This is more than 8 times larger than the estimated PD junction capacitance, with the same PD voltage swing and 100% fill factor to avoid underestimation of it. As the pixel pitch increases from 5 μm to 10 μm, the elevation of FWC can be observed, reaching up to 4 Me- for 10 μm pixel with the fill factor of 50%, while 5.6 Me- of FWC is measured for the pi-shaped pixel (fill factor 81% (Table 1, Fig. 4(b), Fig. 5(b)). This observation implies that the generated signal charges are well collected at the MOS capacitor of the TFT channel on the integration node. As a result, charge transfer happens along the IGZO channel, not through the PD, so the charge transport mainly depends on TFT properties rather than TFPD which usually has lower mobility than Si.

In addition, FWC increase by the fill factor is studied, which also shows boosted FWC for a higher fill factor (Fig 5). This confirms that the FWC of the pixel is well described by the MOSCAP of the IGZO channel, meaning that the PG is working as expected.

Finally, the FWC is measured by changing the VPG (Fig. 6). With the larger voltage swing, further increase of FWC is expected, accompanied by more photocurrent with higher

PD reverse bias (Table 2 and Fig. 6). Once again, an increase of FWC can be found for the V_{PG} change, in turn, PD voltage swing (Fig. 6(b)). Here, IGZO potential lower by 0.5 V com-pared to the V_{PG} is assumed for the FWC estimation, due to the work function difference between TiN electrode to IGZO [10, 17].

This beyond-1Me- FWC within 5 µm pixel pitch shows one of the largest signal storage capabilities, showing 55 ke-/µm^2 (Table 2). Though this value is already high enough, it can be even further boosted by having higher-k materials, and by thinning the gate dielectric. Since the TF-PPD active pixel has the same topology as the passive pixel described in this work, FWC estimation can be made as it has been done for the test structure [10]. For the active pixel, FWC is expected to be 621 ke-. Considering the single-digit dark readout noise of the active pixel down to 6.1 e-, dynamic range becomes 100.2 dB, while the 3T pixel shows 82 dB, presenting significant increase in SNR by the introduction of the novel pixel architecture [10, 18].

In this work, a TF-PPD pixel is proposed with the full monolithic scheme from Si ROIC to TFPD, with the insertion of a IGZO TFT module between them. The PPD scheme inherently provides the low noise, by the introduction of PG, FWC is boosted up to 1.4 Me- with the 5 µm pixel pitch. This beyond-megaelectron FWC can be well modeled by the MOS capacitor of PG, demonstrating that generated signal charges at PD are subsequently collected at the TFT channel, and then transferred along this layer. From these results, it is expected that the presented TF-PPD pixel will serve as a high SNR pixel topology for the TFPD category of image sensors.

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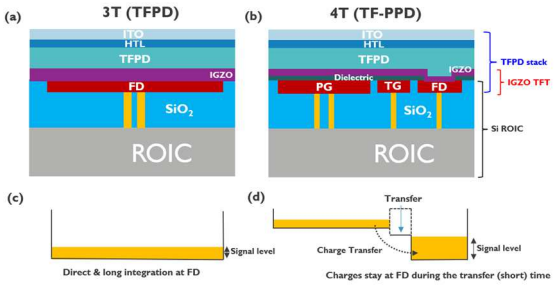

Figure 1. Pixel cross-section for the monolithic TFPD image sensor (a) 3T, and (b) 4T (TF-PPD) structure (TCO: Transparent Conductive Oxide, HTL: Hole Transport Layer, PG: Photogate, TG: Transfer Gate, FD: Floating Diffusion). Electric potential and signal readout configuration for 3T pixel (c), and for 4T pixel (d).

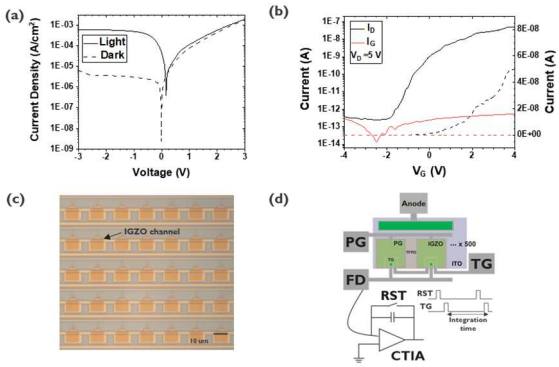

Figure 2. I-V characteristic of QDPD test structure (a), and of IGZO TFT (b), a micrograph of the TF-PPD passive pixel array, and its measurement schematic (d).

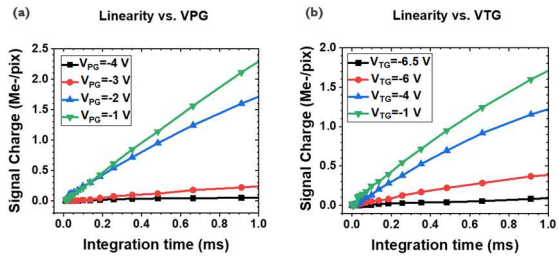

Figure 3. Signal output vs. integration time with different VPG and VTG values with the illumi-nation. Signal curves with the fixed VTG (-1 V), varying VPG (-4 ~ -1 V) (a), the same graphs for the fixed VPG (-2 V), and different VTGs (-6.5~-1 V) (b).

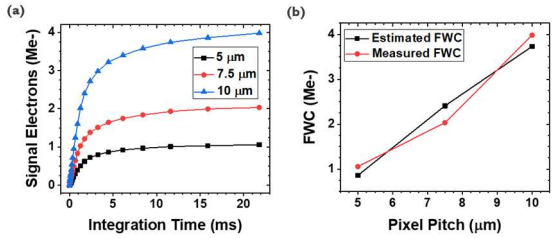

Figure 4. (a) Pixel output vs. integration time for different pixel pitches. (b) FWC comparison between estimation and measurement.

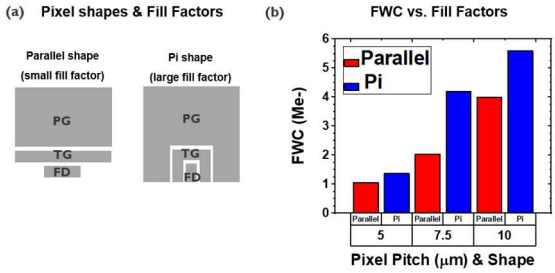

Figure 5. FWC comparison by different pixel fill factors. Pixel schematics for different shapes (a), and FWC by different pixel shapes and pitches (b).

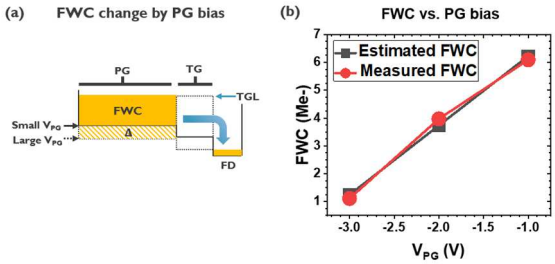

Figure 6. Potential diagram describing FWC increase by the larger VPG (a), and FWC vs. VPG (b).

Table 1. Estimated and measured FWC of TF-PPD pixels.

Pixel Pitch	Fill Factor	Estimated FWC	Measured FWC
5 μm	46%	0.9 Me-	1.1 Me-
	73%	1.4 Me-	1.4 Me-
7.5 μm	57%	2.4 Me-	2.0 Me-
	88%	3.7 Me-	4.2 Me-
10 μm	50%	3.7 Me-	4.0 Me-
	81%	6.1 Me-	5.6 Me-

Table 2. FWC comparison for different pixels

Ref.	FWC (ke-)	Pixel Pitch (μm)	FWC density (ke-/μm^2)
This work	1,367	5	55
[19]	103	6.5	2
[20]	12	1	12
[21]	20	2.8	3
[22]	10	0.6	28
[23]	8	2.4	1
[24]	120	2.8	15
[25]	20	0.64	49
[26]	24,300	16	95