In Depth Characterization and Radiation Testing of a High Performance Fully Passivated Charge Domain CDTI based CCD-on-CMOS Image Sensor

Antoine Salih Alj[1,2,3], Marjorie Morvan[1], Pierre Touron[4], François Roy[4], Stéphane Demiguel[3], Cédric Virmontois[2], Valérian Lalucaa[2], Julien Michelot,[5], Pierre Magnan[1], and Vincent Goiffon[1]
[1]ISAE-SUPAERO, 10 Av. Edouard Belin, Toulouse, France, [2]CNES, 18 Av. Edouard Belin, Toulouse, France
[3]Thales Alenia Space, 5 All. Des Gabians, Cannes, France, [4]STMicroelectronics, 850 Rue Jean Monet, Crolles, France,
[5]Pyxalis, 170 Rue de Chatagnon, Moirans, France
E-mail : antoine.salih-alj@isae-supaero.fr, Tel: +33 (0) 5 61 33 80 39

A new type of charge domain CCD-on-CMOS built with Capacitive Deep Trench Isolation (CDTI) is described and characterized. Dark current, Charge Transfer Inefficiency (CTI) and Full Well Charge (FWC) are investigated through temperature dependence and radiation effects i.e. Total Ionizing Dose (TID) and Displacement Damage Dose (DDD).

I. INTRODUCTION

CMOS charge transfer devices bring many benefits compared to CCD counterparts thanks to advanced state-of-the-art manufacturing processes, high integration level, low power voltages and higher radiation hardness. However, CCDs are still irreplaceable for some key applications that benefit from signal summation on charge domain and multiple charge transfers. For instance, TDI Imaging, Accumulation CCD (ACCD) and Electron Multiplying CCD (EMCCD). Yet, a CCD-on-CMOS device with performances matching pure CCD at high line rate is still to be developed. The purpose of this work is to characterize a promising new CCD-on-CMOS technology based on CDTI transfers [1] and to assess its radiation hardness through TID and DDD tests.

II. DEVICE DESCRIPTION

A CDTI is a vertical MOS gate (Fig. 1) replacing the standard planar gates inherited from CCDs and allowing charge transfer within the Si bulk in a high FWC Buried Channel (BC). The potential well enclosed in-between two facing CDTIs follows a parabolic shape allowing for electrons to be dragged into the center of the finger and avoid interface interactions (Fig. 2). By solving the 1D Poisson equation, one finds the following equation :

$$V(x) = \frac{-N_d q}{2\epsilon}(x^2 - Wx) + V_s \quad (1)$$

Where W is the space in between trenches, N_d is the concentration of donor atoms, q is the elementary charge, ϵ is the dielectric constant in Si and V_s the surface potential. Charge transfer is performed in a 2-phase operation thanks to the design of a barrier (virtual phase) at the beginning of each CDTI gate (Fig. 2-3(a)). By using Transverse CDTI (TCDTI) the width W is reduced, which as can be observed on

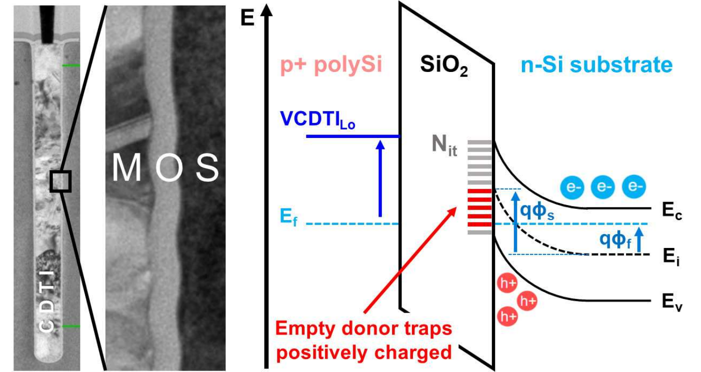

Fig. 1: On the left is a SEM view of a CDTI showing the MOS interface. On the right is a scheme of a MOS junction in strong inversion at equilibrium featuring the surface defect density N_{it}.

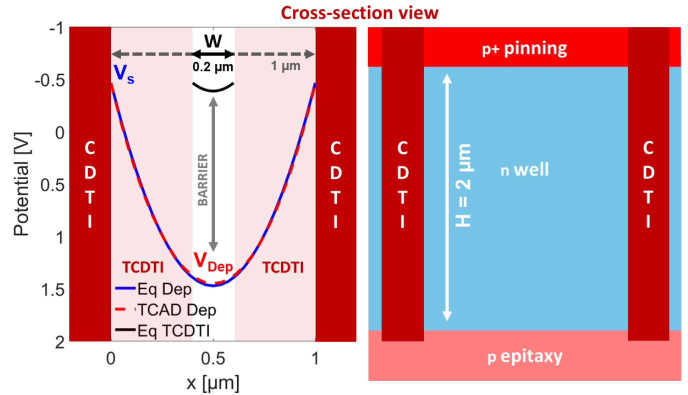

Fig. 2: Analytic and TCAD computation of the parabolic potential well defined in between CDTIs. By reducing the width W (TCDI) a barrier is created. On the right is the doping profile of the finger.

equation (1) effectively reduces the potential of the channel. The potential well depth at the TCDTIs is determined to be 77.5 mV, which corresponds to the difference between the surface potential V_s and the barrier potential V_b. At Low state for storage ($\mathrm{VCDTI_{Lo}} = -1\,\mathrm{V}$), CDTIs are inverted allowing full interface passivation. At High state for transfer ($\mathrm{VCDTI_{Hi}} = 3\,\mathrm{V}$), the passivation is momentarily lost as in-

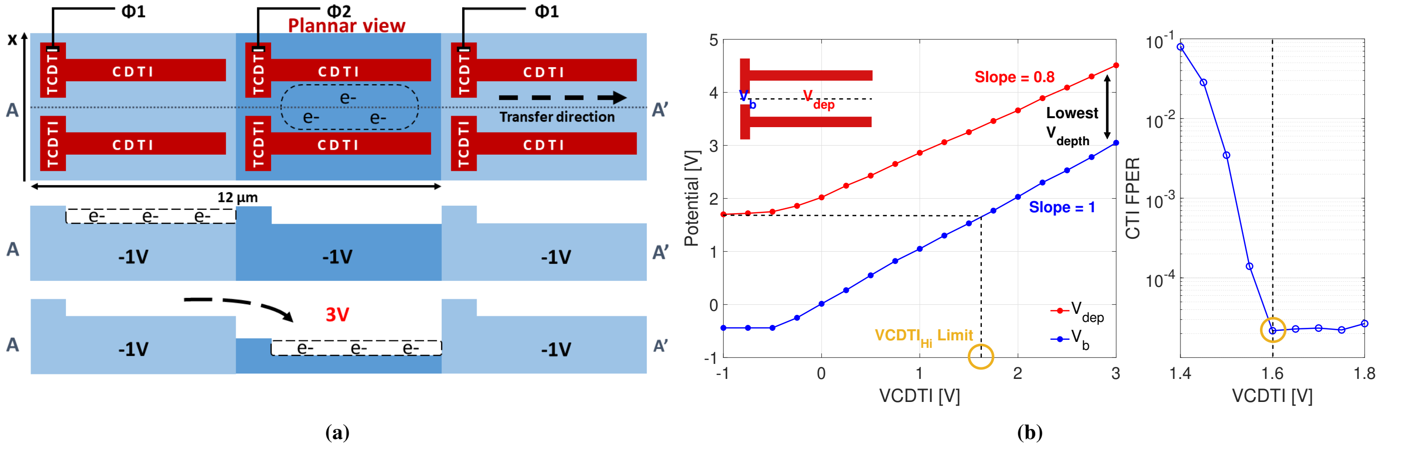

Fig. 3: On (a), the 2Φ transfer operation is sketched with the effect of CDTI bias on the channel potential. On (b), Surface and Depletion potential are plotted with respect to VCDTI. At -1 V the MOS is inverted/passivated hence the potential is pinned. At High State, over the transfer barrier limit, the potential depth is at its lowest. The transfer condition is verified by use of a CTI measurement relative to VCDTI.

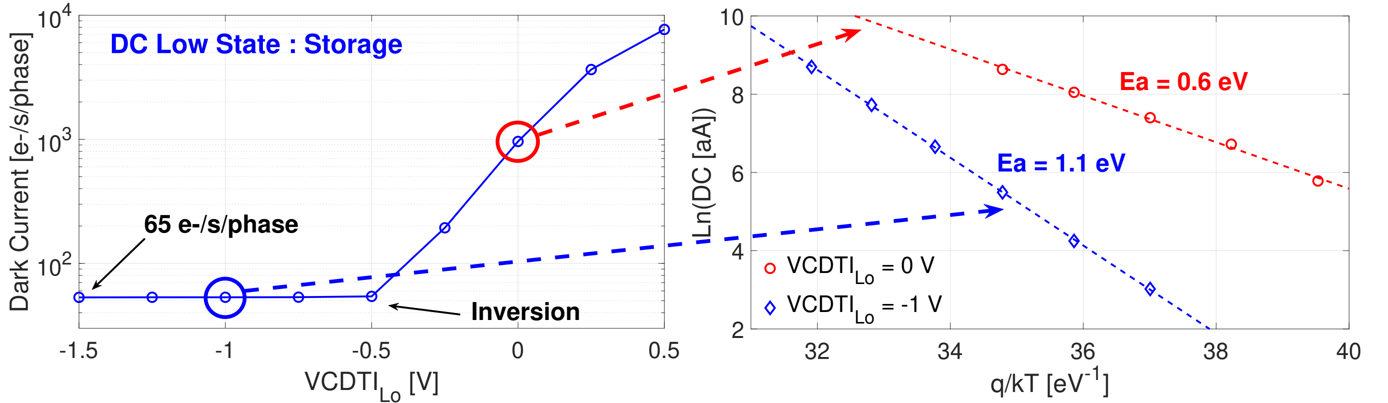

Fig. 4: Dark Current in storage mode vs $VCDTI_{Lo}$. Inversion is reached at -0,5 V and DC cannot be further reduced. The corresponding activation energy appears on an Arrhenius plot. At -1 V, (E_a) matches the silicon bandgap. Hence, diffusion prevails as interface traps are fully passivated. At 0 V, Ea falls at 0.6 eV, indicating a strong contribution from midgap interface states.

terfaces get depleted. The surface and depletion potential with respect to the CDTI bias are shown in Fig. 3(b). A minimum High state bias is required so that the barrier potential gets above the depletion potential of the previous channel, ie. no potential pockets.

III. Experimental Details

The image sensor under study is manufactured by STMicroelectronics. The test structure is composed of a transfer line with an injection stage to emulate signal acquisition. Packaged devices are used to perform measurements in a thermal test chamber and TID exposure under biasing as in fly conditions. The used radiation source for TID is a tungsten tube X-ray source operated with peak energy 70 kV and 12,5 mA resulting in 37 krad(SiO_2)/h of doserate. The 62 MeV protons exposure are carried on grounded chips at UCLouvain. Irradiations and electrical tests are performed at ambient temperature.

IV. Dark Current and Activation Energies

In storage mode, the accumulated hole layer on the interfaces allow the emptying of electrons from most of the donor traps, hence suppressing midgap states (Fig. 4). It is confirmed by the measure of the activation energy E_a, which equals the Si bandgap. In comparison when inversion is lost at 0 V, midgap states contribute heavily and E_a is back at midgap. These activation energies correlate with the temperature dependence of the SRH interface generation rate in both inverted and depleted configurations (when supposing a sharp maximum for midgap states with $E_t = E_i$) [2]:

$$U_{inv} = -\frac{\sigma v_{th} N_{\mathrm{it}} n_i^2 E_g}{p} \qquad U_{dep} = -\frac{\sigma v_{th} n_i N_{\mathrm{it}} \pi kT}{2} \tag{2}$$

With σ the quadratic mean capture cross sections of the defects, v_{th} the thermal velocity, N_{it} the interface defect density, n_i the intrinsic carrier concentration, E_g the Si bandgap, p the hole concentration and kT the thermal energy of the carriers. When neglecting the prefactors temperature dependence, it leads indeed to $U_{inv} \propto e^{E_g/kT}$ and $U_{dep} \propto e^{E_g/2kT}$. When switching in transfer mode, passivation remains if the transfer time is significantly short when compared to the hole emission time constant of interface states [3]. Under

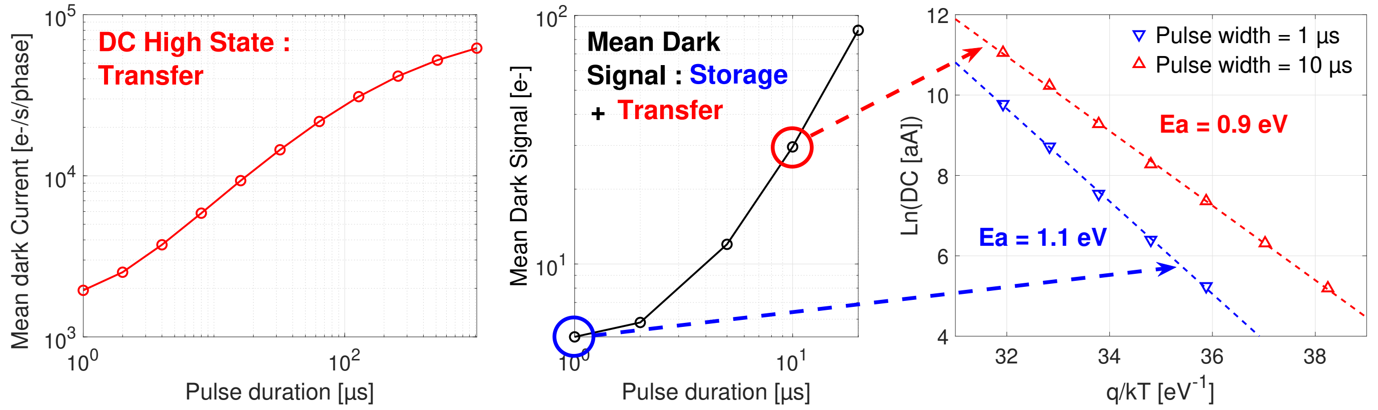

Fig. 5: On the left is the Dark Current at High state (3 V) integrated dynamically for increasing pulse duration. A significant proportion of traps remain occupied by holes for transfer times shorter than the hole emission time constant (≈ 25 ms at 300 K). Hence, the mean DC comprising storage and transfer contributions is greatly reduced for short pulses, with an E_a close to bandgap.

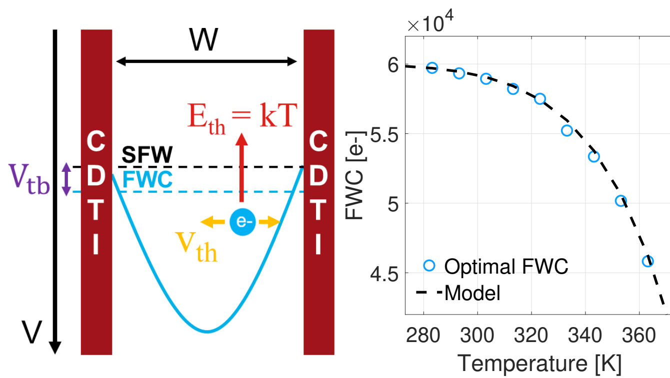

Fig. 6: The thermionic emission is sketched in the context of this device. FWC vs temperature is plotted and compared to equation (3) with t_{PW}=10 µs and V_{tb}=0.46 eV.

similar hypothesis as equation (2), this time constant can be expressed as follow : $\tau_e = (\sigma v_{th} n_i)^{-1}$. Assuming at ambient temperature $\sigma = 10^{-15}\,\mathrm{cm}^{-2}$, $v_{th} = 2.5 \times 10^6\,\mathrm{cm.s}^{-1}$ and $n_i = 1.5 \times 10^{10}\,\mathrm{cm}^{-3}$, it yields $\tau_e = 25\,\mathrm{ms}$. On Fig. 5, the use of much shorter transfer pulses demonstrates the efficiency of the traps deactivation and how much Dark Current can be suppressed. Under nominal charge transfer condition, the mean Dark Signal is reduced using short transfer pulses because (1) integration time at High state is mitigated and (2) interfaces are pseudo-passivated. It enables a Multi-Pinned Phase mode (MPP), essentially suppressing interface state Dark Current [4]. It is confirmed with a measure of the corresponding activation energies in the case of a fully passivated (PW=1 µs) and partially passivated (PW=10 µs) transfer operation. In the first case, $E_a = 1,1\,\mathrm{eV}$ is retrieved, whereas in the later the E_a is diminished by a contribution of midgap interface traps.

V. Temperature Effects

The temperature dependence of the device is investigated through CTI and FWC in prerad conditions to reveal whether native bulk or interface defects plays a significant role in the device performances. For temperature ranging from 260 K to 360 K no bulk defects signature is revealed as the measured EPER CTI at 50% FWC remains within error margin. Considering surface defects, the measure indicates that near to zero interface interactions occur with the charge packet. The calculated emission time constant of midgap states varies from 400 ms to 30 µs with temperature yielding an emission probability during dwell time of 0 to 0.3. In case of a large trap activity, a change in CTI would have been observed. Perhaps higher temperature CTI measurements could reveal small effects. On the other hand, FWC is reduced with increased temperature of operation (Fig 6). At the onset of filling the potential well enclosed in between the CDTIs, the electrons thermal energy kT allow them to hop on to interface traps [5]. Since the thermal energy scales with T, the optimal FWC diminishes by the quantity of electrons able to jump over an effective thermal barrier. It can be modeled considering the electron thermal velocity v_{th}, the average distance to interface $W/2$, the transfer duration t_{PW} and the effective thermal barrier V_{tb}:

$$\mathrm{FWC} = \mathrm{SFW}\left(1 - \frac{2 v_{th} t_{PW}}{W} e^{-\frac{V_{tb}}{kT}}\right) \tag{3}$$

With SFW the Surface Full Well. Such model is compared with the experimental measure on Fig. 6. Considering the discussion above on depletion dark current, it is very likely that this barrier depends also on the proportion of traps that have lost passivation over t_{PW} laps of time.

VI. Radiation Effects

TID tests up to $100\,\mathrm{krad(SiO_2)}$ were performed on biased packaged devices. The resulting voltage shifts on V_s and V_{dep} are plotted in Fig. 7(a). Since interfaces are depleted for positive biases, the resulting interface charge is neutral and the observed shift is only due to trapped charges in the oxide. Flatband shift follows a 4.1 mV/krad trend. In comparison, CTI is probed against signal output for several transfer duration times and irradiation levels using the EPER method (Fig. 7(b)). Three CTI regimes are noticeable as well as the optimal FWC when CTI switched from Buried Channel (BC) to Surface

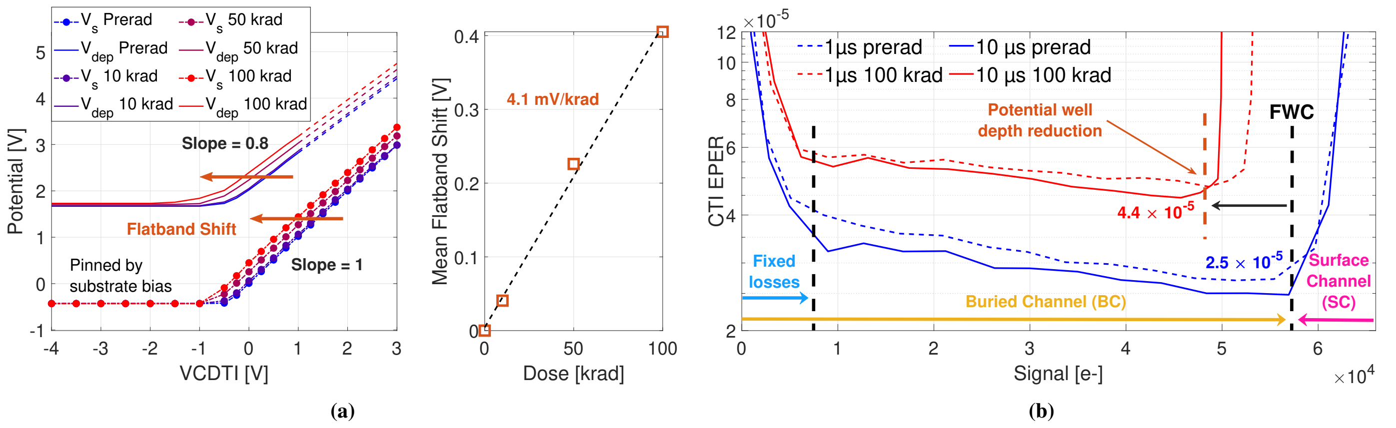

Fig. 7: On (a), potentials vs VCDTI are measured for different irradiation levels, which reveals a flatband shift of 4.1 mV/krad. On (b), Charge Transfer Inefficiency (CTI) is plotted using the EPER method on a reference device and after 100 krad(SiO2) exposure at ambient temperature. The optimal FWC is measured when switching from BC to SC. It is indeed reduced with the TID induced flatband shift.

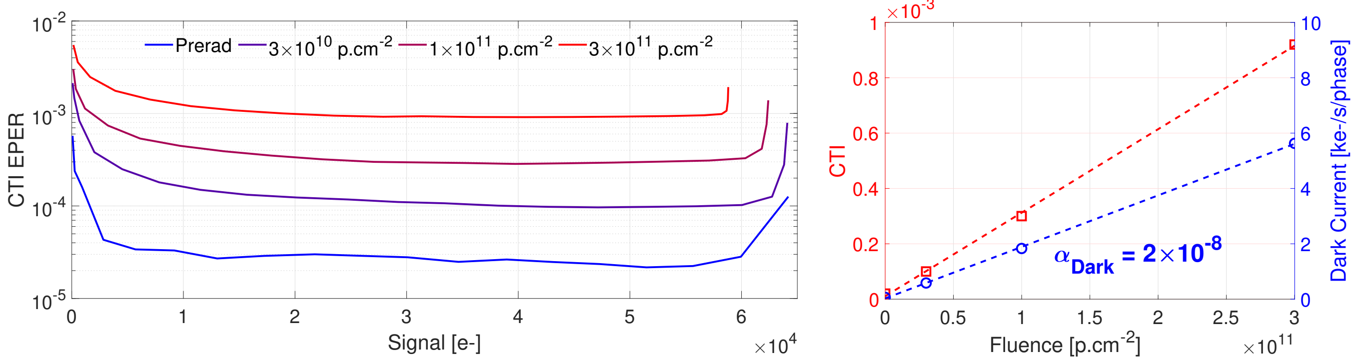

Fig. 8: CTI EPER is plotted for a reference and 3 irradiated devices with 62 MeV protons with fluences of 3×10^{10} p.cm^{-2}, 10^{11} p.cm^{-2} and 3×10^{11} p.cm^{-2}. Mean BC CTI and Dark Current increase are plotted with respect to fluence. One can extract the DC slope to compute the damage factor K_{dark}.

Channel (SC). As expected, FWC is reduced with TID as a consequence of potential well depth cutting induced by trapped charges in the oxide. Results show that transfer time of 1 µs and below is authorized without CTI or FWC trade-off while yielding interface passivation. It seems TID worsens the BC CTI which is believed to be caused by TCDTIs interactions with the charge packet, although further investigations are needed to confirm this hypothesis. Finally, a look at CTI and Dark Current deterioration with 62 MeV protons at different fluences is given in Fig. 8. Charge transfer occurs in a fully depleted BC, only altered by damage in the Si bulk. Proportionality on CTI and Dark Current is found as Displacement Damage Dose (DDD) induces defects in the channel both responsible for generation and trapping. One can extract from this data the damage factor $K_{dark} = \alpha_{dark}/(V_{dep}\mathrm{NIEL}_{62\mathrm{MeV}})$ and find a value of $K_{dark} = 1.85 \times 10^5\ \mathrm{e}^{-}.\mathrm{cm}^{-3}.\mathrm{sec}$ per $\mathrm{MeV.g}^{-1}$ in close agreement with the universal damage factor at $1.9 \pm 0.6 \times 10^5\ \mathrm{e}^{-}.\mathrm{cm}^{-3}.\mathrm{sec}$ per $\mathrm{MeV.g}^{-1}$ [6]. The CTI measure on Fig. 8 also features TID effects since a similar FWC reduction as in Fig. 7 is observed.

VII. Conclusion

The studied device was found promising for high line rate charge domain noiseless binning operations, making it perfectly suitable for high resolution imagery in harsh environment, such as Earth observation using Time Delay Integration (TDI). When compared to the CCD-on-CMOS state of the art using planar gates [7]–[9], the CDTI transfer yields an excellent dynamic range (82 dB) because of improved FWC and fully passivated interfaces. No critical damage was observed within the radiation conditions tested. On the contrary, an opportune TID tolerance is brought by a MPP mode. This study highlights the key requirement of using short transfer times to yield the best performances of this image sensor.

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A 200 Stages Bi-directional 2-Phases CCD-on-CMOS Back Side Illuminated Time Delay Integration Image Sensor

Julien Michelot
Pyxalis
Moirans, France
julien.michelot@pyxalis.com

Jean-Baptiste Mancini
Pyxalis
Moirans, France
jean-baptiste.mancini@pyxalis.com

Mohamed Hadji
Pyxalis
Moirans, France
mohamed.hadji@pyxalis.com

Marie Guillon
Pyxalis
Moirans, France
marie.guillon@pyxalis.com

Paul Monsinjon
Pyxalis
Moirans, France
paul.monsinjon@pyxalis.com

Sophie Caranhac
Pyxalis
Moirans, France
sophie.caranhac@pyxalis.com

Abstract— **In this paper we describe the architecture of a TDI test-chip embedding a 5 µm pitch pixel, 200 stages, bi-directional TDI pixel fabricated in a BSI technology. This pixel makes use of a unique CDTI based transfer register. The obtained performances are presented and compared to other state-of-the-art CCD-on-CMOS published works.**

Keywords— Time delay Integration (TDI), CCD-on-CMOS, Back Side Illumination (BSI), Bi-directional, anti-blooming, Modulation transfer function (MTF) Time delay Integration (TDI), CCD-on-CMOS, Back Side Illumination (BSI), Bi-directional, anti-blooming, Modulation transfer function (MTF)

I. INTRODUCTION

A new type of charge transfer registers, based on capacitive deep trench isolation (CDTI), has emerged recently paving the way to new CCD-on-CMOS time delay integration (TDI) sensors [2]. These types of image sensors are mostly used in spaceborne and airborne earth observation applications were the motion of the scene is highly predictable. By using a CCD-like charge transfer register, integration time of the scrolling scene can be increased and so signal to noise ratio (SNR) of the obtained image is drastically increased with limited loss of modulation transfer function (MTF).

We have been using this type of charge transfer register for some years now using front-side illuminated technologies (FSI), this paper focuses on our latest achievements obtained on a test-chip embedding a small-pitch, 200-stages charge transfer register fabricated in backside illumination (BSI) technology.

II. TEST CHIP ARCHITECTURE

A. General test-chip overview

Presented results come from a CREAPYX test-chip [1], embedding a 5 µm pitch, CCD-on-CMOS pixel, staggered to form a 200 stages TDI charge transfer register. Since the aim of this test chip is only to characterize pixel performances, the number of columns is restricted, nevertheless pixel design is compatible with 1-dimensional stitching rules so that very large linear sensors can be manufactured. Pixel array is composed of 50 columns and is subdivided into 13 sub-matrices of various sizes in order to choose the amount of summed TDI stages. Since often it is not possible to modulate the aperture of the optical system, choosing the number of summed TDI stages is an important feature that can be seen as a derivative mean to control integration time in order to avoid pixel saturation.

Four dedicated phase drivers have been designed in order to allow the test chip to operate in both transfer directions at a maximum line rate of 100 kHz. Those drivers are made to operate the charge transfer registers sub-matrices in both directions so that scene scan direction can be chosen but also in order to drain the charges generated in the unused register stages in the direction opposite to so scene scan.

Transfer registers embed at both ends a specific output stage, allowing for correlated double sampling (CDS) and having charge conversion factor (CVF) value is 50 µV/e-, yielding an excellent readout noise figure of 3.6 e- rms. Output stages have an extra non-photosensitive TDI stage that allows non-synchronous readout of multiple TDI arrays.

The output of our test-chip is purely analog, output signals are converted in external16 bits ADCs (commercially available). The test-chip sequencer is programmed thanks to a serial interface. Fig. 1 shows a simplifiedblock diagram of the test-chip.

Pixel array has been partially covered by a backside opaque tungsten shield with a specific pattern that can be used for in-situ MTF measurements as well as for anti-blooming efficiency measurements. Pixel array can be operated in two different modes, classical TDI or fame transfer. The latter is

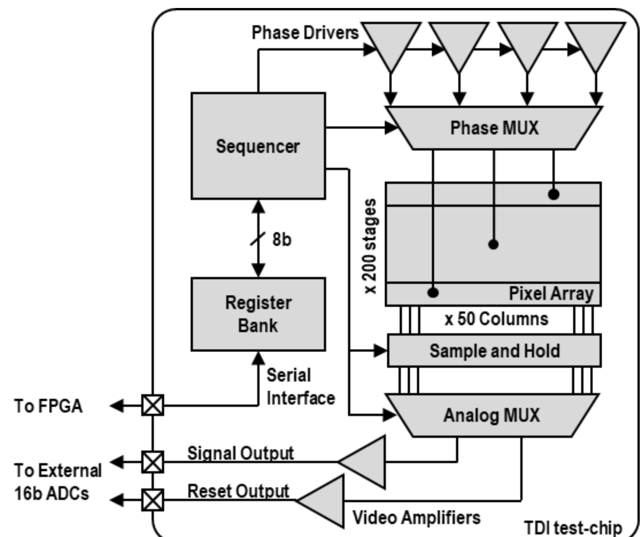


Fig. 1. TDI test-chip block diagram.

mainly used to ease pixel characterization. Fig. 2 shows the layout of the tungsten shield that exhibits slanted edges for MTF measurement purposes and the corresponding image obtained using frame transfer readout.

B. Power concerns

CCD based TDI used to be power-consuming device and the usage of CDTI trenches to mimic CCD behavior was quite troublesome since the capacitance to drive were quite important.

Nevertheless, by choosing an appropriate photodiode doping scheme, we found out that the capacitance operates in a depletion regime most of the time, thus decreasing the apparent capacitance of the trenches and the necessary power to drive them. Accumulation regime is only used to avoid excessive dark current by passivating trenches sidewalls. Going from front side illumination (FSI) to BSI also reduced the CDTI depth, lessening the total power consumption.

Fig. 3 shows a cross-sectional view of a pixel in FSI and in BSI technologies. When going from FSI to BSI, the sensor not only becomes more sensitive to light but power consumption also reduces due to shallower CDTI trenches. There is no noticeable impact on charge transfer efficiency since photodiodes are less deep than CDTI trenches.

Fig. 4 shows a measurement of the CDTI trenches capacitance using a dedicated test structure embedded in the test chip. After reset of the trenches to a negative voltage (V_{reset}), a constant current (I_{cap}) gradually loads the capacitance. Trench capacitance can then be measured thanks to the time derivative of the measured voltage (V_{CDTI}), that is the slope of the obtained curve. One can see that trench capacitance drastically decreases when going from hole accumulation regime ($V_{CDTI} < 0$ V) to depletion regime ($V_{CDTI} > 0$V).

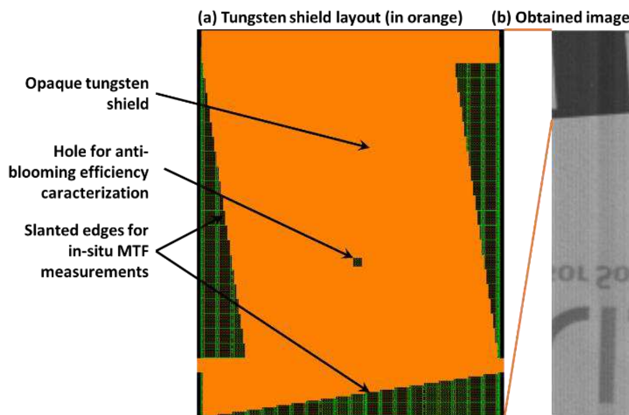


Fig. 2. (a) Backside tungsten shield layout. (b) Obtained image using frame transfer readout.

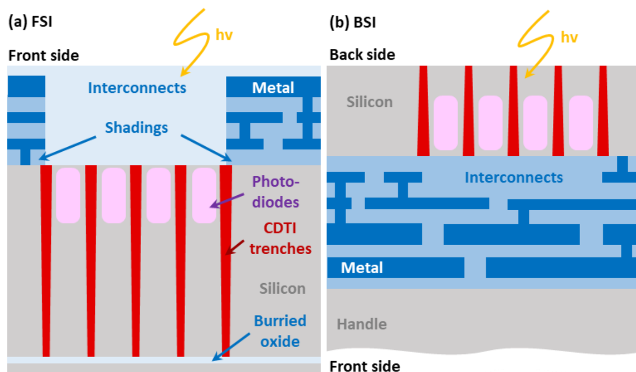


Fig. 3. Cross-sectionnal view of a pixel in FSI (a) and BSI (b).

Fig. 5 shows how CDTI trenches are pulsed during charge transfer. Surface state passivation is lost during the transfer pulse since the CDTI are in depletion regime meanwhile. If the pulse lasts for too long, this can contribute to a dark current increase, so it is preferable to minimized that time length. Since CDTI trenches are less capacitive in BSI technology than in FSI, that time length can be minimized in BSI ($t_{BSI} < t_{FSI}$). Presented charge transfer technology has thus remarkably low dark current and as a consequence low readout noise in darkness.

III. Pixel Design

Pixels are designed thanks to the juxtaposition of bi-directional 2-phases charge transfer registers. Actually, pixel transfer registers are made out of 4 phases (2 are longitudinal and 2 are transverse [2]). By choosing an appropriate pair of phases, charges are transferred in one direction or the other.

Fig. 6 shows an electrostatic potential diagram describing how charges are transferred in a first direction when phases 0 and 1 (Φ_0, Φ_1) and respectively phases 2 and 3 (Φ_2, Φ_3) are operated simultaneously. When phases are paired differently, charges will be transferred in the opposite direction.

A specific anti-blooming device has been designed thanks to TCAD simulations and added to the pixel periphery in order to avoid column blooming when pixel array is over-illuminated. Specific collection devices have been added to the pixel in order to enhance charge collection and thus quantum efficiency.

IV. Results

The designed test chip functionality in TDI mode was validated up to a line rate of 100 kHz, nevertheless

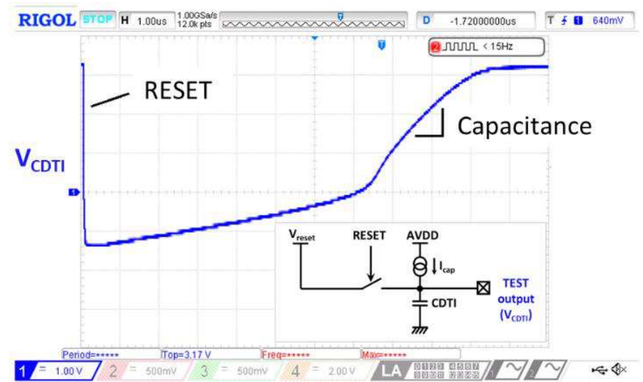


Fig. 4. Measurement of CDTI trenches capacitances.

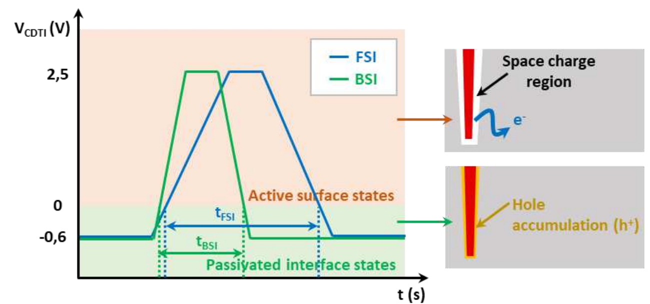


Fig. 5. Trenches sidewall passivation.

performances given here were characterized at a more applicative line rate of 70 kHz.

Fig. 7 shows the obtained mean-variance plot, from which we extract pixel's CVF and linear full well (Qsat) figures. CVF is measured at about 50 µV/e- which yields an outstanding input referred readout noise in darkness of 3.6 e- rms. Linear full well is found at the maximum of the mean-variance at a value of 14.3 ke-. This value is reduced due to the presence of a specific anti-blooming device inside the pixel; no blooming behavior has ever been detected on the detector.

Fig. 8 gives the measured quantum efficiency. Detector shows a peak quantum efficiency of 82% at a wavelength of 530 nm.

Thanks to the use of a BSI technology and reduction of phases pulses duration, our CCD-on-CMOS TDI sensor shows a uniquely low dark current of 3.5 nA/cm² at 60 °C.

Fig. 9 shows how MTF was measured in-situ from previously described backside tungsten light shield pattern. First, pixel data is acquired using frame transfer readout mode

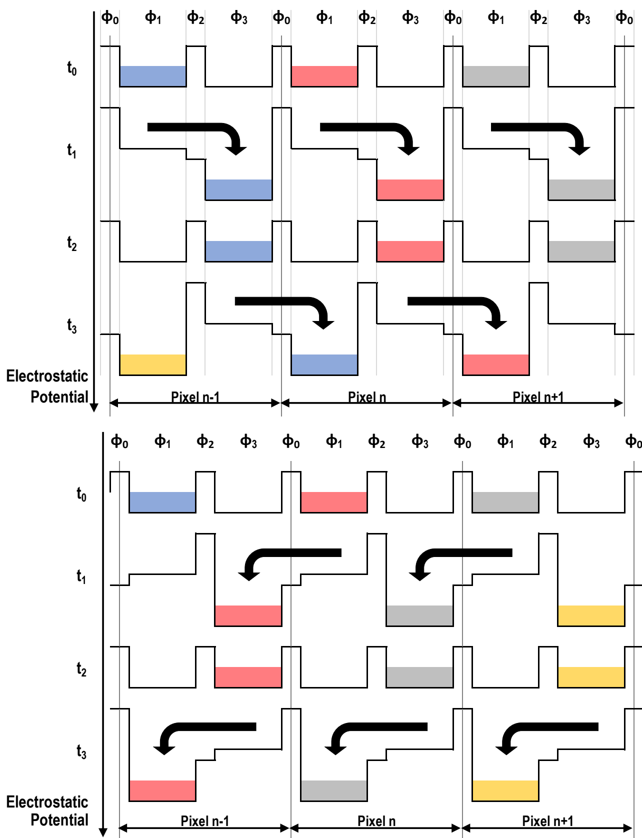


Fig. 6. Electrostatic potential along the register for both transfer directions.

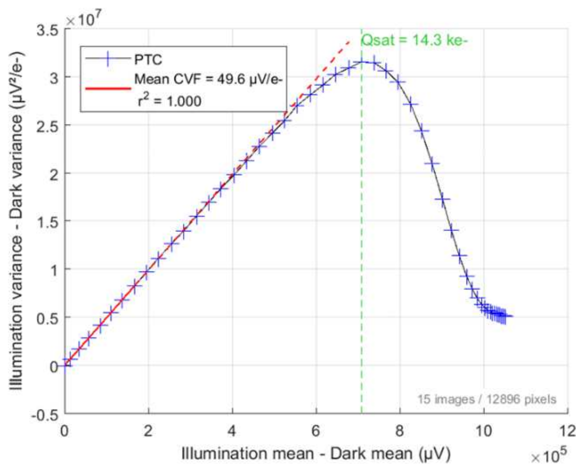


Fig. 7. Mean-variance curve.

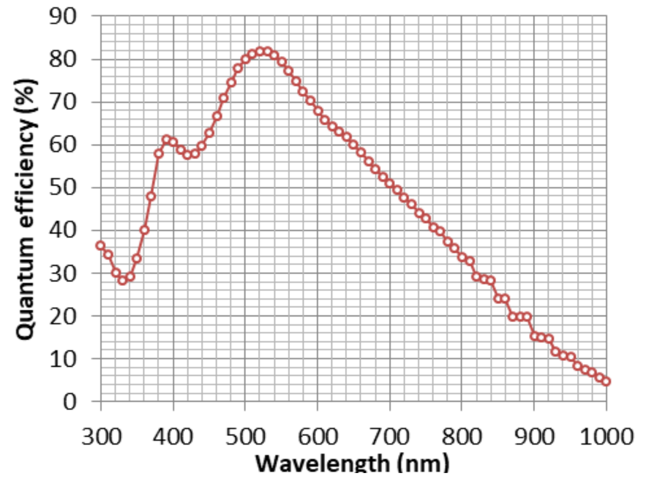
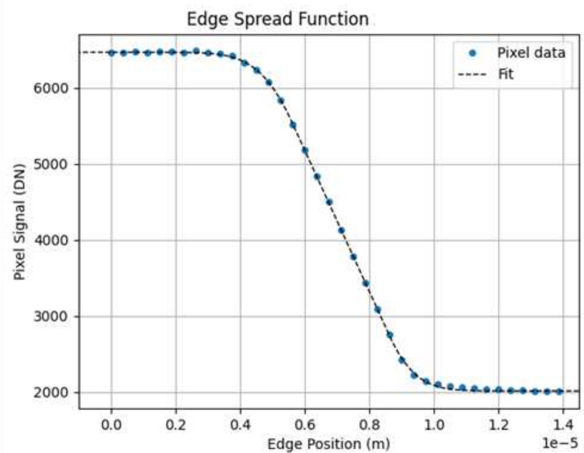


Fig. 8. Measured quantum efficiency.



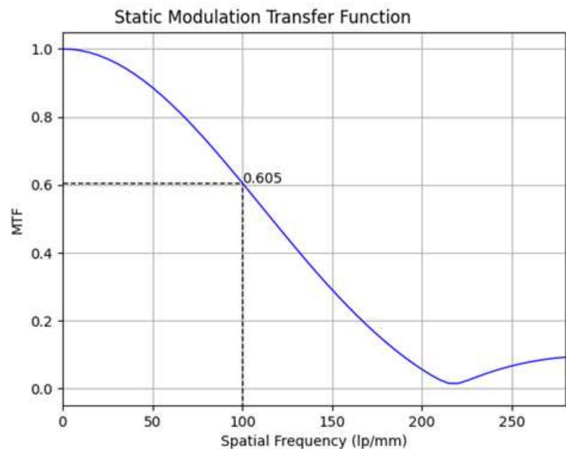


Fig. 9. Edge spead function (top) optained thanks to the tungsten shield and computed MTF curve (bottom).

TABLE I. COMPARATIVE TABLE OF SIMILAR CCD-ON-CMOS IMAGES

	This work	[3]	[4]	[5]	[6]
CCD stages	200	256	192	256	15
Pixel pitch (µm)	5	5.4	3.5	5	5
Pixel architecture	2 phases	4 phases	3 phases	4 phases	4 phases
Row selection	Yes	Yes	Yes	Yes	Yes
Bi-directionnality	Yes	Yes	Yes	Yes	No
Noise in darkness (e- rms)	3.6	10 (HG) 40 (LG)	20	12	12
Linear full well (ke-)	14.3	12.8 (HG) 31.6 (LG)	30	>30	42
CVF (µV/e-)	49.6	62 (HG) 28 (LG)	NA	NA	33
Peak QE (%)	82 (BSI)	89 (BSI)	40.6 (FSI)	53 (FSI)	43
Dark current (nA/cm²)	3.5 (at 60°C)	3.5 (at RT)	3.8 (at 40°C)	3.7 (at 25°C)	NA
Charge transfer inefficiency	< 5.10^{-5}	< 5.10^{-5}	< 5.10^{-4}	< 1.10^{-5}	< 5.10^{-6}
Line rate (kHz)	100	800	58	270	NA
Supply voltage swing (V)	3.1	4.8	NA	NA	NA

and plotted against various positions of this light shield. This data is then fitted in order to obtain a line spread function. Finally, thanks to a Fourier transform, MTF curve is computed. We measured an excellent MTF value of 60.5% at Nyquist frequency. Note that this figure is the static MTF of the pixel and does not include motion blur MTF due to TDI operation, since image was acquired using frame transfer readout mode.

We measured a charge transfer efficiency (CTI) lower than 5.10^{-5}, which is comparable with state-of-the-art CCD-on-CMOS TDI images sensors.

Table I compares our sensor to other similar CCD-on-CMOS published works [3], [4], [5] and [6]. Our work particularly stands out for its low dark current value as well as for its low readout noise. Most papers do not indicate if their TDI image sensor embeds any specific anti-blooming structure. Our TDI is low power thanks to the reduced voltage swing which is applied to the capacitive trenches (-0.6 V to 2.5 V).

ACKNOWLEDGMENTS

We would like to thanks Thales Alenia Space as well as ISAE-Supaero's design and characterization teams for their support to this work.

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A 316MP, 120FPS, High Dynamic Range CMOS Image Sensor for Next Generation Immersive Displays

Abhinav Agarwal[1], Jatin Hansrani[1], Sam Bagwell[1], Oleksandr Rytov[1], Varun Shah[1], Kai Ling Ong[1], Daniel Van Blerkom[1], Jonathan Bergey[1], Neil Kumar[1], Tim Lu[1], Deanan DaSilva[2], Michael Graae[2], and David Dibble[2]

[1]Forza Silicon (Ametek Inc.), Pasadena, California, USA
[2]Madison Square Garden Entertainment, New York City, New York, USA
Corresponding Author: abhinav.agarwal@ametek.com

***Abstract*—We present a 2D-stitched, 316MP, 120FPS, high dynamic range CMOS image sensor with 92 CML output ports operating at a cumulative date rate of 515Gbit/s. The total die size is 9.92cm × 8.31cm and the chip is fabricated in a 4 metal BSI process with an overall power consumption of 23W. A 4.3 μm dual-gain pixel has a high and low conversion gain full well of 6600e- and 41000e- respectively with a total high gain temporal noise of 1.8e- achieving a composite dynamic range of 87dB.**

I. Introduction

Large format next generation immersive displays provide challenging requirements for video capture: the combination of size and resolution of the display that necessitates the detailed image resolution also clearly exposes any deficiencies in the image. This requires a sensor that will create very high resolution imagery while maintaining image quality–low noise, high dynamic range, and minimal shutter/image artifacts.

In this paper, we present a very large 2D-stitched 316MP CMOS image sensor capturing video at 18K × 18K resolution. This rolling shutter sensor operates in either a high frame rate single-gain readout mode or a reduced frame rate HDR mode. The HDR mode leverages the dual-gain capability of the pixel to allow extended dynamic range within a single exposure, mitigating motion artifacts that might appear in other HDR approaches.

II. Readout Architecture

The sensor stitch plan (Figure 1) has a total of 8 vertical and 13 horizontal stitch lines. The top and bottom halves of the pixel array are read out independently, with each half sampling 6 pixel rows at a time. To meet the high frame rate requirement, the sensor timing is pipelined as much as possible with overlapping pixel sampling, ADC conversion and digital readout phases. Figure 5 shows a detailed sensor block diagram with more details of the sensor partitioning.

The sensor readout is divided into repeating units. Stitch blocks 'B' and 'H' consist of six readout units each whereas stitch blocks 'A','C','G','I' contain two readout units each (Figure 5). Every readout unit is responsible for sampling [400 pixel columns × 6 pixel rows] per 'row time'. Each pixel column feeds into a set of 12 single slope ADCs (6 rows * ping/pong), so there are a total of 441,600 ADCs in this design. To fit in the 4.3μm pixel pitch, each pixel column has 4 vertically stacked rows of 3 ADCs arrayed at a 1.4μm pitch.

III. Operating Modes

There are two modes of operation in this sensor, viz single gain and dual gain (HDR) mode. Die size limitations constrained the height of the readout circuitry, making it necessary to use the same ADC stack for both readout modes of the sensor. Detailed sensor timing for the single and dual gain modes is illustrated in Figure 2.

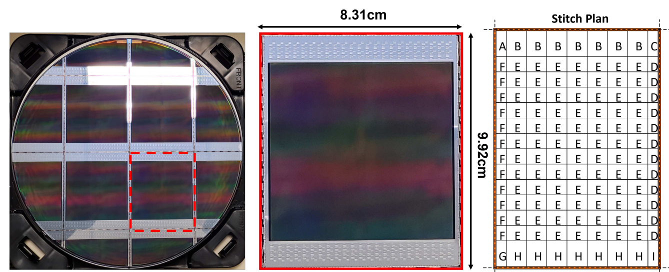

Fig. 1. Sensor on 12-inch wafer (4 die per wafer), die photo and stitch plan

A. *Single Gain Mode@120FPS*

Every pixel is sampled with a fixed conversion gain (either high or low conversion gain) with a standard 4T read timing. The ADC array is operating in a ping-pong type timing, where half the array is sampling while the other half is converting the previous sample.

B. *Dual Gain Mode@60FPS*

To implement a single exposure HDR functionality, we leveraged the existing programmable conversion gain of the pixel, where the high conversion is set by the floating diffusion (FD) capacitance and the low conversion gain achieved by connecting a secondary capacitor in parallel with the FD. The effective extended dynamic range is set by capacity in the low gain mode and the noise of the high gain mode. Each integration is read out in both high and low conversion gains, and the resulting two values are transferred off-chip and processed into a single HDR value capturing more scene contrast.

1) Proposed Dual Gain Timing: Whereas the single-gain mode uses the ADC array in a pipelined ping-pong type operation, the dual-gain mode re-configures the ADC array such that the 'ping' ADCs sample the high gain pixel readout and the 'pong' ADCs sample the low gain pixel readout, and all ADCs convert at once. This effectively doubles the readout time in this mode and thus halves the frame rate. The first operation in this readout is to reset the pixel FD and sample that reset value into both the high-gain and low-gain ADCs. Then there is a first charge transfer in the pixel onto the FD node, and this value is read into the high-gain ADCs.

Finally, the low-gain capacitor is switched into the pixel and another charge transfer is done (combining what was on the FD with any charge left in the photodiode), and this value is read into the low-gain ADCs. All ADCs are then converted simultaneously.

2) Pros and Cons: The approach implemented here provides substantially less dynamic range improvement than the well-known LOFIC approach[1]. However, this approach allows for the simple re-use of the existing single-gain ADC array, whereas typically the low-gain readout from a LOFIC pixel is in the opposite polarity from the high-gain readout, necessitating modifications to the ADC sampling network and ramp. Due to the already extreme density of the ADC array and the readout height limitations, it was not possible to support a LOFIC type readout in addition to the high-frame rate single gain readout. This approach also obviated concerns about overflow path control and process tuning to better achieve first silicon success.

IV. Challenges and Solutions

We present some of the key challenges in designing this large footprint CIS chip along with our proposed solutions.

A. ADC Electrical Crosstalk

Due to the vertical stacked arrangement of ADCs, the outputs of the top ADCs and pixel output lines travel the full height of the ADC column. The ADC layout is done at a small pitch of 1.4μm with limited metal layers for shielding. This results in an unavoidable parasitic coupling between the pixel line (victim) and ADC outputs (aggressor) causing electrical crosstalk. In order to mitigate this, we implemented a novel shielding scheme by dynamically configuring the vertical ADC routing and shielding network according to the timing and mode of operation (as a means to reduce crosstalk). The ADC output multiplexing scheme is illustrated in Figure 3.

1) Single Gain Mode: Overlapping sampling and ADC conversion phase (ping-pong timing) results in electrical crosstalk. In a large sensor like this, there can be a significant intensity difference between two six row groups of twelve adjacent rows resulting in ADC crosstalk which is distinctly visible in an image. To mitigate this crosstalk, the outputs of the top two ADCs are multiplexed at the end of the second ADC. This frees up an additional routing line which is used as a shield to reduce crosstalk. The simulated ADC crosstalk improvements as a result of this multiplexing scheme for various scenarios is summarized in Table I.

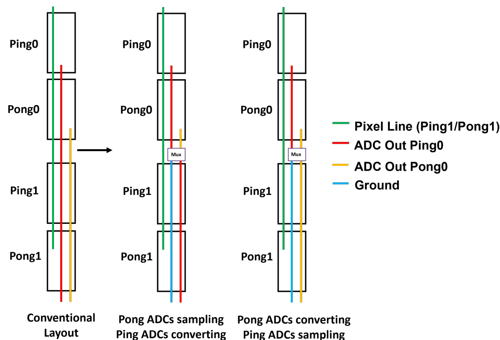

Fig. 3. ADC Output Multiplexing Network

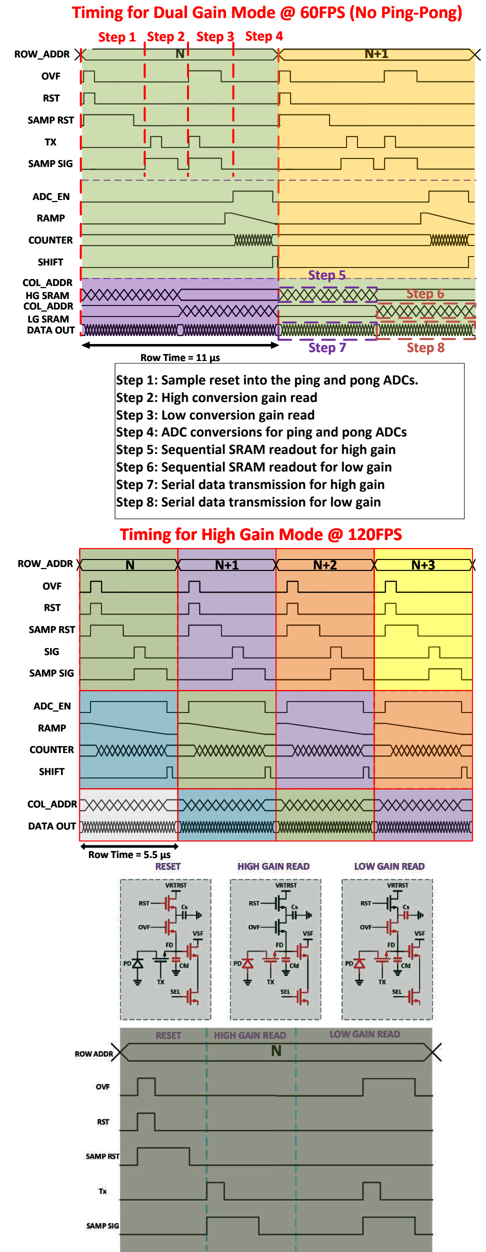

Fig. 2. Sensor Timing for single (high gain) and dual gain operation

2) Dual Gain Mode: Because of the non-overlapping sampling and conversion operations in the dual gain mode, this coupling pathway doesn't cause crosstalk thus allowing usage of individual output lines without any multiplexing.

TABLE I
ADC Crosstalk Improvement (Simulated):Single Gain Mode

Aggressor-Victim	No Dynamic Shield	With Dynamic Shield
Ping0-Pong1(Dark)	4.01DN	0.25DN
Ping1-Pong1(Dark)	2.03DN	0.18DN
Ping0-Ping1(Bright)	-16.5DN	0.04DN
Ping0-Pong1(Bright)	-3.7DN	0.3DN
Ping1-Pong1(Bright)	-1.7DN	0.1DN
Pong0-Ping1(Dark)	0.76DN	0.05DN
Pong0-Ping1(Bright)	-0.72DN	0.01DN

B. High Speed Clock Generation and Distribution

The large amount of data generated by the sensor necessitates a large aggregate data rate – even with 92 output data ports the required data rate is 5.6Gbps (per port DDR), requiring a 2.8GHz clock to be distributed to each of the data ports along the $\approx 8cm$ horizontal chip edges. There are a total of 18 PLLs (one each in stitch blocks 'A','C','G','I','B','H') generating a output clock at 2.8GHz from a 50MHz reference clock provided externally (in each of the stitch blocks). The 2.8GHz PLL output CMOS clock is converted into CML domain (for common mode noise rejection) and distributed to all readout cores within the stitch block through a high speed CML clock distribution network. Two CML buffers in the clock distribution are separated by a readout core pitch of $\approx 1.72mm$ which is comparable to a quarter wavelength of 2.8GHz in silicon. This necessitates a very careful design and optimization of routing traces in between two CML buffers to avoid transmission line artifacts. As a starting point we routed the CML traces in top thick metal having minimum resistance and least coupling capacitance to the substrate. The trace width and separation were carefully fine tuned based on post-layout simulation with RLCK extracted model to minimize attenuation at the operating frequency. Increasing the number of CML buffers to reduce inter-buffer separation has a trade-off with power and device noise. We selected a T-shaped clock distribution and based on simulation results decided with 4 cascaded CML buffer in each left and right directions from center (in stitch block 'B' and 'H').

The output of one CML buffer is AC-coupled into the input of the next stage buffer. This allows us to set a well defined common mode voltage at every CML buffer input pair. It helps to increase robustness by suppressing any systematic or process mismatch causing any common mode imbalance as well as any low frequency noise. One downside of this AC coupling approach is that there is an additional attenuation in the signal path due to the use of MOS capacitors for AC coupling. At the nominal operating frequency, the overall attenuation due to lossy trace and AC coupling stage should be compensated by the large signal gain of the CML buffer.

C. Horizontal Smearing

Horizontal smearing is one of the primary array crosstalk artifacts in any large CIS chip using column parallel readout structures. This artifact occurs when the readout of one portion of the image has a global effect on components that are common to the entire readout. The classical manifestation of this is a very bright region in the image causing a disturbance extending horizontally from the bright region. Significant design effort went into minimizing the absolute value and curvature of this specific artifact.

The ramp generator output is buffered after every two readout units to reduce the ramp propagation delay and minimize the impact of any local ramp kickback causing smearing. Additionally, all the ADC references are re-biased locally in every readout block to create a low impedance net to the center of the array. This helps to locally restrict any reference disturbance caused by aggressor ADCs which further helps to improve horizontal smearing performance. Another important 'global' factor causing smearing is the non-uniformity of pixel and various ADC supplies. Due to sheer size of the sensor and limited routing metal availability in this process, it is challenging to bring power to the pixel and various supply domains of the readout array. At the readout unit level, careful floor planning and layout optimization efforts went into minimizing the IR drop across the pixel array and readout blocks to improve supply uniformity. Among the various supply domains, a larger routing area (lower resistance to pad) was allocated to supplies causing more significant impact on smearing performance based on simulation models. Finally, a comprehensive set of EMIR simulations were performed (Figure 4) for all the supply domains to ensure supply uniformity thus minimizing the impact of smearing.

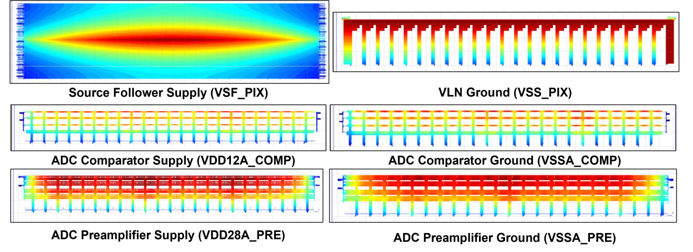

Fig. 4. Generated Thermal Map from Static IR drop Simulation

V. Results and Summary

With the 4.3μm dual conversion gain pixel, we measured a linear full well of 6600e- and 41000e- in high and low conversion gain modes respectively. The measured RMS temporal noise in the high gain mode is 1.8e- giving a composite dynamic range of 87dB. The measured SNR plot for the HDR mode along with the high and low gain transfer functions are shown in Figure 6. Detailed specifications of the CIS sensor are outlined in Table II and a full resolution color image captured at 120FPS (single gain mode) is shown in Figure 7.

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TABLE II
Specification Table

Paramater	Specification
Pixel Pitch	4.3μm
Total Pixels	18400(H)$\times$17712(V)
Active Pixels	18000(H)$\times$17568(V)
Row Time	Single Gain:5.5μs, Dual Gain:11μs
Maximum Frame Rate	Single Gain:120FPS, Dual Gain:60FPS
ADC Resolution	12-bits (2.8GHz count rate)
Linear QSat Full Well	High Gain:6600e-, Low Gain:41000e-
Conversion Gain	High Gain:150μV/e-, Low Gain:19.1μV/e-
Total Temporal Noise	High Gain:1.8e-, Low Gain:13e-
Dynamic Range	87dB
Image Lag	0.45e-
PRNU (ROI: 4000$\times$3000)	0.8%
Dark Current	55e- (measured at 70C)
Total Sensor Power	23W
Die Size	9.92cm $\times$ 8.31cm

Fig. 5. Detailed Block Diagram Showing Sensor Partitioning

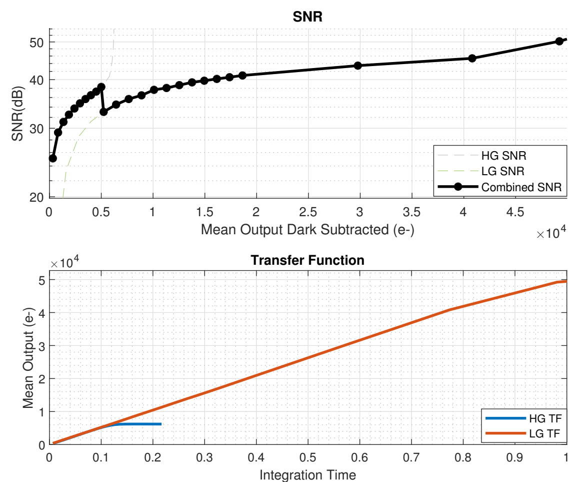


Fig. 6. SNR and Transfer Function in HDR Mode

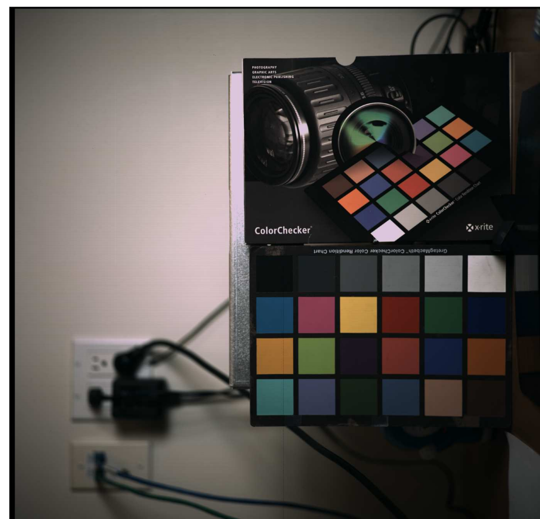


Fig. 7. Full Resolution Color Image Captured in Single Gain Mode at 120FPS

0.5e- rms Read Noise CMOS Image Sensors and Sub-Electron Image Processing for Night Vision Application

Kwang Bo Cho and Brian Johnson
BAE Systems
kwangbo.cho@baesystems.com
1841 Zanker Road, Suite 50, San Jose, CA 95112 USA

***Abstract* - In this paper we present the 0.5e- root mean square (rms) read noise 9.5Mpixel 4K HWK4123 and 1.6Mpixel HWK1411 sensors realized with 65nm CMOS Image Sensor (CIS) technology. These sensors are suitable for very low-light imaging applications such as night vision. We show the sensor architecture and analog signal path used to achieve very low read noise, their performances and comparison, including showing the high near infrared quantum efficiency. Based on these sensors, we show Signal-to Noise Ratio (SNR) measurements and sub-electron images and video processing results.**

1. Introduction

There has been good progress made on image sensor process technology and development over the last several years to achieve low read noise, low dark current, and high quantum efficiency for surveillance, security, and night vision applications [1]. An example is our scientific Complementary Metal-Oxide Semiconductor (sCMOS) 65nm technology with Back Side Illumination (BSI) and improved Near-Infrared Quantum Efficiency (NIR QE). This extends the usable spectrum to 1100nm, delivers extreme low noise, reduces dark current, and boosts QE.

We developed the HWK4123 sensor based on this technology. Using the latest sCMOS BSI technology to enhance NIR QE by increasing the thickness of the epitaxial layer (epi) and applying deeper Deep Trench Isolation (DTI), we developed the HWK1411 to improve low light capability with a larger pixel and even higher NIR QE.

In the first part of this paper, we will present the HWK4123 and HWK1411 sensors, their architectures, measured performances and a comparison. In the second part of this paper, we will discuss recent low light image and video enhancements using these sensors, especially focusing on night vision applications.

2. Low Light Image Sensors – HWK4123 and HWK1411

The HWK4123 incorporates sCMOS BSI technology resulting in a very low-light capable sensor with 4.6µm x 4.6µm pixels, 4K (4108 x 2308) resolution with a market leading 0.5e- rms read noise at 120 Frames Per Second (FPS). In addition, the enhanced NIR QE process leverages the NIR content of nightglow for improved night vision, combining exceptionally low read noise with high quantum efficiency BSI processing enables starlight (<1mLux) imaging capability at 60FPS. The HWK4123 delivers the performance demanded by night vision and high-end surveillance applications with 4K resolution.

Also in the HWK family of products, the HWK1411 incorporates the latest sCMOS BSI technology with enhanced NIR QE into its design. With 1.6M 8µm pixels, this provides an ultra-low light image sensor capable of imaging down to overcast starlight (0.1mLux), meeting recent night vision performance requirements. The HWK1411 has 1440 x 1104 resolution with an 8µm x 8µm pixel and reaches 120FPS at full resolution. The uncompressed data width is 16 bits-per-pixel, which offers up to 96dB high dynamic range for the image. The 4-lane Mobile Industry Processor Interface (MIPI) at 1.5GHz is utilized to simplify integration with industrial ecosystems. It enables night vision applications with the benefits of reduced Size, Weight and Power (SWaP).

The HWK1411 low-light digital image sensor with on-chip 16-bit High Dynamic Range (HDR) processing and dark current compensation with frame memory is designed to capture imagery under overcast starlight (0.1mLux) conditions. It combines,

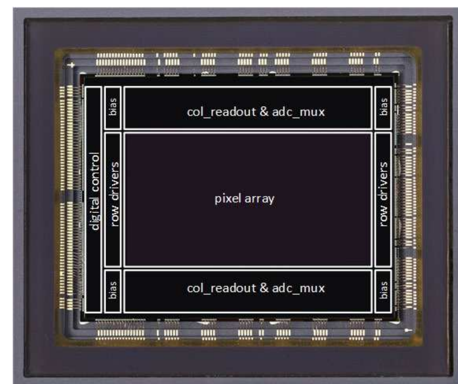
- Large photon-collection array with world-class high NIR quantum efficiency for light sensitivity.
- Ability to see small changes in contrast because of low read noise, 0.5e-, achieved by novel analog design.
- Reduced signal noise due to its low dark current (3e-/s @30C).

This HWK1411 enables the military night vision market's transition into the digital domain because the HWK1411 can replace larger and heavier legacy technology. It provides high-performance imaging capabilities in all light conditions. Its design is optimal for battery-powered systems, unmanned platforms, and intelligence, surveillance and reconnaissance applications. This SWaP optimized design creates a forward-looking design path to next-gen systems that offer technologies such as sensor fusion, augmented reality and artificial intelligence. Enabling these technologies transforms how warfighters perceive the battle space in ultra-low-light conditions.

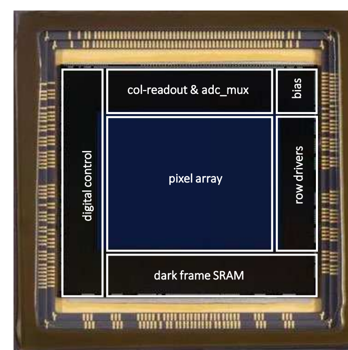
Furthermore, HWK1411 is integrated into a compact Multi-Chip Module (MCM) with a microprocessor, flash memory, power management, a flexible cable for plug-and-play connectivity, and a high-performance glass lens for an optimal field of view.

2.1 Sensor Architecture

Figure 1 shows the HWK4123 and HWK1411 layouts with package. Both HWK4123 and HWK1411 have five-transistor (5T) pixels with pinned photodiodes and use a dual gain column amplifier architecture resulting in 16-bits per pixel to encompass the full HDR. Low-gain and high-gain signal paths provide analog to digital conversions at different gain factors on a pixel by pixel basis.



(a)HWK4123 Layout



(b) HWK1411 Layout

Figure 1. HWK4123 and HWK1411 Layouts with Package.

Figure 2 shows the simplified analog signal path that includes the pixel, column amplifier, gain comparator, variable bandwidth buffer, sample and

hold capacitors, and Analog to Digital Convertor (ADC) module. The column amplifier has two gain modes: a high gain mode of up to 32x and a low gain mode of 1x. The gain comparator is used to automatically drop the gain to unity if the amplifier output exceeds vref_LG, an on-chip programmable reference voltage. The full well capacity is limited by the voltage swing at the floating diffusion node in low gain (1x) mode with a linear full well capacity of 7000e-. The column amplifier bandwidth was carefully adjusted such that the minimum thermal noise contribution from the amplifier is achieved in high gain mode. Further reduction of the bandwidth is available in the variable bandwidth stage. For operation at 120fps, the bandwidth can be set to obtain an average read noise of 0.5e-rms.

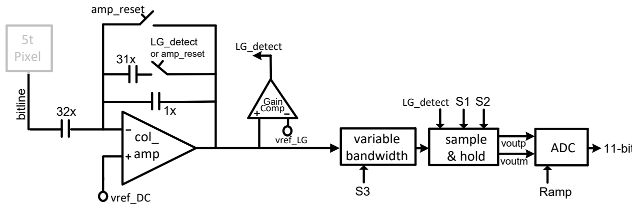


Figure 2. Simplified diagram of the analog signal path.

Figure 3 shows the HDR processing for high gain and low gain merging. By merging either the low-gain signal or the high-gain signal for each pixel with respect to a threshold signal level and post gain adjustment, we maintain both low noise performance at high-gain and large signal at low gain. The result is high native dynamic range in a frame. The HWK4123 merging process is implemented off-chip, while the HWK1411 performs the merging on-chip.

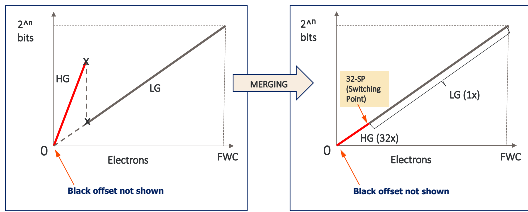


Figure 3. HDR processing for high gain and low gain merging.

2.2 Performance and Measurements

Table 1 shows the relative performance of the HWK4123 and the HWK1411. The key highlight is the 0.5e- rms read noise which enables imaging in darker scenarios. In addition, the enhanced NIR QE process leverages the existing nightglow for improved low-light imaging. By merging high gain (32x) and low gain (1x) outputs, either off-chip for the HWK4123 or on-chip for the HWK1411, they achieve 83dB linear dynamic range to show more detail in high contrast scenes. The pixel's low dark current also enables low noise at longer exposure times for night vision applications.

Table 1. HWK4123 and HWK1411 Performances and Comparison

Parameter	HWK4123	HWK1411
Resolution	9.5Mp (4108 x 2308)	1.6Mp (1440 x 1100)
Pixel (µm)	4.6	8.0
Conversion Gain (µV/e-)	170	170
Read Noise at 32x, 120FPS (e- rms)	0.5	0.5
Linear Full Well Capacity (e-)	7000	7000
Peak QE (%)	87	80
QE (850nm, %)	48	57
QE (940nm, %)	27	39
QE (1060nm, %)	2	6
High Dynamic Range (HDR) (dB)	83	83
Dark Current (e-/sec, at 30C)	2	3
Power Consumption at 120FPS (W)	1.8	0.55

Sensitivity in the NIR domain is key for numerous applications, such as low light, night vision, and biometrics (face recognition for access control, etc.). The major increase of QE in the NIR domain is by increasing the depth of the silicon photodiode pixels. The HWK4123 and HWK1411 have an epi thickness of 2.5 µm and 6.0µm epi respectively. Figure 4 shows their QE.

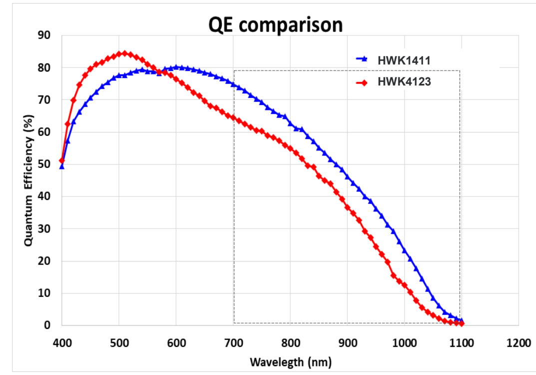


Figure 4. QE comparison on HWK4123 and HWK1411.

3. Test Setup and SNR Measurements

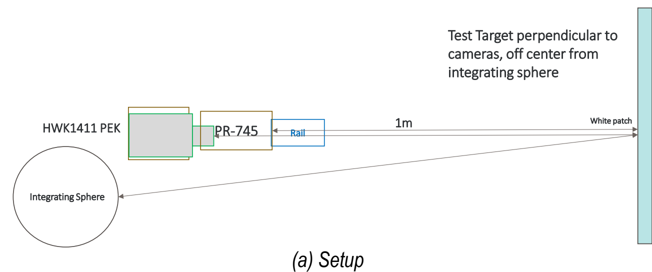
3.1 SNR1-NV Setup and Light Levels

SNR is a good measurement to determine image performance, usually this is done with a target reflectivity of 18% (Gray). The minimum acceptable SNR requirement for security and surveillance applications is typically 1 which occurs when the signal level equals the noise. The light level at which this occurs is referred to as the SNR1. For night vision applications, it is critical to detect objects even when the SNR is below 1. Here we define a new measurement, SNR Night Vision (SNR-NV), where some of the settings for SNR have been changed to better represent night vision applications. A comparison of the settings for SNR-NV and SNR are shown in Table 2 below. The light source for SNR-NV is 2800K to better simulate the spectrum of light from night-glow and the target reflectivity is increased to 95% to better model limits of visibility at very low light levels.

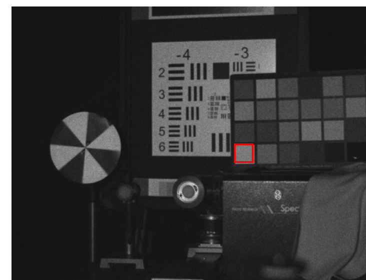
Table 2. SNR-NV and SNR Settings

Parameter	SNR-NV Setting	SNR Setting
Light Source	2800K	3200K
Exposure Time	1/60 second	1/60 second
Lens	F/1.4	F/1.4
IR Cut Filter	Not used	Used
Distance to target	1 Meter	1 Meter
Target Reflectivity	95% (White)	18% (Gray)

Figure 5(a) shows our SNR-NV test setup including the light source, target, light meter (PR-745) and test Image. The light source is an integrating sphere which is illuminated with a 2800K tungsten source. The target is the white patch of an Xrite color checker which has a Lambertian reflectivity of 95%.



(a) Setup



(b) Test Image

Figure 5. SNR-NV Setup and Test Image.

The Table 3 below helps provide an idea of the very low light levels required for night vision applications. We are generally interested in light levels less than 1mlux, which corresponds to a moonless clear night or less.

Table 3. Light Levels at Typical Conditions

Light Level	Condition
1,000.0mlux	Deep Twilight
100.0mlux	Full Moon on a clear night
10.0mlux	Quarter Moon
1.0mlux	Starlight on moonless clear night sky
0.1mlux	Overcast Starlight on moonless overcast night sky

3.2 SNR Measurements

Figure 6 shows the HWK4123 and HWK1411 SNR-NV measurements and comparison at 60FPS with respect to different light levels.

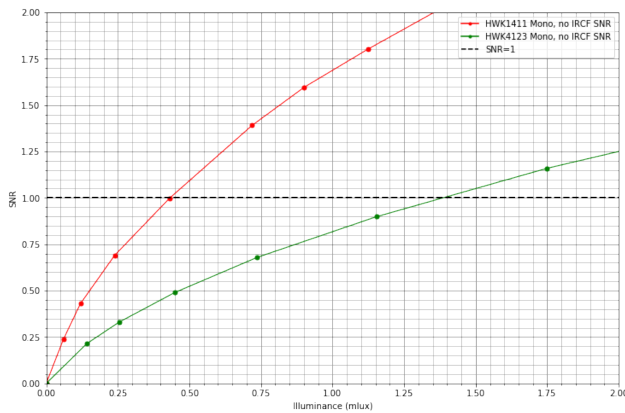


Figure 6. HWK4123 and HWK1411 SNR-NV measurements and comparison at 60FPS.

Figure 7 shows the SNR-NV vs mlux for the HWK1411 Monochrome sensor without an Infrared Cut Filter (IRCF), the HWK1411 Color sensor without IRCF and the HWK1411 Color sensor with IRCF.

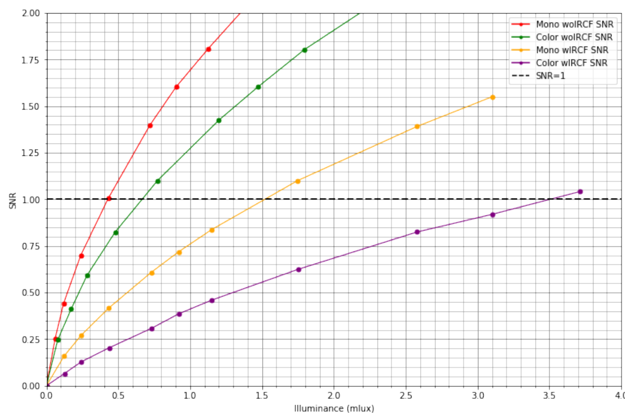


Figure 7. HWK1411 monochrome and color sensors SNR-NV measurement at 60FPS.

4. Low Light Image Processing for Night Vision Applications

In this section, we discuss video processing to improve the quality of low light images and the tradeoffs involved. Since the HWK1411 has better performance at low light, we will use HWK1411 to present improvements.

4.1 Low Light Performance Improvement

In order to get better image quality at the extreme light conditions such as starlight and overcast starlight, we need to increase signal response and reduce noise as much as we can.

To increase signal, first, we need to choose the larger pixel with given resolution and optical format, second, we need to improve QE including NIR, third, we can maximize integration time, increase sensor analog gain, slow frame rate and do pixel summing for signal or binning (averaging) for noise as long as we meet operational requirements. Note that we prefer pixel summing to binning (averaging) to get the bigger signal. Fourth, to increase the amount of light collected, we can choose lower F# lens.

To reduce noise, first, we need to reduce read noise as small as possible at the given gain and frame rate, second, we need to reduce dark current to reduce dark current shot noise. Third, we can apply post image/video processing to reduce the noise using filters like Bilateral, Binomial, Box, Gaussian, etc. Figure 8 shows image comparisons between a raw, unprocessed image and differently binned images.

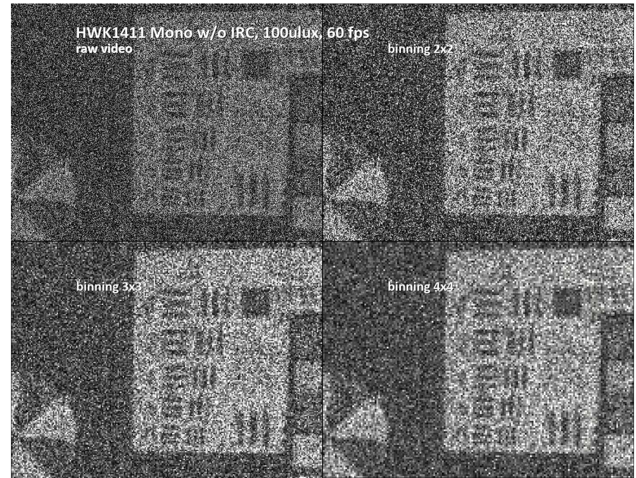


Figure 8. Comparison between raw and binned images.

Figure 9 shows image comparison between a raw image, a 3x3 binned image, a box filtered image and a Gaussian filtered image.

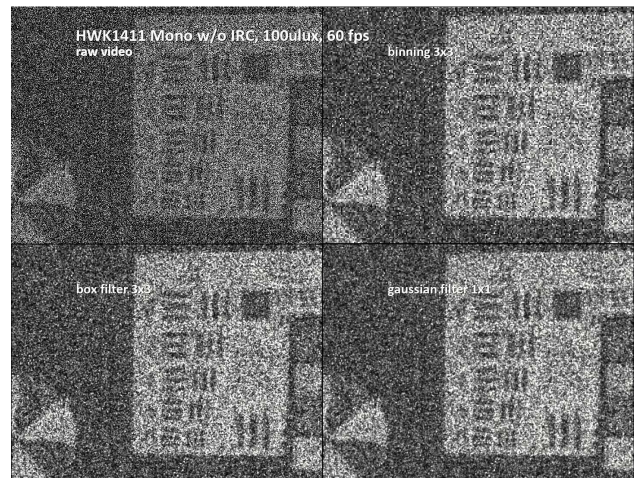


Figure 9. Raw, 3x3 binned, box filtered and Gaussian filtered images.

Table 4 shows the SNR-NV measurements of raw, 3x3 binned, box filtered, and Gaussian filtered images at 100µlux (overcast starlight) and 60FPS. In the raw image at 100µlux, we have less than 0.4e- average signal/pixel and a measured SNR-NV = 0.44. As we can see in Figure 9, we can still recognize object at this sub-electron image.

Table 4. SNR-NV measurement between raw image, 3x3 binning image, box filter and Gaussian filter image captures at 100µlux, 60FPS

At 100µLux Light Condition	SNR-NV
Raw	0.44
Binned	2.45
Box	2.99
Gaussian	4.04

4.2 Sub-Electron Image and Video Processing

An interesting area for study is the sub-electron image region where the photon shot noise is bigger than signal, meaning SNR is always less than 1. During the study, we notice that although we measure an SNR of less

than 1 in a still image, when watching video our eyes see much cleaner video due to our brain's visual processing filtering out the noise. Figure 10 shows a raw capture and averaged images at 100μlux. Based on subjective tests, most people feel that the image quality of an average of 9 frames, is close to the quality of the raw video. This means we perceive an SNR improvement of 3x due to our eye and visual cortex processing the video.

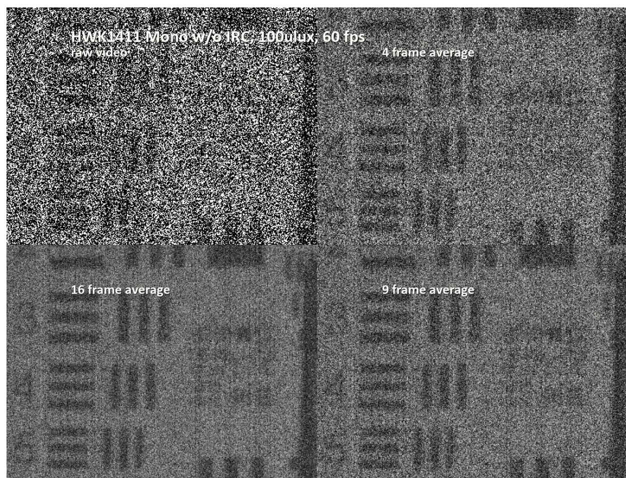


Figure 10. Experiment on raw video vs. averaging images.

This indicates our effective noise in video is 1/3 of measured noise in a still image, so our useful video signal range can be extended further down. Therefore, when we have a 1e- or sub-electron pixel image, even though it is less than SNR1, we may see an acceptable image and better video.

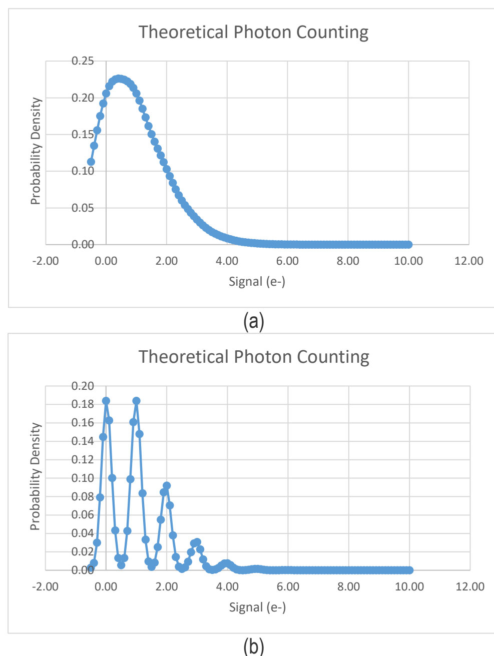


Figure 11. 1e- average signal distribution. (a) With 0.5e- rms noise. (b) With 0.17e- rms noise.

To check average 1e- signal on pixel and display on monitor, Liquid Crystal Display (LCD), Light Emitting Diode (LED) display, or Head Mounted Display (HMD) properly, we would like to know signal distribution. In Figure 11, we show two different signal distributions, (a) a 1e- average signal with 0.5e- rms noise and (b) a 1e- average signal with 0.17e- rms noise. At the 99th percentile, it will be a 4e- signal. A signal with an average 1e- per pixel can be as large as 4e- signal at each frame based on distribution.

Another constraint to consider is a limitation on Conversion Factor (CF). The HWK1411 has a CF of 8DN/e- (Data Numbers/electron), meaning 1 electron is represented by only 8DN. If we want to have more DN/e-, we will need to increase analog gain or ADC bit depth, or digital gain with missing bits.

In addition, we think there are dependencies on noise and display bit depth. We showed that effective noise could be much less than 1/10th of measured noise by doing noise filtering and image/video averaging. For display bit depth, a typical display bit depth for HMD is 8-bit that is 256-level. In order to show 1e- signal on HMD properly, there are on-going research efforts to improve image quality by doing the proper dark frame subtraction & black level control, noise filtering, tone mapping, and even with deep learning [2]. Figure 12 shows tone mapping examples in the HWK1411.

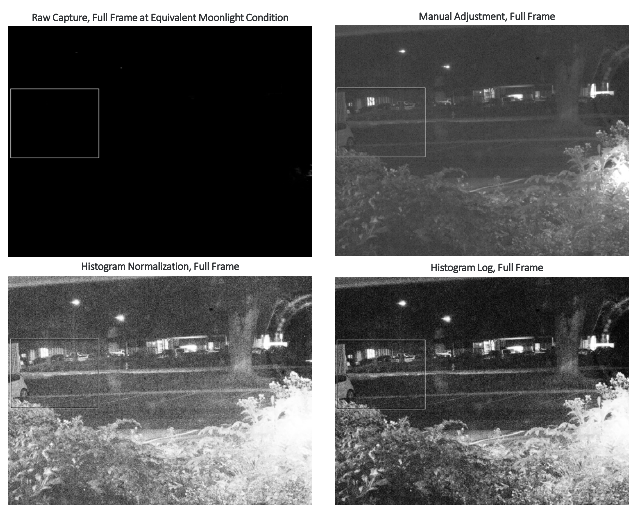


Figure 12. Tone mapping examples.

5. Conclusion

We presented the 9.5Mpixel HWK4123 and the 1.6Mpixel HWK1411 sensors with 0.5e- rms read noise implemented with 65nm sCMOS technology. These sensors are suitable for very low light imaging applications such as night vision. We have shown the sensor architectures, the analog signal path to achieve very low read noise, high near infrared quantum efficiency, and their performance. Based on these sensors, we present SNR measurements and sub-electron image and video processing results. The HWK1411 paves the way to achieve image and video capture down to overcast starlight condition, and enables transition of the night vision market to CMOS image sensors. This SWaP optimized design creates a forward-looking path to next-gen night vision systems to transform image system design at ultra-low-light conditions.

Acknowledgement

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High-speed Time-Delay-Integration (TDI) Imaging with 2-D SPAD arrays

Daniel Van Blerkom, Steve Huang, Barmak Mansoorian
SWIRLabs Corporation, Pasadena, California, USA
dvb@swirlabs.com

Abstract— **We describe the implementation of very high speed TDI imaging using 2-D SPAD arrays. We propose a fast frame read approach to optimize SNR and scalability and investigate its performance using simulation and measurements from a prototype 2-D SPAD sensor.**

I. Introduction

TDI imaging is a technique used when a scene is moving relative to the sensor. Multiple images of the scene are shifted to remove the relative movement and then summed to improve the SNR by effectively increasing the integration time. While the charge-packet accumulation and shifting of CCD technology fits naturally with TDI imaging, TDI sensors have recently been described using CMOS pixels, where the accumulation occurs digitally. However, both CCD and CMOS TDI sensors have speed and noise limitations.

II. Motivation

SPAD based sensors can break the speed bottleneck for TDI, while operating close to the shot noise limit. The combination of precise time resolution and single-photon detection of SPADs makes it a natural candidate for TDI imaging. A digital "charge packet" can be accumulated over multiple lines with no excess noise, unlike a traditional CMOS image sensor, where noise will corrupt each readout. The advantage of applying this Quanta Image Sensor (QIS) approach to TDI is anticipated in [1]; here we examine the implementation of such a sensor with SPAD technology.

Table I compares the performance of recent published TDI sensors with the proposed SPAD TDI sensor. The SPAD TDI can reach line rates that are not possible with a CCD, with an extremely low noise floor. The SPAD TDI readout temporal noise is principally due to the SPAD dark count rate, which is a fraction of an electron at the line rate. The current generation SPAD PDE is lower than the equivalent peak QE of CCD implementations, and the SPAD pitch is larger than CCD TDI pixel sizes, limiting the number of columns that can be implemented in the sensor. However, recent research shows >80% PDP at visible wavelengths with SPAD pitches of 2.5 μm. [2] The power of the SPAD implementation is high due to the large bandwidth requirement of the readout, but it benefits from the continued reduction in digital supply voltages, whereas CCD transfer gates do not share this benefit. The SPAD TDI full-well is determined by the register width allocated to the digital accumulators; this can also scale to larger values with tighter digital processes. In the sensor described here, the full-well can be traded against the line rate, from 255e- at the maximum 12.5 MHz line rate to 4095e- at 780 kHz line rate.

TABLE I. Comparison of TDI Sensors

Parameter	*SPAD TDI*	*[3]*	*[4]*	*[5]*
TDI Stages	256	256	256	256
Columns	512	4096	4096	9072
Pixel Pitch	10 μm	5.4 μm	5 μm	5 μm
Peak QE/PDE	55%	96%	49%	82.4%
Full-well	255 e- / 4,095 e-	23 ke-	30 ke-	15.8 ke-
Noise floor	<< 1 e-	15 e-	12 e-	11.4 e-
Dark current at RT	200 cps = 32 pA/cm^2	2.5 nA/cm^2	3.7 nA/cm^2	4 ke-/sec = 2.5 nA/cm^2
Max Line Rate	12.5 MHz / 780 kHz	1000 kHz	270 kHz	600 kHz
Power	8 W	N/A	2 W	5.5 W

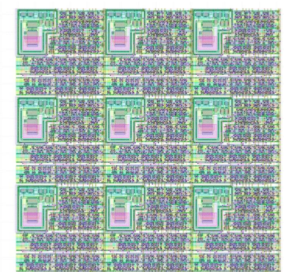


Fig 1. Layout of bottom circuit layer implementing an 8-bit in-pixel accumulator.

The most straight forward digital implementation of a SPAD based TDI imager would be to mimic the operation of the CCD charge packet shifting in the digital domain. This approach is described in [6], where a ripple counter is dedicated to each SPAD to manage the count of detected photons. Fig. 1 shows a 3x3 layout for this approach in the 65nm/40nm ST Microelectronics stacked SPAD process under a 10μm SPAD, with 8 counter bits. As SPAD device pitch decreases with improvements in the technology, the size of the ripple counter must also reduce, limiting the effective full-well and SNR. There is also a timing

overhead to transferring the data and clocking the array, during which photons are not detected, and the simultaneous clocking during the transfer of the ripple counter values leads to a large peak current.

III. SPAD TDI SENSOR

To improve the SNR, we propose to move the TDI accumulators outside of the SPAD array and implement a single bit memory in each SPAD pixel, which can be read and emptied very quickly with a fast frame readout. The sensor architecture is shown in Figure 2. For a 512x256 10µm pitch stacked SPAD array, we simulate operation with a frame rate of 80 nsec per frame. This frame rate can support a TDI line rate of 12.5 MHz. If a lower TDI line rate is needed, then multiple samples can be accumulated for each line, oversampling the array and increasing the SNR. Since the SPAD readout is essentially noiseless, readout noise does not accumulate for multiple reads as it would with a CMOS TDI sensor.

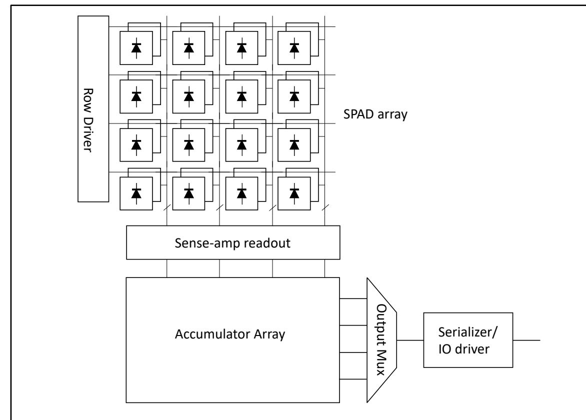


Fig 2. SPAD TDI sensor block diagram.

Each pixel consists of two 1-bit storage nodes for photon detection, as shown in Fig. 3. To avoid interrupting the imaging to reset the detection state, one bit can be read out and reset while the other captures the current frame's SPAD pulse. The entire array is read out in a row-wise fashion, and then the other bit is selected for readout. This ping-pong approach allows for global-shutter and integrate-while-read (IWR) operation. Similar ping-pong approaches have been proposed in, for example, [7] and [8], although not for TDI imaging.

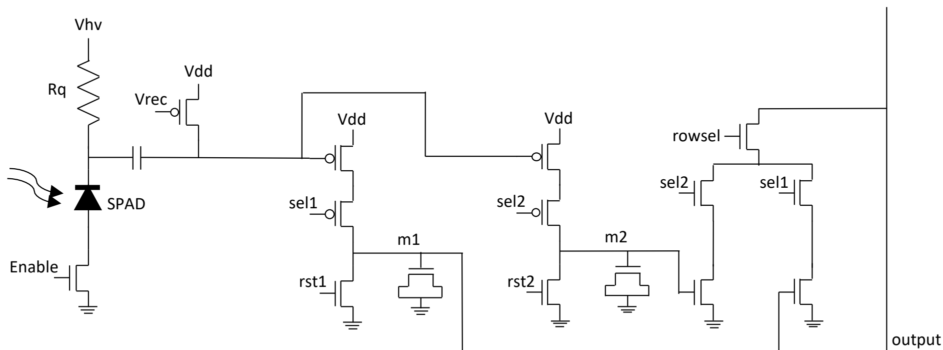


Fig 3. SPAD pixel schematic for fast TDI imaging.

The timing diagram for the ping-pong frame collection is shown in Fig. 4, and the row readout sequence is shown in Fig. 5. Following the row selection for readout, the pixel memory is reset to prepare it to capture the next frame. To support the fast row-select time for a large array, the row driver logic is generated and periodically buffered in the pixel, utilizing the remaining free layout area in each pixel.

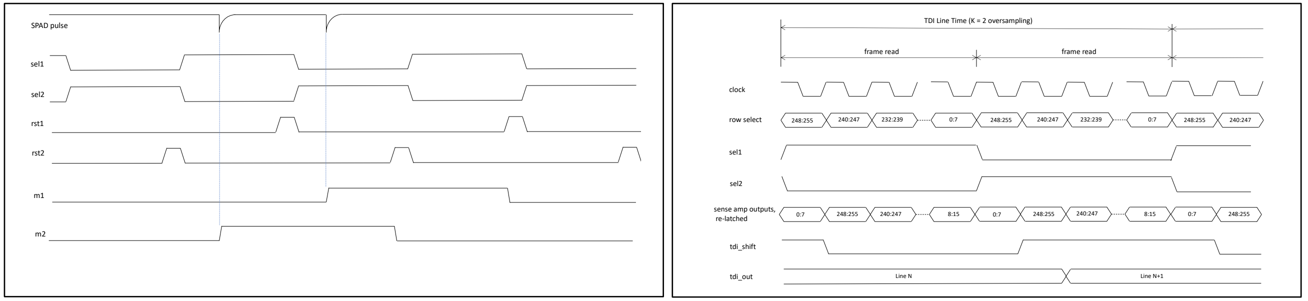


Fig 4 & 5. Pixel timing and row readout timing.

Reading the entire array of memories in one TDI line time is a potential speed and power bottleneck. To reduce the bandwidth requirement, multiple rows are read out in each row time. For a 10µm SPAD pixel pitch, 8 bit-lines per pixel column allows for 8 rows to be read out simultaneously, with a row time of 2.5 nsec. Once the data is read out of the SPAD pixel array, the accumulators are not limited in size by the pixel pitch. For 256 TDI stages, a 12-bit final TDI register can accommodate 16x oversampling of the 1-bit pixel values per TDI stage. As the pixel data is read out of the array, it is added to the appropriate accumulators.

The block diagram and implementation of the accumulator digital logic is shown in Fig. 6. The TDI accumulators are arranged into blocks of 8 adjacent accumulator registers. The readout proceeds from the bottom to the top of the array by passing an enable bit from block to block. The accumulator values are shifted down in the array to make room for the next line, as determined by the oversampling desired. To make the best use of the routing resources, the accumulator blocks are implemented on a two-column pitch, and four columns of accumulators share clock and reset buffering. Clock gating is used to only enable the accumulator logic being addressed, reducing the power requirement significantly. The bit widths of the accumulators are progressively scaled in size to match the increasing full-well of the signal, as the TDI accumulation progresses from the first stage to the last. This means the first accumulator blocks are significantly smaller than the last accumulator blocks.

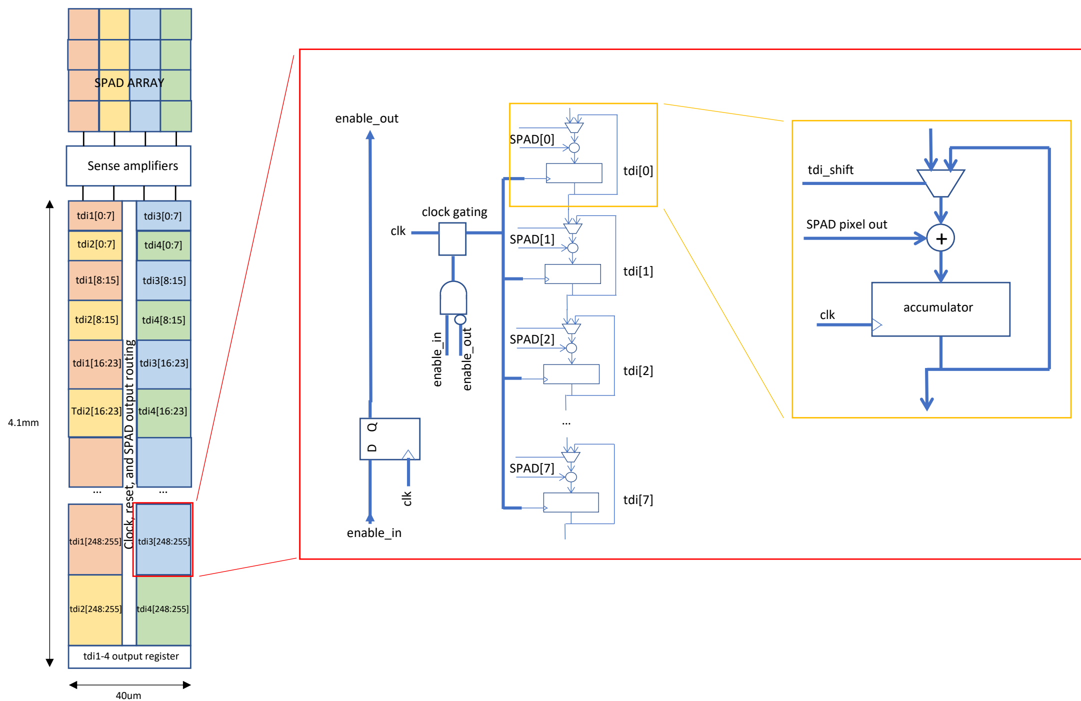


Fig 6. SPAD digital accumulator block implementation.

IV. Power Breakdown

The power consumption of the SPAD TDI sensor can be broken into four main circuit components: the row-selection drivers, the pixel readout and sense-amplifiers, the digital accumulators, and the output serializer and driver. In addition, there is power dissipated by the firing of the SPADs, which is scene dependent. The largest circuit power consumption is due to the digital accumulators, which require 10 mW per column when running at the highest speed. The overall circuit power of the 512x256 sensor is approximately 6 W. If the illumination causes every SPAD to fire for every frame time, the power due to the SPADs themselves is 2 W, giving a total worst-case power of 8 W. At the highest line rate of 12.5 MHz, the sensor outputs an aggregate of 51.2 Gbps of data.

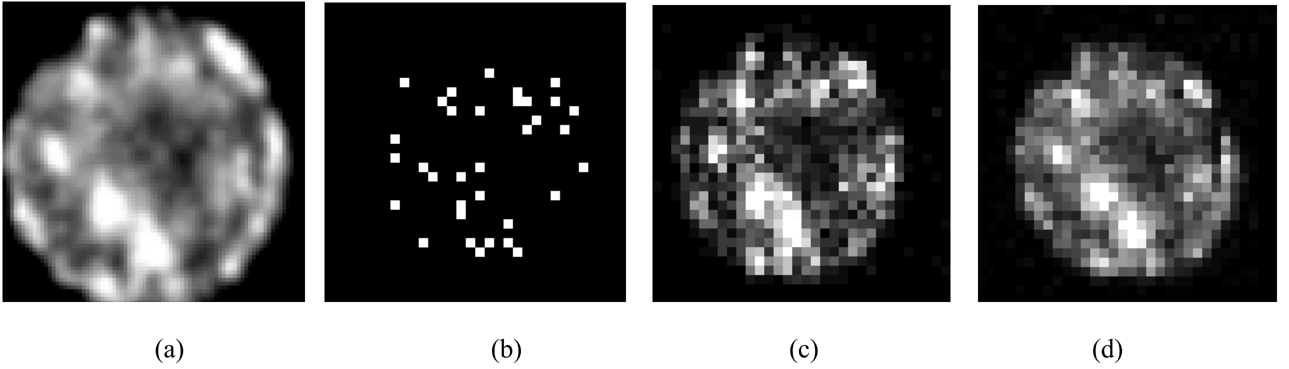
V. APPLICATIONS

Any photons that arrive during the SPAD dead time are missed. This leads to a soft saturation of the final accumulated count as the illumination increases. For the proposed TDI pixel, a similar situation occurs if more than one photon arrives during a frame readout time. Following [5], the final TDI count can then be approximated:

$$S = \frac{\eta\phi N_{TDI} T_{line}}{1+\eta\phi\frac{T_{line}}{M}} \qquad (1)$$

Where T_{line} is the TDI line time, N_{TDI} is the number of TDI stages, ϕ is the photon arrival at the SPAD, η is the SPAD PDP, and M is the oversampling value. This soft saturation effectively extends the dynamic range of the sensor. [1,8]

One potential candidate for high-speed TDI imaging is flow cytometry [11], where there is great interest in imaging the cell morphology and precise location of fluorescence markers on the cell. To show the potential performance of the SPAD TDI approach, we took multiple shifted images of a cell micrograph with the prototype 2-D SPAD sensor and performed the TDI operation off-chip. We illuminated with a flicker-free monitor and captured frames with 300 nsec integration time. Fig. 7 shows the ground truth image, one example captured frame, and the final TDI output. Also shown is an image captured statically (i.e. no TDI shifting) at 30 μsec integration. The cell shape and non-uniformity within the cell are clear in the final TDI output, showing the promise of SPAD TDI sensors.



(a) (b) (c) (d)

Fig 7. Ground-truth image (a), one frame of TDI sequence (b), final TDI output (c), and a statically captured image for comparison.

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