In Depth Characterization and Radiation Testing of a High Performance Fully Passivated Charge Domain CDTI based CCD-on-CMOS Image Sensor

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A new type of charge domain CCD-on-CMOS built with Capacitive Deep Trench Isolation (CDTI) is described and characterized. Dark current, Charge Transfer Inefficiency (CTI) and Full Well Charge (FWC) are investigated through temperature dependence and radiation effects i.e. Total Ionizing Dose (TID) and Displacement Damage Dose (DDD).

I. Introduction

CMOS charge transfer devices bring many benefits compared to CCD counterparts thanks to advanced state-of-the-art manufacturing processes, high integration level, low power voltages and higher radiation hardness. However, CCDs are still irreplaceable for some key applications that benefit from signal summation on charge domain and multiple charge transfers. For instance, TDI Imaging, Accumulation CCD (ACCD) and Electron Multiplying CCD (EMCCD). Yet, a CCD-on-CMOS device with performances matching pure CCD at high line rate is still to be developed. The purpose of this work is to characterize a promising new CCD-on-CMOS technology based on CDTI transfers [1] and to assess its radiation hardness through TID and DDD tests.

II. Device Description

A CDTI is a vertical MOS gate (Fig. 1) replacing the standard planar gates inherited from CCDs and allowing charge transfer within the Si bulk in a high FWC Buried Channel (BC). The potential well enclosed in-between two facing CDTIs follows a parabolic shape allowing for electrons to be dragged into the center of the finger and avoid interface interactions (Fig. 2). By solving the 1D Poisson equation, one finds the following equation :

$$V(x) = \frac{-N_d q}{2\epsilon}(x^2 - Wx) + V_s \tag{1}$$

Where W is the space in between trenches, N_d is the concentration of donor atoms, q is the elementary charge, ϵ is the dielectric constant in Si and V_s the surface potential. Charge transfer is performed in a 2-phase operation thanks to the design of a barrier (virtual phase) at the beginning of each CDTI gate (Fig. 2-3(a)). By using Transverse CDTI (TCDTI) the width W is reduced, which as can be observed on

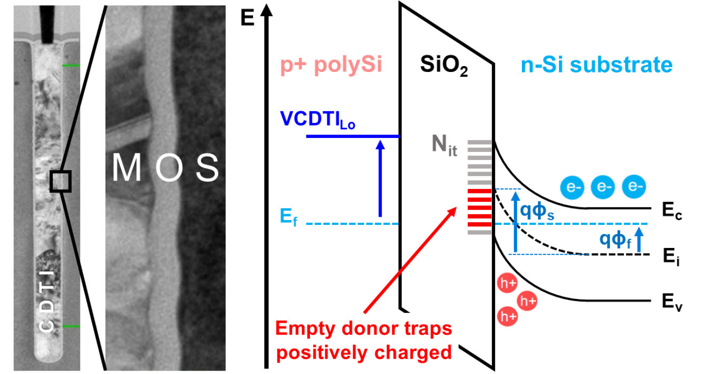

Fig. 1: On the left is a SEM view of a CDTI showing the MOS interface. On the right is a scheme of a MOS junction in strong inversion at equilibrium featuring the surface defect density N_{it}.

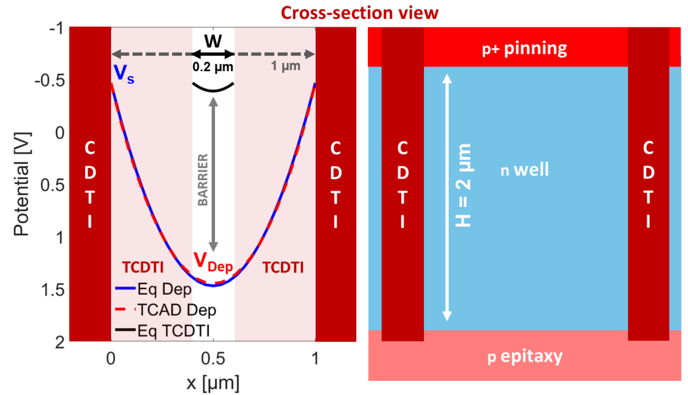

Fig. 2: Analytic and TCAD computation of the parabolic potential well defined in between CDTIs. By reducing the width W (TCDI) a barrier is created. On the right is the doping profile of the finger.

equation (1) effectively reduces the potential of the channel. The potential well depth at the TCDTIs is determined to be 77.5 mV, which corresponds to the difference between the surface potential V_s and the barrier potential V_b. At Low state for storage ($\mathrm{VCDTI_{Lo}} = -1\,\mathrm{V}$), CDTIs are inverted allowing full interface passivation. At High state for transfer ($\mathrm{VCDTI_{Hi}} = 3\,\mathrm{V}$), the passivation is momentarily lost as in-

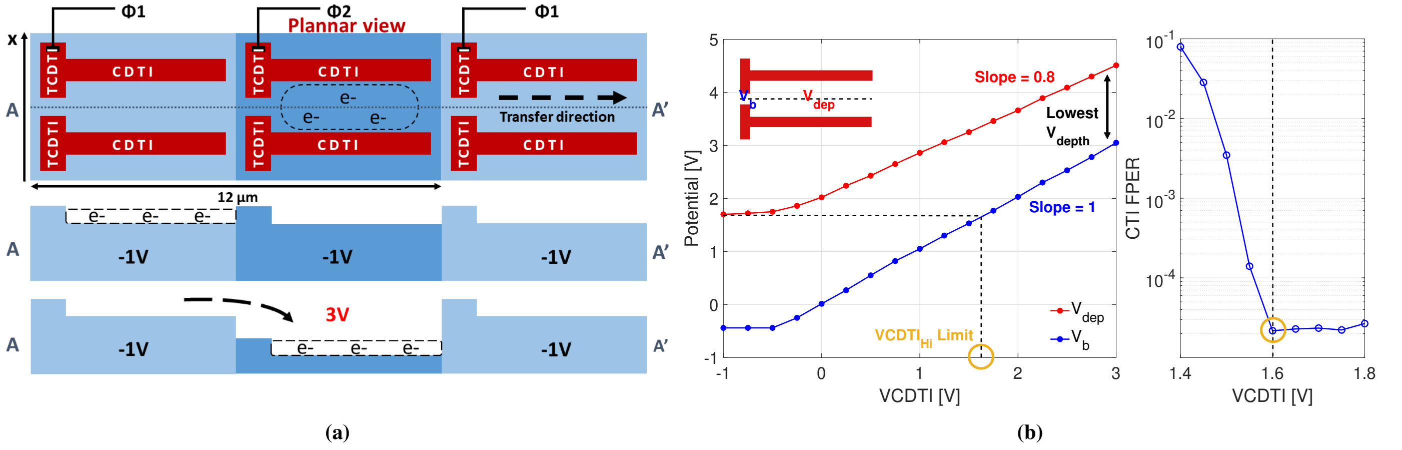

Fig. 3: On (a), the 2Φ transfer operation is sketched with the effect of CDTI bias on the channel potential. On (b), Surface and Depletion potential are plotted with respect to VCDTI. At -1 V the MOS is inverted/passivated hence the potential is pinned. At High State, over the transfer barrier limit, the potential depth is at its lowest. The transfer condition is verified by use of a CTI measurement relative to VCDTI.

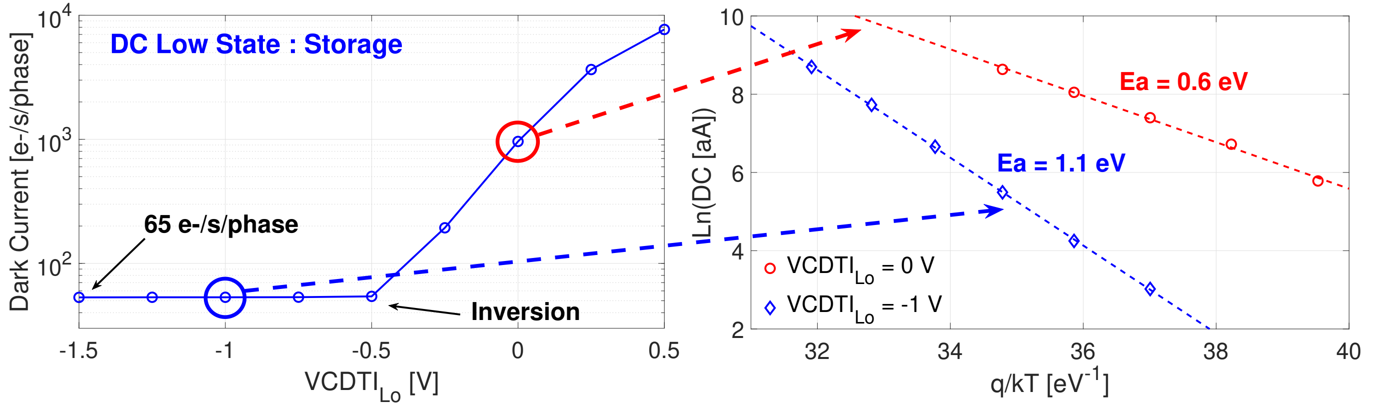

Fig. 4: Dark Current in storage mode vs $\mathrm{VCDTI_{Lo}}$. Inversion is reached at -0,5 V and DC cannot be further reduced. The corresponding activation energy appears on an Arrhenius plot. At -1 V, (E_a) matches the silicon bandgap. Hence, diffusion prevails as interface traps are fully passivated. At 0 V, Ea falls at 0.6 eV, indicating a strong contribution from midgap interface states.

terfaces get depleted. The surface and depletion potential with respect to the CDTI bias are shown in Fig. 3(b). A minimum High state bias is required so that the barrier potential gets above the depletion potential of the previous channel, ie. no potential pockets.

III. Experimental Details

The image sensor under study is manufactured by STMicroelectronics. The test structure is composed of a transfer line with an injection stage to emulate signal acquisition. Packaged devices are used to perform measurements in a thermal test chamber and TID exposure under biasing as in fly conditions. The used radiation source for TID is a tungsten tube X-ray source operated with peak energy 70 kV and 12,5 mA resulting in 37 krad(SiO_2)/h of doserate. The 62 MeV protons exposure are carried on grounded chips at UCLouvain. Irradiations and electrical tests are performed at ambient temperature.

IV. Dark Current and Activation Energies

In storage mode, the accumulated hole layer on the interfaces allow the emptying of electrons from most of the donor traps, hence suppressing midgap states (Fig. 4). It is confirmed by the measure of the activation energy E_a, which equals the Si bandgap. In comparison when inversion is lost at 0 V, midgap states contribute heavily and E_a is back at midgap. These activation energies correlate with the temperature dependence of the SRH interface generation rate in both inverted and depleted configurations (when supposing a sharp maximum for midgap states with $E_t = E_i$) [2]:

$$U_{inv} = -\frac{\sigma v_{th} N_{\mathrm{it}} n_i^2 E_g}{p} \qquad U_{dep} = -\frac{\sigma v_{th} n_i N_{\mathrm{it}} \pi kT}{2} \tag{2}$$

With σ the quadratic mean capture cross sections of the defects, v_{th} the thermal velocity, N_{it} the interface defect density, n_i the intrinsic carrier concentration, E_g the Si bandgap, p the hole concentration and kT the thermal energy of the carriers. When neglecting the prefactors temperature dependence, it leads indeed to $U_{inv} \propto e^{E_g/kT}$ and $U_{dep} \propto e^{E_g/2kT}$. When switching in transfer mode, passivation remains if the transfer time is significantly short when compared to the hole emission time constant of interface states [3]. Under

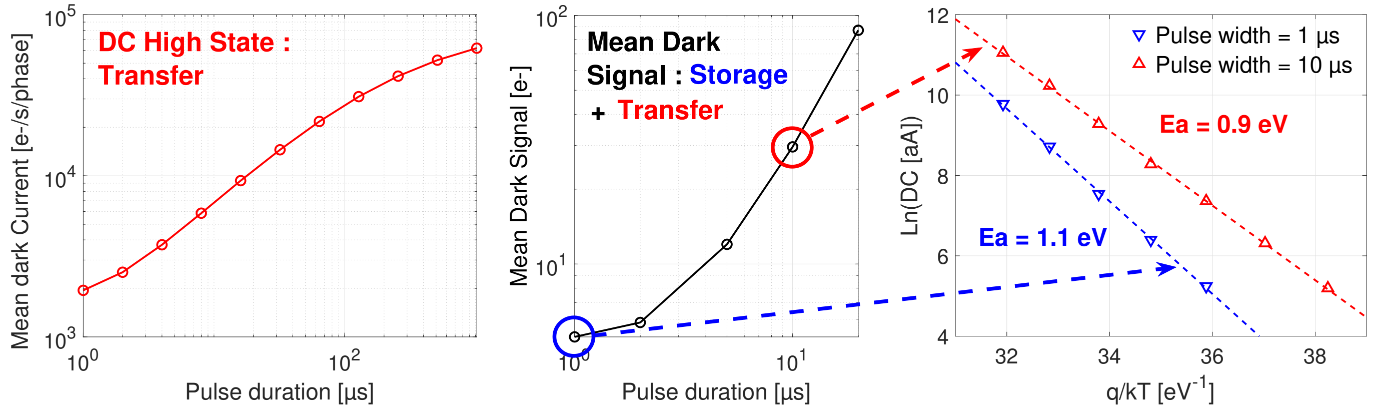

Fig. 5: On the left is the Dark Current at High state (3 V) integrated dynamically for increasing pulse duration. A significant proportion of traps remain occupied by holes for transfer times shorter than the hole emission time constant (≈ 25 ms at 300 K). Hence, the mean DC comprising storage and transfer contributions is greatly reduced for short pulses, with an E_a close to bandgap.

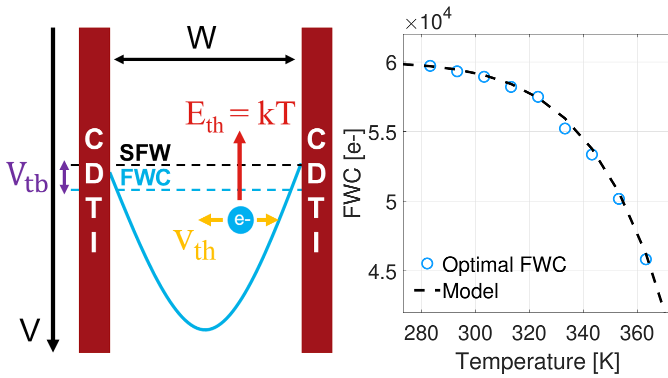

Fig. 6: The thermionic emission is sketched in the context of this device. FWC vs temperature is plotted and compared to equation (3) with t_{PW}=10 µs and V_{tb}=0.46 eV.

similar hypothesis as equation (2), this time constant can be expressed as follow : $\tau_e = (\sigma v_{th} n_i)^{-1}$. Assuming at ambient temperature $\sigma = 10^{-15}\,\text{cm}^{-2}$, $v_{th} = 2.5 \times 10^6\,\text{cm.s}^{-1}$ and $n_i = 1.5 \times 10^{10}\,\text{cm}^{-3}$, it yields $\tau_e = 25\,\text{ms}$. On Fig. 5, the use of much shorter transfer pulses demonstrates the efficiency of the traps deactivation and how much Dark Current can be suppressed. Under nominal charge transfer condition, the mean Dark Signal is reduced using short transfer pulses because (1) integration time at High state is mitigated and (2) interfaces are pseudo-passivated. It enables a Multi-Pinned Phase mode (MPP), essentially suppressing interface state Dark Current [4]. It is confirmed with a measure of the corresponding activation energies in the case of a fully passivated (PW=1 µs) and partially passivated (PW=10 µs) transfer operation. In the first case, $E_a = 1,1\,\text{eV}$ is retrieved, whereas in the later the E_a is diminished by a contribution of midgap interface traps.

V. Temperature Effects

The temperature dependence of the device is investigated through CTI and FWC in prerad conditions to reveal whether native bulk or interface defects plays a significant role in the device performances. For temperature ranging from 260 K to 360 K no bulk defects signature is revealed as the measured EPER CTI at 50% FWC remains within error margin. Considering surface defects, the measure indicates that near to zero interface interactions occur with the charge packet. The calculated emission time constant of midgap states varies from 400 ms to 30 µs with temperature yielding an emission probability during dwell time of 0 to 0.3. In case of a large trap activity, a change in CTI would have been observed. Perhaps higher temperature CTI measurements could reveal small effects. On the other hand, FWC is reduced with increased temperature of operation (Fig 6). At the onset of filling the potential well enclosed in between the CDTIs, the electrons thermal energy kT allow them to hop on to interface traps [5]. Since the thermal energy scales with T, the optimal FWC diminishes by the quantity of electrons able to jump over an effective thermal barrier. It can be modeled considering the electron thermal velocity v_{th}, the average distance to interface $W/2$, the transfer duration t_{PW} and the effective thermal barrier V_{tb}:

$$\text{FWC} = \text{SFW}\left(1 - \frac{2 v_{th} t_{PW}}{W} e^{-\frac{V_{tb}}{kT}}\right) \tag{3}$$

With SFW the Surface Full Well. Such model is compared with the experimental measure on Fig. 6. Considering the discussion above on depletion dark current, it is very likely that this barrier depends also on the proportion of traps that have lost passivation over t_{PW} laps of time.

VI. Radiation Effects

TID tests up to $100\,\text{krad}(\text{SiO}_2)$ were performed on biased packaged devices. The resulting voltage shifts on V_s and V_{dep} are plotted in Fig. 7(a). Since interfaces are depleted for positive biases, the resulting interface charge is neutral and the observed shift is only due to trapped charges in the oxide. Flatband shift follows a 4.1 mV/krad trend. In comparison, CTI is probed against signal output for several transfer duration times and irradiation levels using the EPER method (Fig. 7(b)). Three CTI regimes are noticeable as well as the optimal FWC when CTI switched from Buried Channel (BC) to Surface

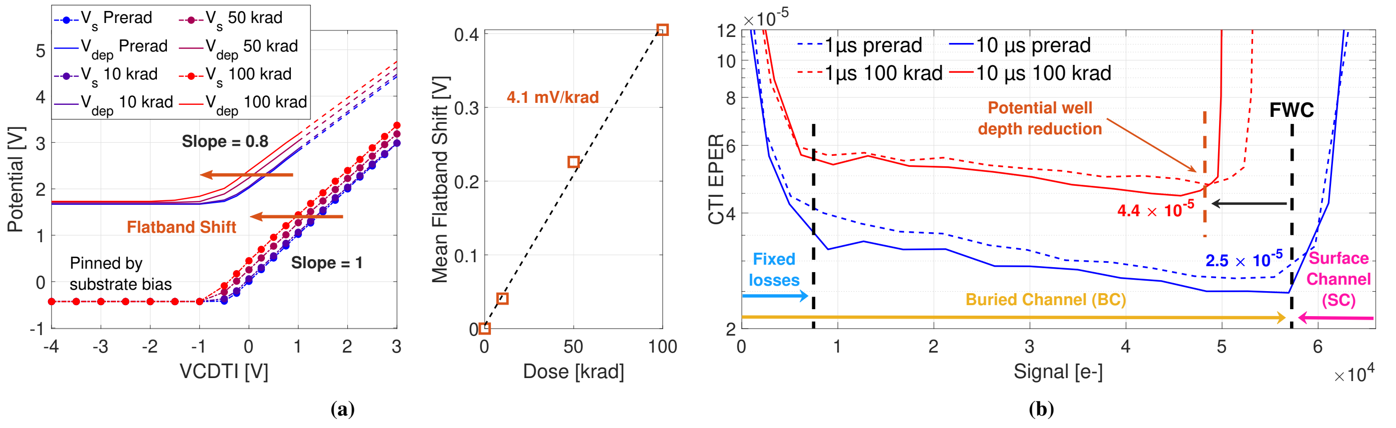

Fig. 7: On (a), potentials vs VCDTI are measured for different irradiation levels, which reveals a flatband shift of 4.1 mV/krad. On (b), Charge Transfer Inefficiency (CTI) is plotted using the EPER method on a reference device and after 100 krad(SiO2) exposure at ambient temperature. The optimal FWC is measured when switching from BC to SC. It is indeed reduced with the TID induced flatband shift.

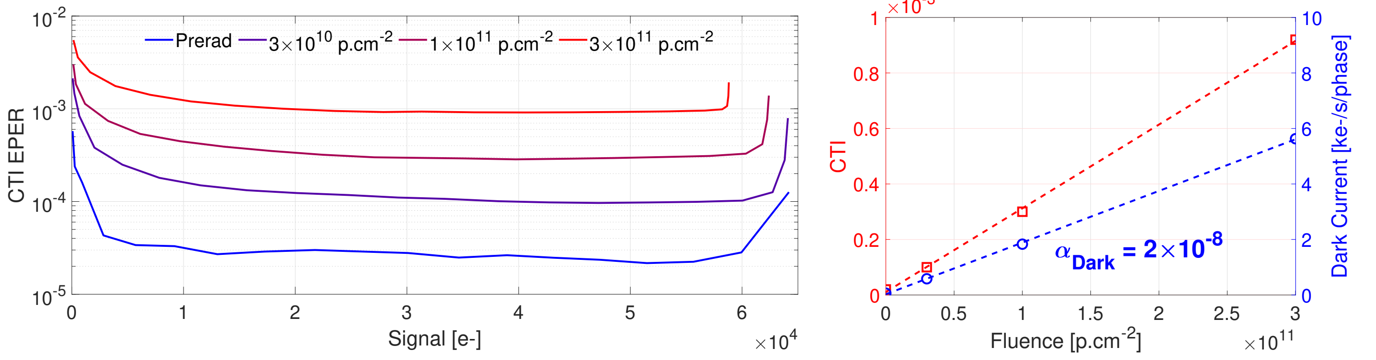

Fig. 8: CTI EPER is plotted for a reference and 3 irradiated devices with 62 MeV protons with fluences of 3×10^{10} p.cm^{-2}, 10^{11} p.cm^{-2} and 3×10^{11} p.cm^{-2}. Mean BC CTI and Dark Current increase are plotted with respect to fluence. One can extract the DC slope to compute the damage factor K_{dark}.

Channel (SC). As expected, FWC is reduced with TID as a consequence of potential well depth cutting induced by trapped charges in the oxide. Results show that transfer time of 1 µs and below is authorized without CTI or FWC trade-off while yielding interface passivation. It seems TID worsens the BC CTI which is believed to be caused by TCDTIs interactions with the charge packet, although further investigations are needed to confirm this hypothesis. Finally, a look at CTI and Dark Current deterioration with 62 MeV protons at different fluences is given in Fig. 8. Charge transfer occurs in a fully depleted BC, only altered by damage in the Si bulk. Proportionality on CTI and Dark Current is found as Displacement Damage Dose (DDD) induces defects in the channel both responsible for generation and trapping. One can extract from this data the damage factor $K_{dark} = \alpha_{dark}/(V_{dep}\mathrm{NIEL}_{62\mathrm{MeV}})$ and find a value of $K_{dark} = 1.85 \times 10^5\ \mathrm{e}^{-}.\mathrm{cm}^{-3}.\mathrm{sec}$ per $\mathrm{MeV.g}^{-1}$ in close agreement with the universal damage factor at $1.9 \pm 0.6 \times 10^5\ \mathrm{e}^{-}.\mathrm{cm}^{-3}.\mathrm{sec}$ per $\mathrm{MeV.g}^{-1}$ [6]. The CTI measure on Fig. 8 also features TID effects since a similar FWC reduction as in Fig. 7 is observed.

VII. Conclusion

The studied device was found promising for high line rate charge domain noiseless binning operations, making it perfectly suitable for high resolution imagery in harsh environment, such as Earth observation using Time Delay Integration (TDI). When compared to the CCD-on-CMOS state of the art using planar gates [7]–[9], the CDTI transfer yields an excellent dynamic range (82 dB) because of improved FWC and fully passivated interfaces. No critical damage was observed within the radiation conditions tested. On the contrary, an opportune TID tolerance is brought by a MPP mode. This study highlights the key requirement of using short transfer times to yield the best performances of this image sensor.

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