A 3.06 µm SPAD Pixel with Embedded Metal Contact and Power Grid on Deep Trench Pixel Isolation for High-resolution Photon-counting

J. Ogi, F. Sano, T. Nakata, Y. Kubo, W. Onishi, C. Koswaththaghe, T. Mochizuki, Y. Tashiro, K. Hizu, T. Takatsuka, F. Koga, T. Hirano, and Y. Oike
Sony Semiconductor Solutions Corporation
4-14-1 Asahi-cho, Atsugi, Kanagawa, Japan
E-mail: Jun.Ogi@sony.com Tel: +81-50-3141-4151

I. Introduction

Single photon avalanche diode (SPAD) pixels have been developed for time-of-flight (ToF) range image sensors [1–3] and photon counting image sensors [4–6]. Recently, the SPAD pixel size has been reduced to 5 µm or smaller to improve the pile-up problem and resolution of the SPAD-based image sensors [7–9]. However, the dark count rate (DCR) and photon detection efficiency (PDE) in smaller SPAD pixels are significantly worse compared to pixels larger than 6 µm [5,10,11]. This is due to edge breakdown (EBD) in the high electric field region at the pixel edge or the small avalanche region. The latest work can address this issue, achieving over 80% PDE and below 5 cps (count per second) DCR with a 3.0-µm-pitch SPAD pixel [12]. However, the crosstalk is higher compared to a 6-µm SPAD pixel due to the small pitch. Additionally, the power consumption and voltage drop with SPAD multiplication must be improved in high-resolution photon-counting image sensors with large array of such small pixels. In this paper, we present a 3.06-µm-pitch SPAD pixel using the embedded metal contact and power grid on two-step deep trench isolation in the pixel to suppress the EBD, the crosstalk, and the voltage drop, and to maintain the PDE and the DCR simultaneously [13]. Additionally, we demonstrate a reduction in charge per event (CPE) with SPAD multiplication by integrating a polysilicon resistor on the SPAD pixel.

II. Pixel structure

Figure 1(a) shows a schematic diagram of the developed 3.06-µm-pitch SPAD pixel. One of the contacts in the pixel is embedded, with the embedded metal contact on the two-step deep trench isolation. This increases the vertical distance between the two contacts, suppressing both EBD and DCR. The metal filling in the deep trench acts as an optical shield, contributing to optical crosstalk suppression through avalanche multiplication. This two-step trench decreases the total width by integrating two functions of the embedded contact and metal shield into one trench structure. Additionally, the metal acts as low impedance metal wiring in the SPAD array, as shown in Fig. 1(b). This "embedded power grid" reduces the voltage drop across the wiring even for a significant multiplication current in a large SPAD array and under high light illumination conditions.

A polysilicon resistor, $R_{k,}$ is integrated on the pixel by inserting it in series with the SPAD and quenching circuit, as shown in Fig. 1(c), and can reduce the amplitude of the voltage swing at the V_{in} node, resulting in SPAD multiplication and contributing to CPE reduction. Figure 1(d) shows a transmission electron microscope (TEM) image of the fabricated 3.06-µm-pitch SPAD pixel. The embedded metal contact and the polysilicon resistor on the pixel are successfully integrated.

III. Pixel potential design

Figure 2 shows the distribution of the electric field on the avalanche multiplication region in the pixel, simulated with the pixel structure using TCAD simulation. Figure 2(a) shows the electric field based on the same design concept for a SPAD pixel larger than 6 µm. The electric field on the pixel edge is high, and edge breakdown can occur in this basic design

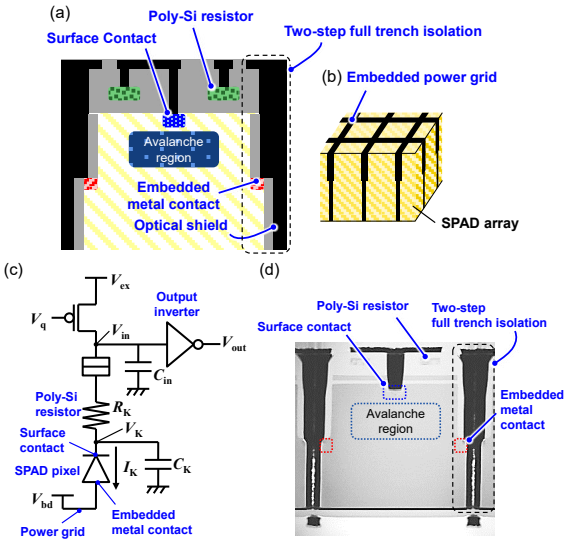

Figure 1. (a) Schematic of 3.06 µm SPAD pixel with embedded metal contact on two-step deep trench pixel isolation and (b) embedded power grid in SPAD array. (c) Circuit diagram for SPAD quenching circuit with polysilicon (Poly-Si) resistor. (d) Cross-sectional TEM image of the 3.06 µm SPAD pixel.

even with the embedded metal contact. We optimized the potential design to decrease the size and increase the depth of the avalanche multiplication region, as shown in Fig. 2(b), resulting in the reduction of the electric field on the pixel edge.

IV. Measurement results of the pixel characteristics

Figure 3 shows a prototype for a proof-of-concept of the 3.06-μm-pitch SPAD pixels. The back-illuminated 3.06-μm-pitch 640 x 1056-pixel array is stacked on a 12.24-μm-pitch 160 x 264 photon counting circuits array with a 14-bit counter via Cu-Cu connections.

Figure 4(a) shows the photon-counting operation with increasing SPAD applied voltage (V_{ex}-V_{bd}). The counting operation starts at approximately 22.4 V, demonstrating that the 3.06-μm-pitch SPAD pixel successfully works as a photon-counting pixel. The median breakdown voltage (V_{bd}) of the pixel can be calculated as 20.9 V with 1.5 V of the threshold voltage (V_{th}) in the output inverter. Figure 4(b) shows the variation of the V_{bd} through the whole pixel array. The variation is 72 mV, which is less than 100 mV, thus successfully demonstrating stable operation of the 3.06-μm-pitch pixel array.

Figure 5 shows the measurement results of DCR with the basic and optimized potential designs from Fig. 2. The DCR is 15.8 cps at 25 °C with the optimized design and 313 cps with the basic design.

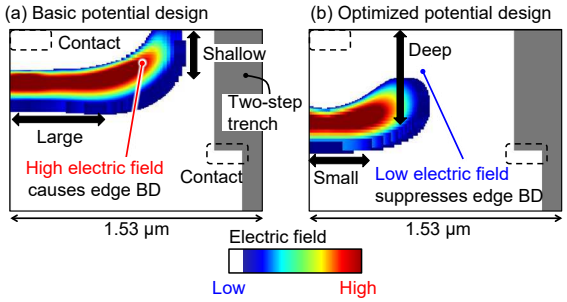

Figure 2. Contour plot of electric field on multiplication region estimated by TCAD simulation with (a) basic potential design and (b) optimized potential design.

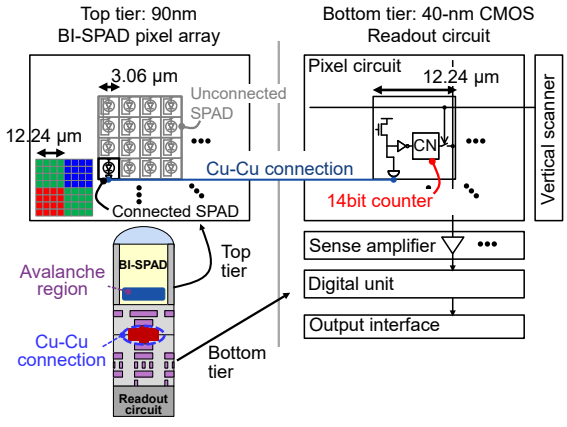

Figure 3. Implementation of prototype for proof-of-concept of the 3.06-μm-pitch SPAD pixels.

The DCR in the optimized design is improved by a factor of 10 compared to the basic design. This result shows that the optimized design can successfully reduce the electric field on the pixel edge, as estimated with the potential simulation in Fig. 2.

Figure 6 shows a measured PDE at various wavelengths. The pixel array of the prototype has a Bayer array of on-chip color filters, and the PDE is measured through each color filter. The peak PDE obtained through the green color filter is 57% with 3 V of V_{ex}. This can be achieved by optimizing the potential slope in the SPAD pixel for electron transfer [14].

Figure 7 shows the measurement results of crosstalk probability with and without full trench isolation. For the crosstalk measurement, a special pixel connection is used where adjacent 3.06-μm-pitch 3 × 3 pixels are connected to the 12.24-μm-pitch photon counting circuit by metal wiring. Figure 7(a) shows that the crosstalk probability is less than 0.4% with the two-step full trench isolation, while Fig. 7(b) shows that the

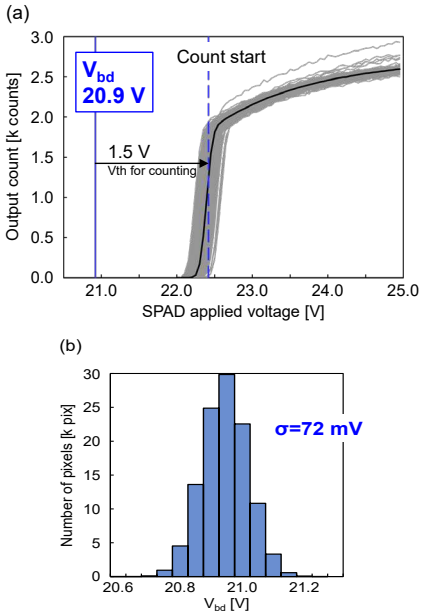

Figure 4. Measurement results of SPAD breakdown operation V_{bd} and its variation at 25 °C.

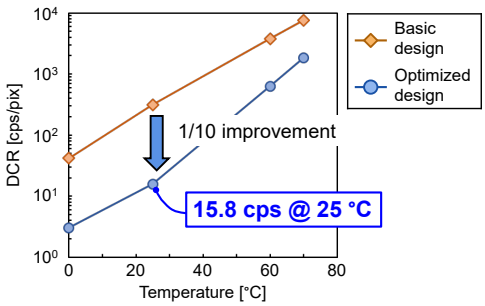

Figure 5. Measurement results of DCR at 25 °C and 3 V of V_{ex} with the two different avalanche potential designs depicted in Fig. 2.

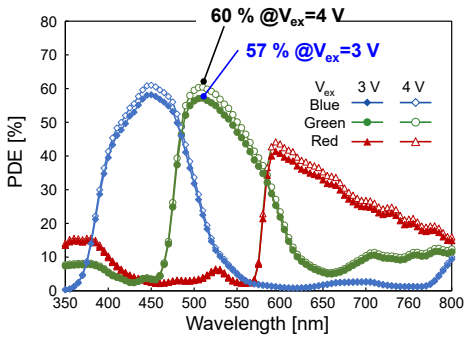

Figure 6. Measurement results of PDE at 25 °C and 3 V and 4 V of V_{ex}.

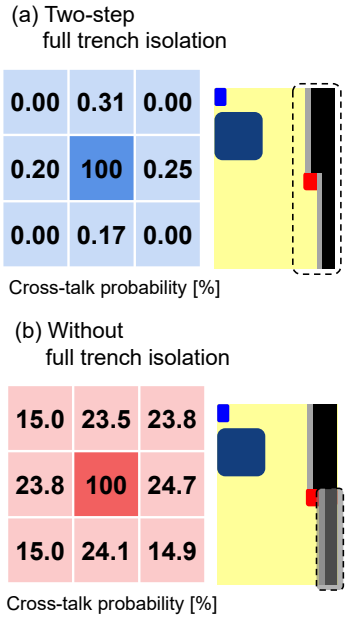

Figure 7. Measurement results of crosstalk probability at 25 °C and 3 V of Vex (a) with and (b) without full trench isolation.

crosstalk probability is greater than 20% without the full trench isolation under the embedded contact. These results highlight the advantage of the two-step full trench isolation, where the embedded metal contact is combined with the full trench isolation.

A color image was successfully captured with only a few defects by using the prototype 3.06-µm-pitch SPAD pixel array as shown in Fig. 8.

V. CPE reduction with polysilicon resistor

The polysilicon resistor on the SPAD pixel can reduce CPE Q_{CPE} with SPAD multiplication using the following equation:

$$Q_{CPE} = C_K V_{ex} + C_{in}(V_{ex} - R_K I_K) \quad (1)$$

Here, C_K is the capacitance at the SPAD cathode before the polysilicon resistor, and C_{in} is the total parasitic capacitance after the resistor to the input node of the output inverter. R_K is the resistance of the polysilicon resistor, and I_K is the current at the SPAD cathode. C_{in} is much larger than C_K because of the Cu-Cu connection and the metal wiring in the CMOS

Figure 8. Image captured with the 3-µm-pitch pixel array and 12-µm-pitch photon counting circuit.

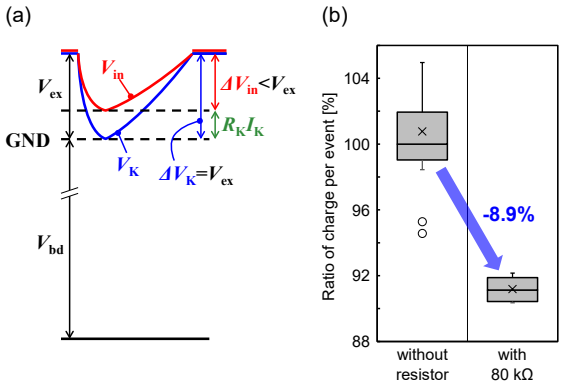

Figure 9. (a) Schematic potential diagram of V_K and V_{in} with SPAD multiplication. (b) Ratio of CPE with 80 kΩ resistor to those without the resistor. The median of the CPE without resistor is 100 %.

circuits, and it dominates the CPE. The contribution of C_{in} can be reduced with R_K because the amplitude of the voltage swing at the input node of the inverter (ΔV_{in}) by SPAD multiplication is reduced by the voltage drop with R_K and I_K, as shown in Fig. 9(a). Figure 9(b) shows the measurement results of the ratio of the CPE with an 80 kΩ polysilicon resistor to those without the resistor. The CPE decreased by 8.9% with the resistor.

VI. Conclusion

Table I and Fig. 10 show a comparison of the pixel characteristics of this work with those of previous works. The PDE obtained in this work is significantly higher than that of previous works with 5-µm-pitch or smaller pixels[7–9], while the DCR is comparable to that of previous works with 6-µm-pitch pixels [5,10,11]. The PDE and DCR are worse than those with 3.3- or 3-µm-pitch pixels [12], while the crosstalk is lower than those of [12]. This is because of the full trench isolation with embedded metal and the extension of the metal over the silicon surface, as shown in Fig. 1(a) and (d). Additionally, the integration of a power grid and the polysilicon resistor on SPAD pixels can contribute to a reduced voltage drop in anode power supply and reduced power consumption with SPAD multiplication, respectively, in a large SPAD pixel array for a high-resolution photon-counting image sensor.

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Table I. Characteristics comparison with previous works.

	Unit	[5]	[10]	[11]	[7]	[8]	[9]			[12]			This work
Pixel pitch	µm	6.12	6	6.39	5	3	4	3	2.2	3.3	3.0	2.5	3.06
Array size	-	160 X 264	N/D	2072 X 1548	N/D	4 x 4	4 x 4			N/D			160 X 264
Techno-logy	-	BI-3D 90 nm	BI-3D 90 nm	BI-3D 90 nm	FI	FI 130 nm	FI 180 nm			BI-3D 90 nm			BI-3D 90 nm
V_{bd}	V	N/D	22	30	N/D	15.8	22.1	23.6	32.35	19	19	18	20.9
V_{ex}	V	3	3	2.5	5.8*3	1.2	6	6	6	3	3	3	3
Peak PDE	%	58	69.4*1	69.4	12*2*3	6*3	14.2	5.6	2	82.5	78.3	76.1	57
DCR @25°C	cps	35.4	19	1.8	17.3*3	1343	2.5	1.6	751	2.2	2.2	173	15.8
Cross-talk	%	N/D	0.5	N/D	4.9*3	<0.2*4	3.57	2.75	2.97	0.85	0.95	1.0	<0.4

*1 Referred from [12]
*2 No data for peak PDE. The largest value in the article is used.
*3 No numerical value is expressed in the articles. The author calculated the value from the graphs in the articles.
*4 Vex = 1V.

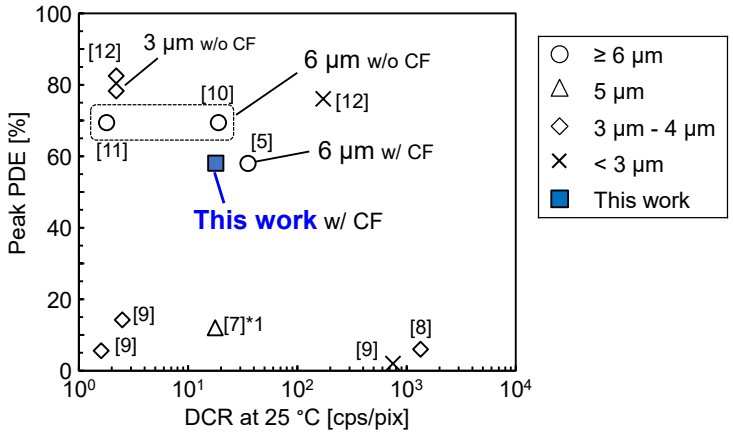

Figure 10. Comparison of PDE and DCR with previous works.
*1 No data for the peak PDE. The largest value in the manuscript is used.

A high PDE and high maximum count rate and low power consumption 3D-stacked SPAD device for Lidar applications

B. Mamdy[1] ; R. A. Bianchi[1] ; D. Golanski[1] ; B. Rae[2] ; T. M. Bah[1] ; D. Rideau[1] ; F. Twaddle[2]; R. Helleboid[1] ; C. Buj[3] ; N. Moussy[3] ; R. Fillon[1] ; Y. Henrion[1] ; E. Lacombe[1] ; R. Neri[1] ; F. Brun[1]; I. Nicholson[2] ; M. Agnew[2] ; B. Murray[2] ; M. Basset[1] ; R. Perrier[1] ; M. Al-Rawhani[2] ; S. Jouan[1] ; A. Lopez[2] ; L. Stark[2] ; S. Pellegrini[2]

[1]*STMicroelectronics, 850 rue J. Monnet BP16, 38926 Crolles cedex, France*
E-mail: bastien.mamdy@st.com Tel : +33 6 78 36 43 12
Email: raul-andres.bianchi@st.com Tel : +33 7 64 40 92 79
[2] *STMicroelectronics, 1 Tanfield, Inverleith Row, Edinburgh EH3 5DA, UK*
[3] *CEA LETI, 17 Av. des Martyrs, 38054, Grenoble, France*

***Abstract*—We present a 10.17µm pitch 3D-stacked backside illuminated Single Photon Avalanche Diode (SPAD). The wafer stack features a fully custom top tier process which is highly optimized for optical performance and a 40nm bottom tier which enables dense and low-power signal processing, local to the pixel array. State-of-the-art pixel performance is presented with a specific focus on high-sensitivity, low power, and high-speed operation. With a minimum operating voltage of 19.1V (at 60°C) a PDE of 18.5% is obtained at 940nm, with a 2.5V excess bias (which rises to 22% at 3.5V), with low DCR and low Jitter. This is achieved while consuming only 70fC of charge per pulse. The combination of low breakdown voltage and low charge per pulse minimizes power consumption which is essential for array scaling and for enabling low-power portable applications. With the selected sensing circuit design, tailored for high frequency performance, 85Mcps Max Count Rate is achieved, with a 2.5V excess bias (rising to >110Mcps at 3.5V), significantly reducing the pressure on pixel pitch reduction to cope with high illumination levels.**

Keywords— SPAD pixel, 3D 40nm SPAD technology, Low Power, High Count Rate, LIDAR, portable applications.

I. INTRODUCTION

Three-dimensional technology has revolutionized the field of electronics by enabling the development of more compact and more performant devices and pixels. Single-Photon Avalanche Diodes (SPADs) are a critical component in the field of imaging applications. The use of 3D technology in SPAD fabrication allows for the creation of smaller, more sensitive devices [2][3][4], but also faster and more power efficient devices, making them ideal for applications such as medical imaging, time-of-flight (TOF) ranging, and 3D imaging; most of them operate in the Near Infra-Red (NIR) and can require large pixel arrays (>100Kpixels) with specific requirements in terms of low power consumption and high dynamic range.

The pixel diodes and their driving/data-processing circuits presented are realized in-house on separate wafers, joined together through a standard wafer bonding technique and back-side processed. For the top-tier imaging technology, silicon remains the best choice for SPADs due to the maturity, reliability, and production costs of 300mm silicon process platforms, although III-V materials have superior optical properties in the infrared. Special care has been taken at SPAD design & process levels to maximize sensitivity, in the NIR, together with low power consumption.

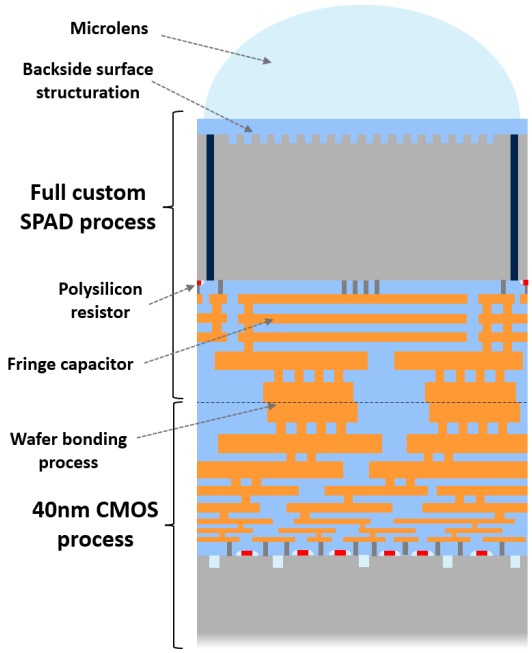

Fig. 1. Cross-section of our 3D-stacked backside illuminated SPAD pixel.

For the bottom-tier, a 40nm CMOS technology has been selected, which offers high circuit density, low cost and high silicon processing and chip design maturities. Special care has been taken in the design of the sensing circuitry of the pixel to ensure very high-count rates.

In this paper, we will explore the development of this SPAD in 3D 40nm technology, discussing the benefits of the technology and the pixel design, the challenges faced during its development, and potential advantages for applications demanding high-sensitivity together with low-power and high-count rates.

II. SPAD Pixel 3D Architecture

Fig. 1 shows the whole pixel structure: a 10.17µm pitch 3D-stacked backside illuminated SPAD architecture optimized for high sensitivity. It is composed of a 40nm CMOS, bottom-tier technology with 7 interconnect layers, and a 65nm top-tier imaging technology with 4 interconnect layers. Both are realized in-house on separate wafers and joined together by a standard hybrid bonding process performing electrical connections at pixel level. Back-side processing consists of surface structuration, anti-reflective coatings, micro lenses, and passivation layers.

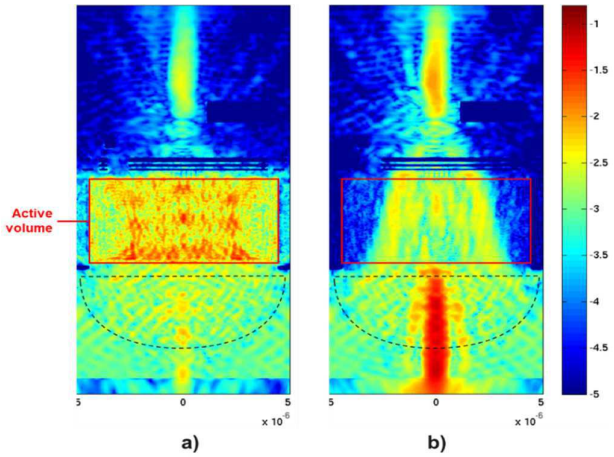

Fig. 2. Cross-section of a 3D-FDTD optical simulation showing the Poynting vector amplitude (log scale) for light at 940nm for our SPAD with (a) and without (b) back-side structuration.

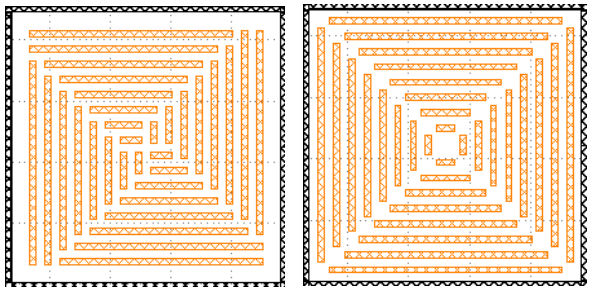

Fig. 3. Top view of the back-side structuration patterns used to significantly increase the optical absorption of the SPAD.

The 3D back-side illuminated structure allows high fill factor and isolates a large carrier collection volume. The resulting NIR sensitivity increase is in the order of a factor 10, compared to previous front-side 2D SPAD technologies. To maximize the photon absorption within the active volume, a back-side structuration pattern has been optimized through 3D-FDTD simulations (see Fig. 2). It has been implemented with a dedicated etch process, different than the conventional wet process leading to inverted pyramid shapes [1]. Trench-like shapes are produced, allowing a large variety of structuration pattern designs (see Fig. 3) and specific optimizations.

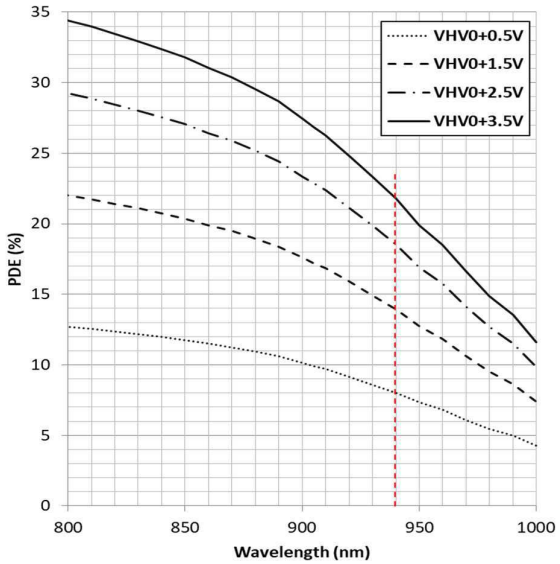

Fig. 4. Photon Detection Efficiency vs wavelength and excess bias at 60°C.

III. SPAD Pixel Standard Performances

The back-side structuration, plus the highly reflective interfaces, induces multiple reflections within the silicon volume and hence increases the effective silicon path-length that light travels through (See in Fig. 2-a, that an almost full pixel illumination is obtained when back-side structuration is added). This, combined with the action of the backend metal reflector, results in an additional sensitivity increase in the order of a factor 4, allowing us to reach never seen before Photon Detection Efficiency (PDE, illustrated in Fig. 4) densities of 0.04%/µm3 of silicon at 940nm, almost twice as high as the value reported in state-of-the-art SPAD devices [2][3].

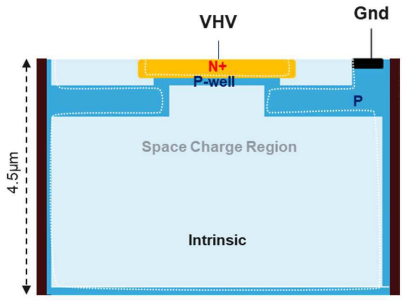

Fig. 5. Diode cross-section with doping scheme.

The diode architecture and implantation scheme are described in Fig. 5. The diode is an N+ over PWell junction

built on a very lightly doped substrate. The PWell depth and doping level are optimized such as to maximize the junction's breakdown probability, maintain ~18.6V breakdown voltage (VBD), at 60°C, and allows for the entire PWell depth to be depleted at breakdown voltage. Indeed, at the standard operating condition, the space charge region extends deeply within the 4.5µm thick substrate volume. A P-doped guard ring implant is designed and fabricated to prevent edge breakdown and redirect photogenerated carriers towards the central avalanche region.

With a minimum operating voltage (also called VHV0) of 19.1V , at 60°C, a PDE of 18.5% is achieved at 940nm, at 2.5V excess bias (which rises to 22% at 3.5V excess bias, as shown in Fig. 4), together with a low Dark Count Rate (DCR) of 0.81kcps and low Jitter of 119ps Full Width at Half Maximum (FWHM).

IV. Low Power and High Count Rate

The SPAD pixel performances quoted above are achieved while consuming less than 70fC of Charge per Pulse (CPP) at nominal 2.5V excess bias, as illustrated in Fig. 6. The combination of low breakdown voltage and low charge per pulse greatly minimizes array power consumption which is essential for array scaling and for enabling low-power portable applications.

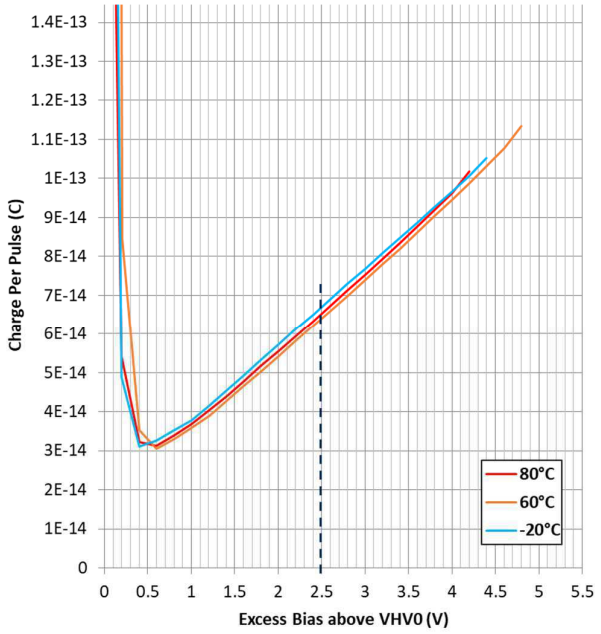

Fig. 6. Quantity of charges generated per avalanche as a function of excess bias and temperature.

This optimized diode architecture is associated to a novel readout circuit described in Fig. 7. Unlike regular SPAD devices [4][5], both the quenching and the detection of the avalanche is performed on the high voltage node (the cathode), as its low capacitance minimizes the pixel power consumption. Similarly, on the high voltage side, a very highly resistive, high voltage compatible, resistor R_Q, is implemented for quenching purposes and to passively limit the power consumption in case of SPAD paralysis, at excessively high illumination levels.

Finally, a combination of a high-voltage cascode N-type MOSFET, a low-voltage N-type enable MOSFET, and a V_{PULLUP} clamp diode, all connected to the anode of the SPAD, allows full disable of selected pixels. When EN is set to V_{SUB}, the anode voltage is allowed to rise more than the excess bias, putting the SPAD safely out of Geiger mode. This is a necessary feature for two reasons: to disable the few defective pixels exhibiting high DCR during BIST system runs, and to disable the array sectors that are not addressed or that are non-illuminated, allowing both very significant power savings, at SPAD array level.

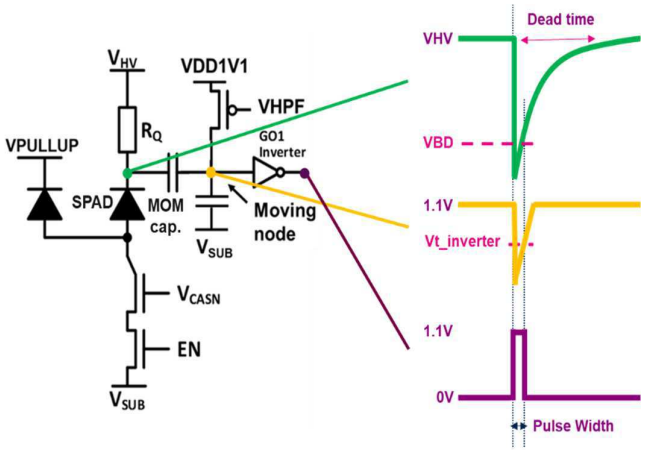

Fig. 7. Pixel schematics including the SPAD diode, the quenching resistor RQ, the Metal-Oxide-Metal coupling capacitor, the readout circuitry, and the disabling circuitry. Expected voltage swing observed at the SPAD cathode (green), the pulse shaping node (yellow) and after the inverter (purple).

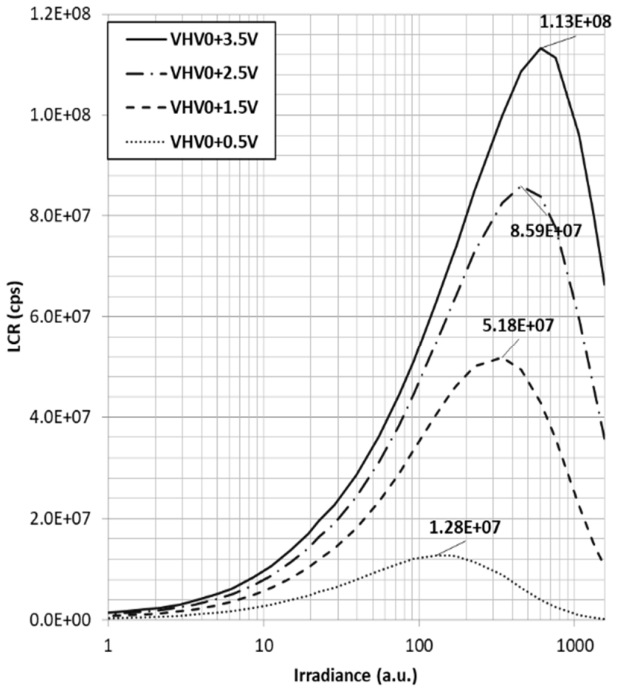

Fig. 8. Light Count Rate (LCR) measurement vs excess bias at 60°C. Max Count Rate (MCR) values correspond to the peak of each LCR curve.

For high frequency performance reasons, the detector is AC-coupled, through a 25V Metal-Oxide-Metal capacitance that also acts as a capacitive voltage divider, as shown in Fig. 7, between the cathode of the SPAD and the input of the inverter; the latter being used to generate the pulsed output signal of the pixel. A pulse shaper transistor is also embedded and connected to the input of that inverter, as a pull-up element. In standard operating conditions, Vhpf is set to 0V to obtain an additional high pass band action that maximizes the bandwidth of the whole detection circuit.

This high frequency detection scheme, that to the best of our knowledge has never been reported, enables very high Max Count Rates (MCR), beyond 100Mcps, as illustrated by Fig. 8. This feature is essential for dynamic range, as PDE increases. In addition, it significantly reduces the pressure on pixel pitch reduction [4], to cope with high illumination levels.

V. Comparison with the State-of-the-Art

TABLE I. summarizes main pixel performance, at 60°C, and for different excess bias conditions along with a comparison to state-of-the-art. Performance at 2.5V excess bias, are comparable to state-of-the-art for 940nm PDE, DCR and Jitter and beyond state-of-the-art for power consumption (CPP, VBD, Ve) and for maximum quench/recharge speed related metrics (MCR, DT).

TABLE I. Pixel Performance Comparison

Parameters	Unit	This work			[2]	[4]
BI Technology	nm	65/40			90/40	90/22
Pixel Pitch	um	**10.17**			10	6
VBD @ 60°C	V	**18.6**			20	22
Excess Bias (Ve)	V	1.5	**2.5**	3.5	3.0	3.0
PDE @ 940nm	%	14	**18.5**	22	14.2	20.2
DCR @ 60°C	kcps	0.57	**0.81**	1.27	0.22	0.3
Jitter FWHM	ps	143	**119**	103	173	137
Max Count Rate	Mcps	52	**85**	113	50	60
Dead Time (DT)	ns	6.9	**4.3**	3.3	8.0	6.3
Charge per Pulse	fC	48	**68**	92	-	-

Even higher sensitivity and speed can be obtained at 3.5V excess bias, at the cost of a higher CPP. Conversely, at a low excess bias of 1.5V, a significant CPP reduction is obtained, while maintaining very good PDE, Jitter, MCR and DT performances.

In TABLE II. pixel performance versus temperature, from -20°C to 80°C, is presented. The VBD and DCR exhibit classical thermal coefficients, of +25.6mV/°C and x2 each 7°C (at high temperature) respectively; while PDE, Jitter, MCR, DT and CPP remains almost unaffected by temperature variations over a very wide range, at constant 2.5V excess bias.

TABLE II. Pixel Performance vs Temperature

Parameters, at 2.5V Ve	Unit	-20°C	**60°C**	80°C
Breakdown Voltage (VBD)	V	16.6	**18.6**	19.2
PDE @ 940nm	%	17.6	**18.5**	18.2
Dark Count Rate (DCR)	cps	8.6	**810**	6923
Jitter FWHM	ps	118	**119**	185
Max Count Rate (MCR)	Mcps	72	**85**	88
Dead Time (DT)	ns	5.1	**4.3**	4.2
Charge per Pulse (CPP)	fC	76	**68**	67

VI. Conclusions

Technology and pixel performance has been presented for a 10.17µm pitch SPAD pixel implemented in a 40nm 3D-stacked backside illuminated technology that represents a significant advancement in the field of single-photon detection, especially for large array applications, requiring low-power consumption and high count-rates. State-of-the-art sensitivity at 940nm (PDE) and noise figures (DCR, Jitter) have been achieved, together with a very significant progress in VBD, CPP, MCR and DT, maximizing pixel dynamic range, thanks to the introduction of specific and novel features at technology, avalanche diode design and sensing circuit design levels.

Specific focus on low-power pixel and array design is essential to enable large array scaling, especially for portable applications. The high-frequency performance of the pixel driving and sensing circuitry enables very high count-rates, which is necessary to sustain high illumination operation. As the demand for high-performance, low-power single-photon detectors continue to grow, this 3D 40nm SPAD technology represents a high performant and cost-effective solution.

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A NIR Enhanced SPAD Fabricated in 110 nm CIS Technology with 78% PDP at 500 nm

Utku Karaca, Ekin Kizilkan, Claudio Bruschini, and Edoardo Charbon
Advanced Quantum Architecture Laboratory (AQUA), École Polytechnique Fédérale de Lausanne (EPFL), Neuchâtel, Switzerland
(e-mail: utku.karaca@epfl.ch; ekin.kizilkan@epfl.ch; claudio.bruschini@epfl.ch; edoardo.charbon@epfl.ch)

***Abstract*—In this work, we demonstrate a 10 µm diameter single-photon avalanche diode (SPAD) fabricated in 110 nm CMOS Image Sensor (CIS) technology with enhanced near-infrared (NIR) sensitivity. Thanks to the electric field engineering with the numerical simulations, the electric field is kept high throughout a wide depletion region by the existence of the extra second peak in the profile. Consequently, this favors the absorption of NIR photons and augments the avalanche triggering probability. The measurement results show that at an excess bias voltage of 4 V, the device reaches a photon detection probability (PDP) of 50% at a wavelength of 500 nm with a normalized dark count rate (DCR) of 0.76 cps/µm^2. At 5.5 V, PDP at 500 nm reaches 78%, while DCR stays at 3.7 cps/µm^2 with an afterpulsing probability of 3%. Furthermore, at 850 nm, the device achieves a PDP of 13% and 25.5% at the same excess bias voltages. To the best of our knowledge, these results are among the highest NIR and visible PDPs obtained in any CMOS SPAD. The jitter of the device is 115 ps at 850 nm at 5.5 V excess bias, which makes the device a great candidate for single-photon sensing at red and NIR wavelengths.**

I. Introduction

Applications such as light detection and ranging (LiDAR), optical tomography, and fiber optic communications require high-sensitivity photodetection in the NIR [1]–[3]. Therefore, there has been an increasing effort towards improving NIR efficiency in solid-state photodetectors. In this category of detectors, SPADs exhibit photon-counting capability and low jitter in a compact and generally low-cost format. In order to enhance sensitivity in the NIR, deeper junctions and wider depletion regions have been investigated to be able to collect deeply absorbed NIR photons in silicon [4]–[11]. Deep multiplication regions are very effective at shifting peak detection wavelengths to NIR while causing a sensing efficiency loss in visible. In wide depletion regions, the electric field magnitude becomes relatively low, and it decays from the multiplication regime to the opposite end of the junction. Therefore, wide depletion devices require high excess bias voltages (∼10 V) to increase the electric field magnitude and avalanche triggering probability. However, high excess biases can increase band-to-band (BTB) and trap-assisted tunneling (TAT) contributions to DCR and lead to noisier devices. Besides, it might complicate the pixel circuit design when the excess bias becomes higher than the allowed rail-to-rail voltage range.

In this study, we propose a new SPAD device to address the high excess bias requirement in the wide depletion region approach. To be able to augment the electric field magnitude and avalanche triggering probability, extensive numerical simulations on TCAD were conducted, which enabled us to design a double-peaked electric field profile and keep the electric field magnitude high throughout a wide depletion volume. This new double-peaked profile is in contrast to the previously designed wide depletion and NIR enhanced SPADs, where the devices only have one peak and the magnitude of the electric field stays low in the remaining depletion region. Owing to this electric field engineering and designing a non-isolated device, we expected to increase NIR PDP while not sacrificing sensitivity in the visible spectrum. The device, afterwards, was fabricated in 110 nm CIS technology node and has an active area with a diameter of 10 µm.

II. Device Design and TCAD Simulations

To create a double-peaked electric field profile and enhance the multiplication rates of the carriers in the depletion region, we utilized a technology-specific deep p-well layer/high-voltage n-well junction where the p-well layer has double peaks in its doping concentration. Thanks to these double peaks in the p-well layer, we also achieved two peaks in the electric field profile. The chosen p-well layer is also relatively lightly doped, which allowed us to obtain a wide depletion region. Moreover, the high-voltage n-well layer was extended to form a guard ring around the main junction and prevent the device from suffering premature edge breakdown. The cross section of the device is provided in Fig. 1.

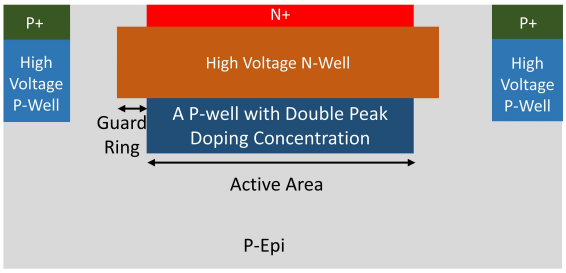

Fig. 1. The cross section of the proposed device.

The electric field simulations of this device can be seen in Fig. 2. The simulations were performed on TCAD numerical tool. Exact doping profiles of the layers used in the cross section were imported into the simulation environment. Then, coupled Poisson and electron-hole drift-diffusion equations

were solved to calculate the electric field magnitude under various voltages. As illustrated in Fig. 2a, in addition to the first electric field peak indicated with red, the second peak appears in the proposed device's field profile at 1 V excess bias, which is depicted with yellow. The variation of the electric field from 1 V to 5 V excess bias voltage is also given, where the second peak becomes more obvious with its emerging red color. Besides, the magnitude of the electric field at the center of the device along the y axis from 1 V to 5 V excess bias is provided in Fig. 2b. It demonstrates that the electric field profile indeed has double peaks, and its magnitude is kept high almost in the entire depletion region, which will result in boosting avalanche triggering probabilities for the electrons and holes and the PDP accordingly. In fact, the electric field magnitude of the second peak is also above the critical avalanche breakdown field in silicon, which is $3x10^5$ V/cm. Therefore, the second peak will behave as a second multiplication center for the carriers, which is a new concept for SPAD design and can be utilized to enhance PDPs in any CMOS technology.

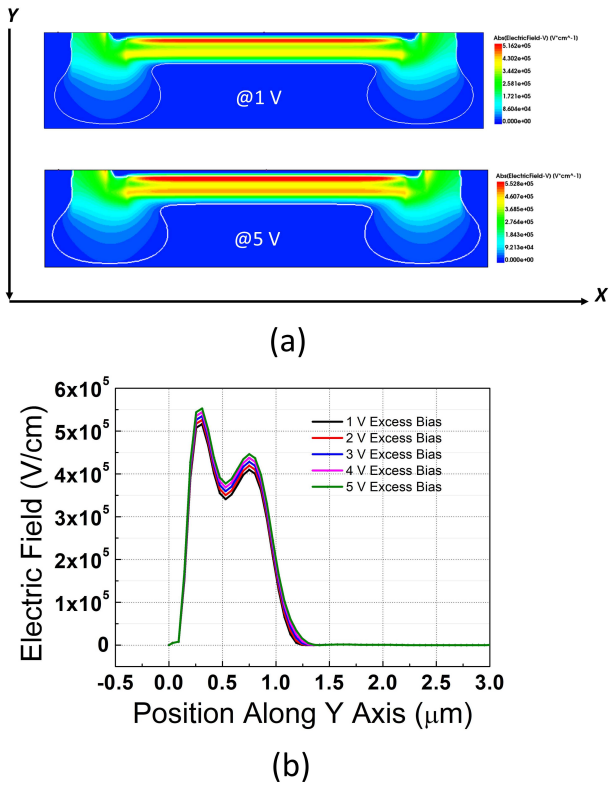

Fig. 2. (a) Electric field simulations of the proposed device on TCAD. (b) Electric field magnitude acquired at the center of the device along the y axis. *Note: White lines on electric field simulations correspond to the depletion region boundaries.*

III. Characterization Results

A. I-V Measurements and Light Emission Tests

Fig. 3a shows the I-V characteristics of the device under ambient light and at room temperature. The breakdown voltage, which is displayed by the sharp increase in the current, occurs at 29.8 V. To verify that the device does not suffer from premature edge breakdown, light emission tests were performed at 3 V and 5 V excess bias voltages. Fig. 3b shows that there is no edge breakdown effect in the proposed device, thanks to the implemented guard ring structure in the design. These results prove that the device functions properly in Geiger mode.

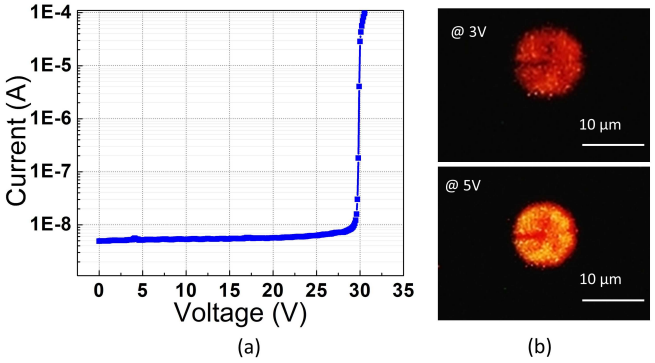

Fig. 3. (a) I-V measurement of the SPAD under ambient light and at room temperature. (b) Light emission tests of the device at 3 V and 5 V excess bias voltages.

B. DCR Measurements

The DCR measurements were taken with an externally connected 660 kilo-ohm resistor to quench and recharge the SPADs. We have measured the same SPAD from different dies to collect statistics about the noise. Fig. 4 demonstrates the DCR measurements belonging to five devices with respect to the excess bias voltage. According to this graph, Device 3 was selected as a reference since it corresponds to the median in the noise measurements. The DCR of this device changes from 8 cps at 1 V to 295 cps at 5.5 V excess bias and at room temperature. The DCR per unit area at 5.5 V excess is 3.7 cps/μm^2, which is among the lowest noise in NIR enhanced SPADs fabricated with CMOS technologies. In the rest of the paper, we will present the characterization results of Device 3.

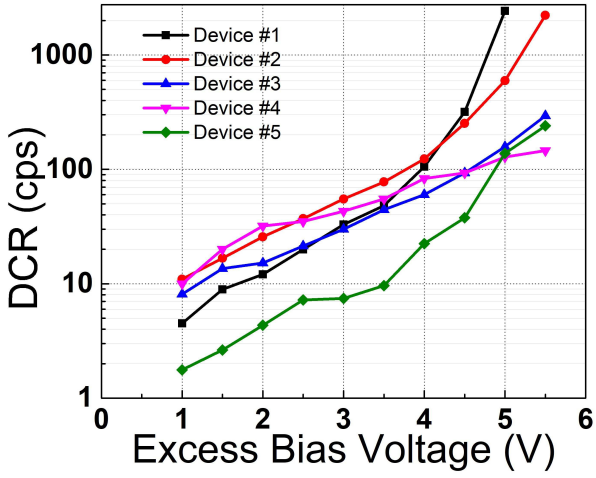

Fig. 4. DCR characterization of the proposed device with respect to the excess bias voltage from five different dies.

C. Afterpulsing Probability Measurement

The afterpulsing histogram of the device was obtained with the inter-avalanche time method. To measure the time interval between the pulses, a high-speed digital oscilloscope (Teledyne LeCroy WavePro 760Zi-A) was utilized. An afterpulsing histogram obtained under dim light is shown in Fig. 5. As the SPAD was passively quenched and recharged through an external resistor, the dead time of the SPAD was around 7 µs. The afterpulsing probability of the device is 3% at 5.5 V excess bias, which is calculated as the ratio of the area between the measured and fitted curves to the area beneath the fitted curve. Hence, this low afterpulsing probability indicates that the defect concentration in the fabricated device is likewise expected to be low.

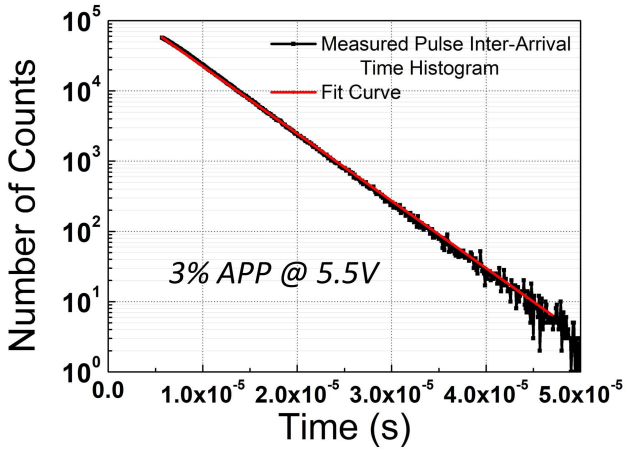

Fig. 5. Inter-arrival avalanche timing histogram with an exponential fit and afterpulsing probability at the excess bias voltage of 5.5 V.

D. PDP Measurements

The PDP of the device was measured via a monochromator setup where a Xenon lamp emits broad-band light and a monochromator selects each wavelength through the gratings. Then, an integrating sphere was used to provide spatially uniform light onto the SPAD and a calibrated reference detector to precisely assess the impinging photon count. Under this configuration, the measured PDP of the device was obtained as shown in Fig. 6, from 1 V to 5.5 V excess bias voltage. As is more obvious at 5.5 V, the peak PDP actually occurs at two different wavelengths, which are 450 nm and 500 nm. We think that this is related to the two-peak nature of the electric field profile of the device, which thereby forms two multiplication regions favoring the detection of these wavelengths the most. At an excess bias voltage of 4 V and 500 nm wavelength, the device has a PDP of 50%, and at 5.5 V excess, PDP at 500 nm reaches 78%. Furthermore, thanks to the high electric field achieved throughout the depletion region, NIR sensitivity of the device is also enhanced. At 850 nm, the SPAD has a PDP of 13% and 25.5% at 4 V and 5.5 V excess bias voltages, respectively. To the best of our knowledge, these PDP values are the highest reported for visible and NIR wavelengths.

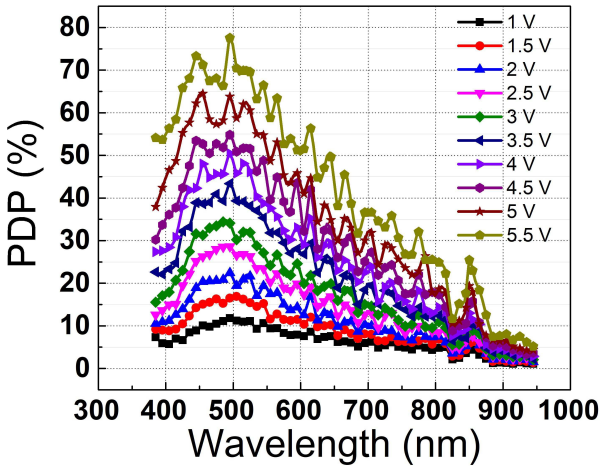

Fig. 6. PDP measurement of the device from 1 V to 5.5 V excess bias voltage.

E. Jitter Measurement

To measure the timing jitter, the time-correlated single-photon counting (TCSPC) technique was employed. The device was illuminated with a 850 nm (A.L.S. GmbH) pulsed laser operating at 100 kHz, and incident power was reduced to single-photon regime with the absorptive neutral density filters. To detect the time difference between the laser clock signal and the positive edge of each avalanche pulse, we used the same high-speed digital oscilloscope. The jitter histograms acquired at 850 nm and at 3 V and 5.5 V excess biases are provided in Fig. 7. The jitter is calculated as full width at half maximum (FWHM), which is 200 ps at 3 V excess bias and reduces to 115 ps at 5.5 V excess bias voltage.

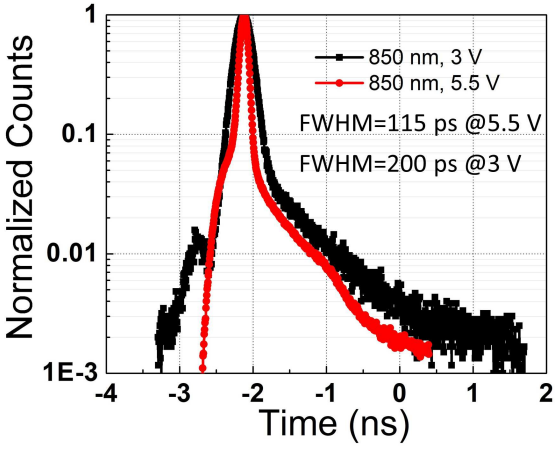

Fig. 7. Timing jitter histogram of the device, which was obtained at 850 nm and for 3 V and 5.5 V excess bias voltages.

IV. Comparison with State-of-the-Art

In Fig. 8, we have chosen the best-performing front-side-illuminated (FSI) CMOS SPADs having a wide depletion and NIR enhanced sensitivity to compare our device with. Fig. 8a indicates the peak PDP achieved with these SPADs versus the normalized DCR with the active areas. As can be seen, our device attains the highest PDP ever reported, along with

one of the lowest DCR per unit area. Fig. 8b shows the PDP comparison at 850 nm wavelength with respect to the excess bias voltage. It demonstrates that our device indeed eliminates the high excess bias needed in wide depletion devices, owing to the double-peaked electric field engineered in this work that increases avalanche triggering probability. Fig. 8b also illustrates that our device reaches one of the highest PDPs at NIR.

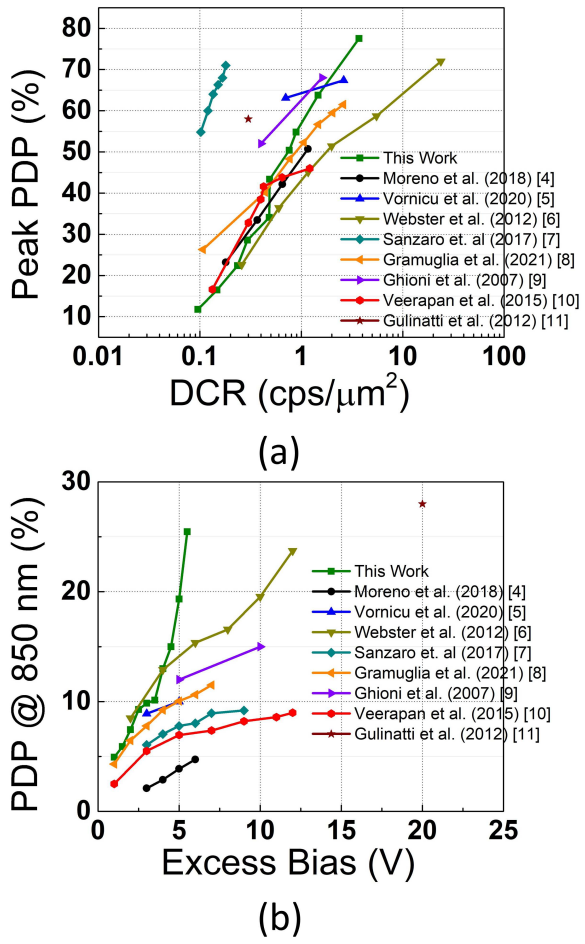

Fig. 8. (a) Peak PDP vs. DCR per unit area, (b) PDP at 850 nm vs. excess bias voltage comparisons of the state-of-the-art FSI SPADs fabricated in the same and other CMOS technology nodes.

V. Conclusion

In this work, we presented a new SPAD design with low noise and enhanced NIR PDP. A double-peaked electric field formed inside the wide depletion region of the device, enabling it to increase the avalanche triggering probability and hence the PDP of the SPAD, which reaches 78% at 500 nm and 25.5% at 850 nm at 5.5 excess bias voltage. The noise of the SPAD remains at 300 cps or 3.7 cps/μm^2 at the same voltage. We believe that this new concept of designing SPADs will pave the way to the design for novel red and NIR enhanced SPADs in near future.

Acknowledgment

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GeSi SPAD for SWIR Sensing and Imaging

N. Na*, Y.-C. Lu, Y.-H. Liu, P.-W. Chen, Y.-C. Lai, Y.-R. Lin, C.-C. Lin,
T. Shia, C.-H. Cheng, C.-L. Hsieh, C.-F. Liang, and S.-L. Chen

Artilux Inc., Zhubei City, Hsinchu County, Taiwan
*neil@artiluxtech.com

We demonstrate a high-performing germanium-silicon (GeSi) single-photon avalanche diode (SPAD) operated at room and elevated temperatures, featuring a low breakdown voltage (BV) < 12 V. At room temperature, dark count rate (DCR) and single-photon detection probability (SPDP) are measured to be ~10 kHz/μm^2 and ~10 % from a device with active area of 15 μm diameter, at a low excess bias (EB) of only 0.5 V. As proof-of-concept, we operate such a GeSi SPAD in conjunction with active quenching circuit (AQC) and time-to-digital circuit (TDC), and successfully capture time-of-flight (TOF) histograms at the proximity of a few to tens of centimeters.

The capability of detecting single photons through solid-state sensors and imagers has greatly advanced research fields such as optical quantum information processing, bio-photonics, and light detection and ranging (LiDAR). While technologies such as Si photomultiplier (SiPM), Si SPAD, InGaAs SPAD, visible-light photon counter (VLPC), and superconducting nanowire single-photon detector (SNSPD) have been demonstrated, issues such as operation temperature and manufacture cost remain as major hurdles towards commercialization. Recently, Si SPAD for three-dimensional (3D) sensing and imaging at near-infrared (NIR) wavelength has attained consumer-level commercialization, and such a success can be attributed to factors such as 1) high crystalline quality allowing very low DCR at room temperature, and 2) compatibility with complementary metal-oxide-semiconductor (CMOS) fabrication making low-cost integration between devices and circuits possible.

However, there has been a growing demand in migrating the operation wavelength from NIR to short-wavelength infrared (SWIR), to achieve better laser eye-safety, lower solar ambient light, higher atmospheric transmission, and negligible interference with Si-based electronic devices and circuits. With SWIR operation wavelength, alternative solutions to Si SPAD are urgently needed because material-wise Si features poor optical absorption for wavelengths beyond 1 μm. Ge-on-Si SPAD using pure Ge as absorption material may be a suitable candidate for SWIR sensing and imaging, and has been investigated in the past decade

by various works [1-5]. While it is CMOS compatible and so promises fabricating low-cost devices integrated with circuits, due to reasons including lattice mismatch between Si substrate and pure Ge as well as other issues, all reported Ge-on-Si SPADs in the literature feature very high DCRs and can only operate at low temperatures at least < 200 K.

In this paper, we report the demonstration of the first high-performing GeSi SPAD operating at room and elevated temperatures. A GeSi SPAD with active area of 15 μm diameter is designed, simulated, and fabricated, targeting a low breakdown voltage below 12 V for low-power operation. Fig. 1 shows the tilted-view scanning-electron-micrograph (SEM) image of the fabricated GeSi SPAD, in which two metal rings are used to bias the cathode and the anode of the device. From the measured IV characteristics, the BV is determined to be around 11 V, which matches the prediction from our numerical simulator very well.

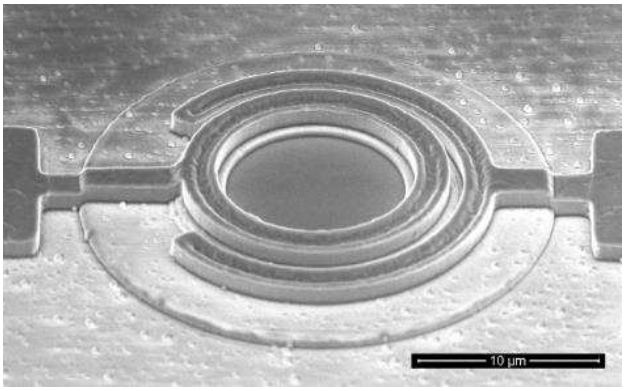


Fig. 1. A tilted-view SEM image of the fabricated GeSi SPAD with active area of 15 μm diameter.

To characterize the DCR and the SPDP of the fabricated GeSi SPAD, gated-mode operation with gate pulse duration of a few ns and gate pulse repetition of a few hundreds of ns is applied, so that a wide range of DCR can be faithfully measured. In Fig. 2 (a), room-temperature DCR and SPDP are measured to be ~10 kHz/μm^2 and ~10 % at a low excess bias (EB) of only 0.5 V, i.e., 4.5% of the BV. The laser wavelength is chosen to be 1310 nm. To the best our knowledge, this is the first DCR and SPDP reported at room temperature from any Ge-based SPADs. DCR and SPDP can be further improved when translating such a technology into back-side illumination (BSI) pixel with smaller active area and thicker absorption layer. To benchmark the GeSi SPAD in this work with the Ge-on-Si SPADs in the literature, we adopt the metric of noise-equivalent power (NEP) using the formula $NEP = \hbar\omega\sqrt{2 \cdot DCR}/SPDP$, and calculate the adjusted temperature required to cool down the referenced devices so that their NEPs are equal to our NEP at 300 K. In Fig. 2 (b), the resultant adjusted temperatures are

at least < 175 K, showcasing the unprecedented performance of our GeSi SPAD. Here we presume that DCR doubles for every 10 K increase in temperature for all devices in comparison, based on the measured value from our GeSi SPAD for temperatures between 20 ºC and 80 ºC.

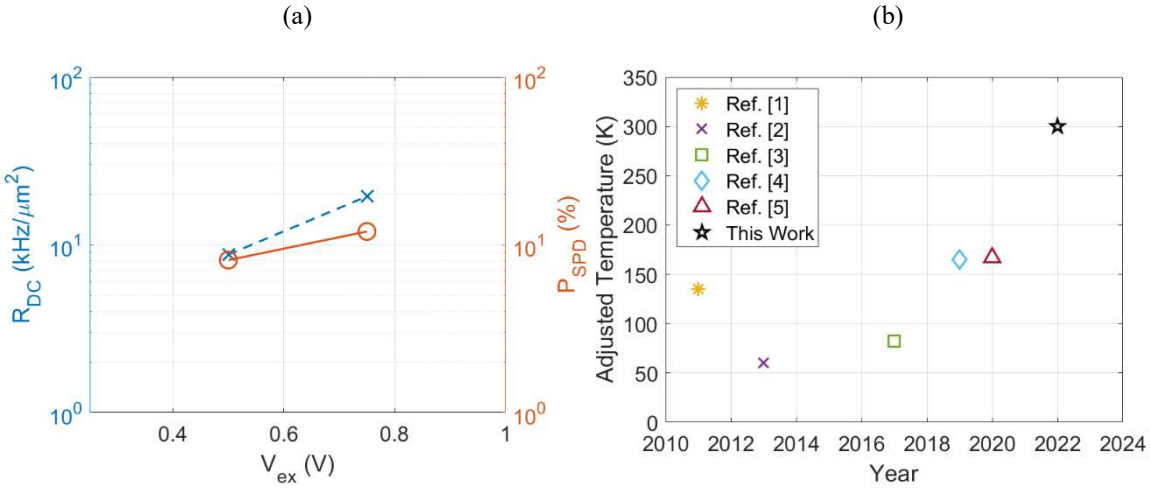
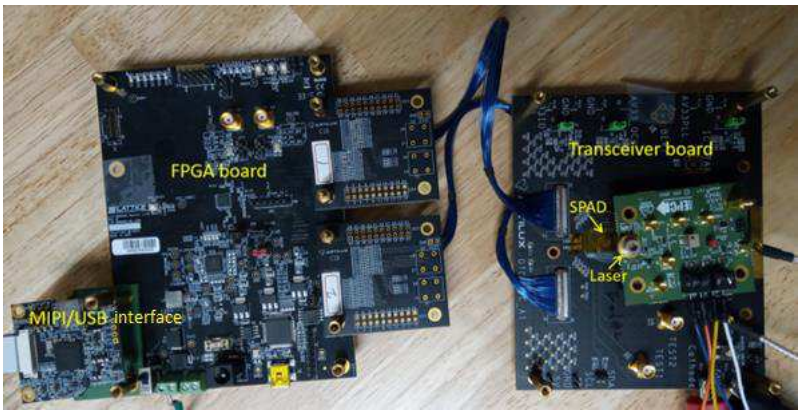


Fig. 2. (a) The measured DCR and SPDP plotted as a function of EB. (b) The adjusted temperatures of the Ge-on-Si SPADs in the literature and the GeSi SPAD in this work shown in chronological order (note the highest operation temperatures of Ref. [1-5] are 200 K, 100 K, 80 K, 125 K, 175 K).

To demonstrate the applicability of our GeSi SPAD for SWIR sensing and imaging, a proof-of-concept ranging demo is carried out and shown in Fig. 3 (a). It consists of a transceiver board, a field-programmable gate array (FPGA) board, and a laptop to display TOF histograms in real-time. On the transceiver board, the transmitter is a 1550 nm laser diode driven by a pulse driver, and the receiver is the GeSi SPAD wired bonded to an application specific integrated circuit (ASIC). The transmitter is positioned closely to the receiver, and no optics, e.g., Tx lens for laser beam collimation and Rx lens for backscattered light collection, are installed. During the experiment, the laser is operated to transmit 200 ps pulses at repetition frequency of 500 kHz and peak power of 20 mW. The TDC and the FPGA are configured to generate each histogram with accumulation duration of 131 ms and bin width of 156 ps. A piece of Kodak gray card, of which the white side is held toward the transceiver board, is used as the target. The collected data are sent for further analyses through a MIPI-to-USB bridge IC. The block diagram of the ranging system is shown in Fig. 3 (b). The ASIC IC is fabricated in a commercial 40 nm CMOS process and interfaces with the SPAD IC through an AQC and a 13-bit TDC designed for baseline resolution of ~1 cm and typical range of ~100 m. Finer resolutions and closer ranges can be obtained by adjusting the phase-locked loop (PLL) clock frequency. A high-speed first-in-first-out (FIFO) port serves as the data buffer to handle the operating speed

difference between the TDC and the FPGA. Finally, the exemplary TOF histograms captured by the ranging system are shown in Fig. 3 (c).

(a)



(b) (c)

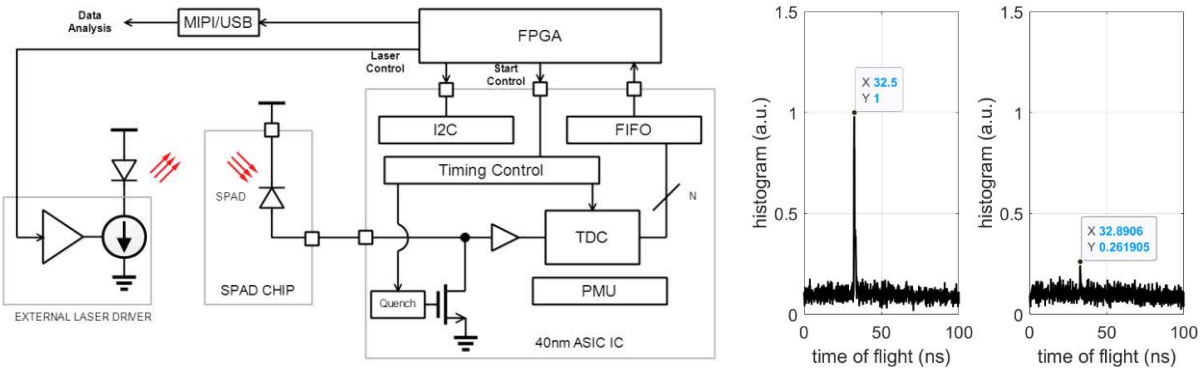


Fig. 3. (a) The ranging system including laser, SPAD, transceiver board, FPGA board, and MIPI/USB interface. (b) Schematic diagram of the ranging system including the 40 nm ASIC. (c) TOF histograms captured when the target is ~3 cm (left) or ~9 cm (right) away from the test board.

To summarize, we have successfully demonstrated the world-first high-performing GeSi SPAD at room and elevated temperatures, and performed a proximity ranging demo. We believe this work will open new possibilities for SWIR sensors and imagers to be applied to the landscape of consumer applications in the near future.

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Germanium on silicon SPAD 32x32 pixel array in 3D-stacked technology for SWIR applications

Y. Benhammou[1], N. Moussy[2], R. Paquet[2], C. Buj[2], O. Saxod[2],
D. Rideau[3], D. Pellissier-Tanon[3], S. Pellegrini[5], F. Calmon[4], D. Golanski[3]

[1]D&FD, STMicroelectronics, Tours, France,[2]CEA-LETI, Minatec Campus, Grenoble, France,
[3]TR&D, STMicroelectronics, Crolles, France email: dominik.golanski@st.com, [4]INL, Université de Lyon, INSA Lyon, France, [5]Imaging Division, STMicroelectronics, Edinburgh, Scotland

***Abstract*— We present a unique integration of a Single Photon Avalanche Diode (SPAD) silicon matrix with a germanium absorber stacked on a CMOS 40nm technology readout circuit. This architecture extends the sensitivity of the silicon SPAD to the Short-Wave Infrared (SWIR). A careful optimization of the process was performed to reduce the dislocations in the germanium epitaxy. The use of a relatively highly doped germanium combined with small dimension area of the pixels lead to a Dark Count Rate (DCR) level contained below 10 kcps (kilo counts per second) at -40°C and 2V excess bias. The light sensitivity at 1300 nm wavelength is maintained at a reasonable level with a Photo Detection Probability (PDP) of 7 %. These results are obtained with a remarkable low dispersion over several thousands of SPADs. A noise equivalent power of 3E-17 W.Hz$^{-1/2}$ is obtained at 1300 nm wavelength and -40°C.**

Keywords— SPAD, SWIR, LIDAR, Germanium, 3D Integration.

I. INTRODUCTION

3-D mapping at medium range distance have found technical solutions with direct or indirect time of flight using silicon detectors. These active illumination techniques work around 940 nm wavelength compatible with silicon sensitivity. Above few tens of meters, high sensitivity or higher illumination power are required. Eye-safety constraints are relieved by more than a factor 10 by extending the spectral range in the SWIR with the LiDAR solutions [1]. Materials such as Germanium [2] [3] and III-V semiconductors InGaAs/InP SPADs [4] [5] can be considered for that purpose.

A controlled noise level can be achieved by using germanium-based detectors with well-Separated Absorption, Charge and Multiplication regions (SACM). The silicon region is used as the multiplication region with a high field PN junction and the germanium region as the absorber [2] [3]. Vines et al [6], reported a high-performance Germanium-on-PiN Silicon SPAD by reducing the electric field in the germanium.

This work reports a fully integrated 3D-stacked 32x32 pixels embedding Ge on Si SPAD device on a CMOS 40nm technology. Dark currents and sensitivity performances are discussed varying the doping level of germanium, excess voltage and operating temperature.

II. SPAD DEVICE ARCHITECTURE

This device is based on an available architecture for silicon SPAD technology [7] with an additional germanium epitaxy and process adaptations (Fig.1). The top tier wafer hosting the SPAD is bonded on a 40nm CMOS technology 12-inches bottom wafer (Fig.2). Each SPAD has a single connection on a 32x32 readout circuit including passive quenching and pulse counting. The pitch of the matrix is 14.5 µm horizontally and 23.5 µm vertically. The top tier is thinned for contact enabling.

The avalanche junction of the SPAD is formed between the PWELL and the deep NWELL implants. It is surrounded by a guard ring realized with an undoped epitaxial layer (EPI) and a shallow trench isolation (STI) (Fig.1). A square cavity less than 1µm deep and a few µm wide is etched in the active silicon. A germanium island is grown inside the cavity by a selective in-situ-doped epitaxy. This area of the cavity is considered for PDP estimation. A 10.5% fill factor is obtained at the pitch of the matrix.

Boron in-situ doping of the germanium is assessed at two concentrations: a highly doped layer and a lowly doped layer. Surface passivation and top contact of germanium are done with a surface boron implantation. An additional Ring implant with boron aims to inhibit the periphery of the cavity where defects and the shape of the cavity can cause early breakdown effects. The second role of this ring is to prevent the leakage of photogenerated carriers at the periphery of the diode.

III. OPERATING PRINCIPLE

Process and electrical simulations are performed with the Synopsys Sentaurus commercial suite. A cartography of the doping scheme of the device is shown Fig.1. While increasing reverse bias on the PN junction, the depletion region extends through the PWELL, the Ge-Si interface and finally into the germanium. Charges can flow through the device above the Punch-Through polarization (Vpt) when the depletion reaches the Ge-Si interface. The doping profiles and thickness of PWELL are tuned in order to obtain a Breakdown Voltage (BV) close to the polarization Vpt. Excess voltage, variations of PWELL dose and Ge doping modify the electric field entering into the germanium (Fig.3) and permit to explore its incidence on sensitivity and dark current.

Technology computer-aided design (TCAD) simulations were performed with the introduction of defects at the heterojunction and in the germanium bulk at a density level proposed by [8] [9]. As expected, higher germanium doping prevents the expansion of the depletion region and reduces the dark currents. The level of these currents and effect of Ge doping on the collection of photogenerated carrier can only be evaluated experimentally.

IV. CHARACTERIZATION RESULTS

A. Currents on stand alone SPAD

Current behavior strongly depends on the doping level of the PWELL as illustrated in Fig.4 at room temperature. The punch through and the breakdown voltage evolution with the PWELL dose is extracted in Fig.5. Two wafers show the closest Vpt≈18V and BV≈20V. One wafer has a high doped germanium, the second one has low doped germanium.

Fig.6 shows the SPAD current-voltage measurements on two different locations on the wafers. The variation Vpt and BV is attributed to a slow modulation of the thickness of PWELL over the surface. The dark currents above Vpt only differ by a factor of 2 between the two wafers. The current density is approximately 8E-5 A.cm-2 over the surface of the germanium cavity at room temperature.

B. 32x32 SPAD array

The 32x32 readout circuit gives access to the count per second (cps) of each individual pixel. The high voltage (VHV) is common to all SPADs and adjusted for each circuit using the median voltage of avalanche detection of the pixels. In order to suppress residual cross talk, only ¼ of the SPADs are biased at the same time above BV during measurements. SPADs with high count rates are also disabled.

In Fig.7 and 8, the thin dot-line plot displays the median, min and max values statistics of each device with 1024 SPADs. At -40°C, the DCR is limited below 10 kcps and the PDP at 1300 nm wavelength reaches 7% at 2V excess bias. The 1-sigma uniformity of BV is less than 80 mV inside the devices. The evolution of the breakdown voltage in temperature measured at +18mV/°C follows the standard behavior of silicon SPAD. The progression of dark counts with temperature follows an Arrhenius law with an activation energy Ea=0.75 eV close to the gap of germanium.

Fig.9 and 10 show the performances of both the lowly and highly doped germanium. As expected DCR is better with a higher doping and also sensitivity is almost 2 times better. These good results are relatively free of artifacts with less than 1% afterpulses and 7 ns pulse duration up to an excess bias of 2V. The afterpulse rate is measured via a histogram of inter-arrival time of dark count pulses (Fig.11). This very low rate corresponds to silicon behavior. Germanium is probably only weakly involved in this effect.

Around 1% PDP sensitivity is measured at 1550nm due to the natural absorption cutoff of germanium and the thickness used for this demonstration (Fig.12). The absorption at 1300 nm wavelength through 300 nm thick germanium is estimated around 20% and the PDP is measured around 7%. Ignoring the reflections inside the 3D stack, these results show that the internal efficiency of the detector is around 35%. The rest of photogenerated carriers are recombined inside the germanium layer and at the heterojunction, or fail to generate an avalanche.

The sensitivity to light increases with temperature from 7% at -40°C to 11% at 0°C, as observed in Fig.13. The driving contribution to this evolution has not yet been identified, among the possible temperature effects of light absorption [10] [11], impact ionization and heterojunction transfer.

Jitter measured on several SPADs using a 30 ps pulsed laser at 1310 nm wavelength (PicoQuant) shows a diffusion tail that varies little with excess voltage (Fig.14). Full width at half maximum (FWHM) and at 1% of maximum (FWM100) are respectively 140 ps and 1100 ps at 2V excess bias and -40°C (Fig.15). These low jitter values most probably result from the low thickness of the germanium layer.

The Fig.16 shows a comparison of the Noise Equivalent Power (NEP) between several publications including InGaAs SPAD technology [6][12][13][14]. The $\mathrm{NEP} = \mathrm{h}\nu * \frac{\sqrt{2.DCR}}{\mathrm{PDE}}$ is calculated with the Photo Detection Efficiency (PDE) defined over the pitch of the matrix. The very good result on this figure of merit with a remarkable improvement in temperature is obtained thanks to a minimized DCR noise and by a very contained afterpulsing.

Overall pixel performance can be improved by the addition of light sensitivity boosters such as higher Ge layer thickness, improved Fill Factor with smaller readout circuit and improved light collection and confinement by the use of micro-lenses and the engineering of light reflections. DCR can be further reduced with Germanium cavity area reduction and doping optimization.

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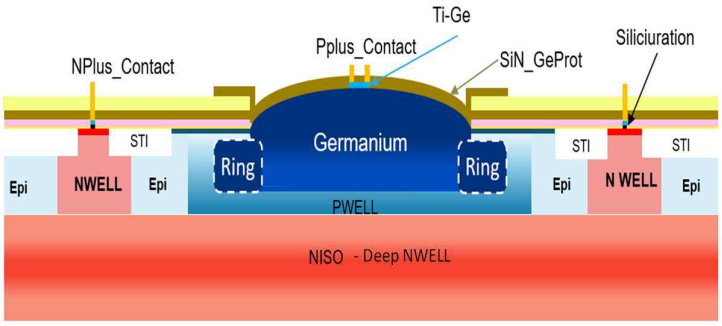

Fig. 1. Architecture of the SPAD with a total dimension of 11.5x11.5 µm²

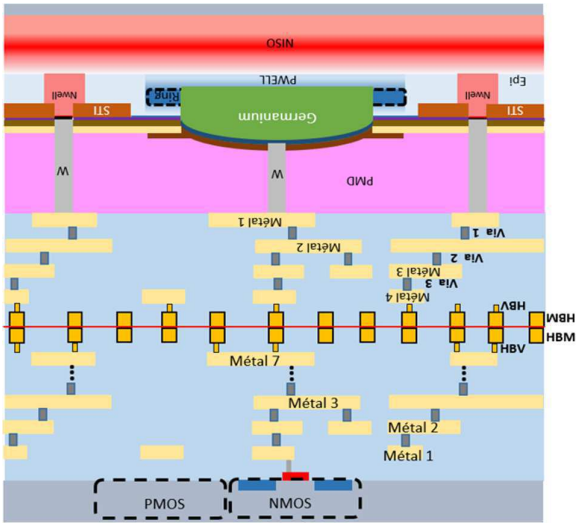

Fig. 2. 3D Integration of the SPAD

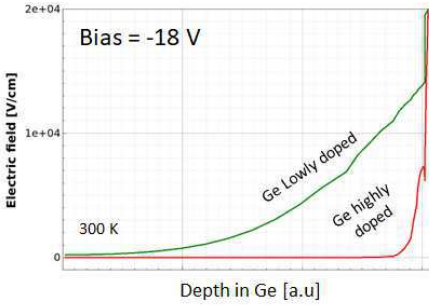

Fig.3 Simulation of electric field at -18V in germanium at two levels of doping

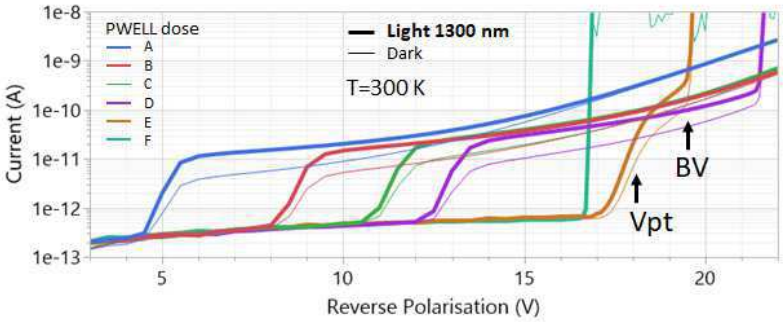

Fig. 4. Current measurement versus bias in dark and under illumination for different PWELL dose.

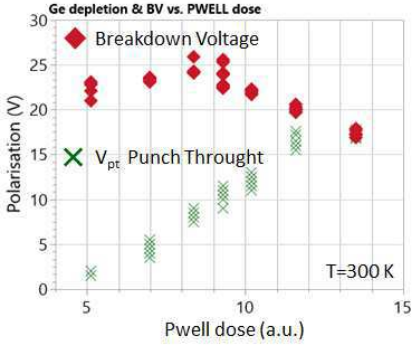

Fig. 5. Measured BV and Vpt versus PWELL dose

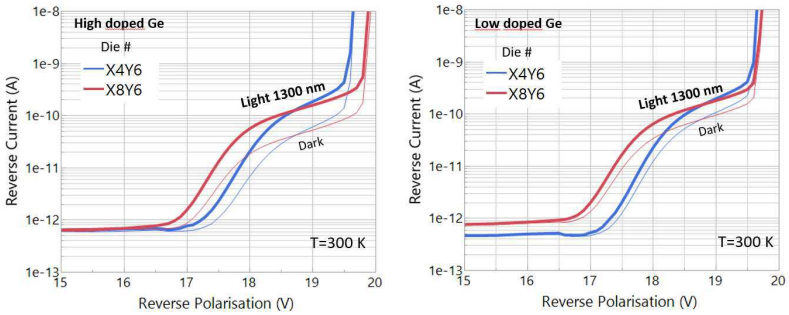

Fig. 6. Dark and light currents on two different SPAD on high doped (left) and low doped (right) germanium wafer

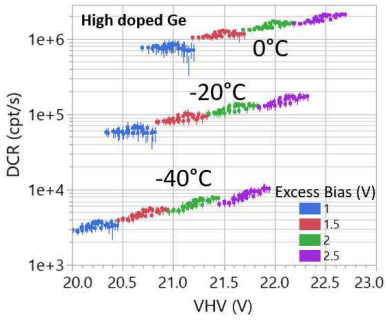

Fig. 7. DCR vs reverse voltage and temperature on high doped germanium wafer

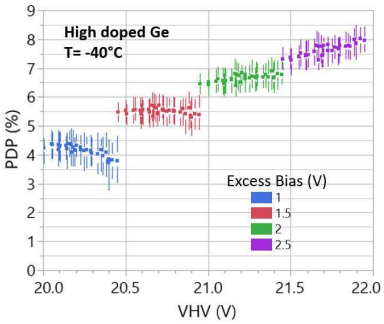

Fig. 8. PDP versus reverse voltage at -40°C

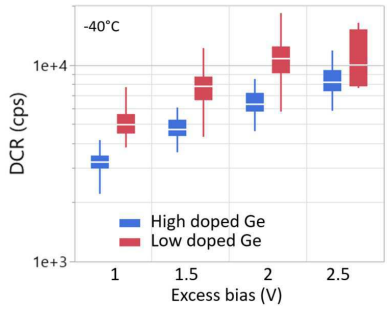

Fig. 9. Comparison of DCR high and low doped germanium (box plot statistics with quantile min., 25%, 50%, 75%, max.)

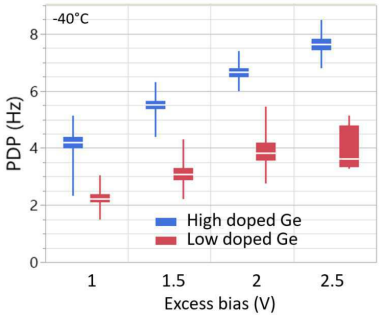

Fig. 10. Comparison of PDP for high and low doped germanium

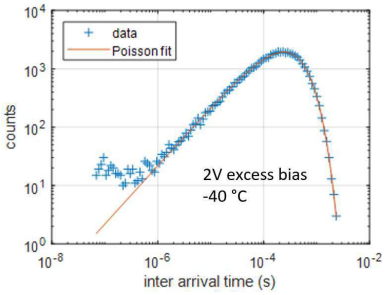

Fig. 11. Histogram of inter-arrival time with Poisson fit at a DCR of 8 kcps

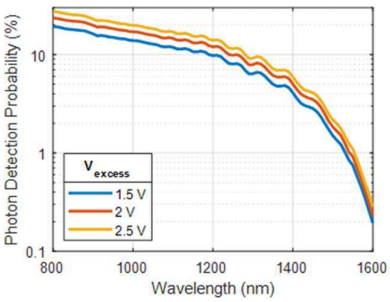

Fig. 12. Sensitivity (PDP) versus wavelength

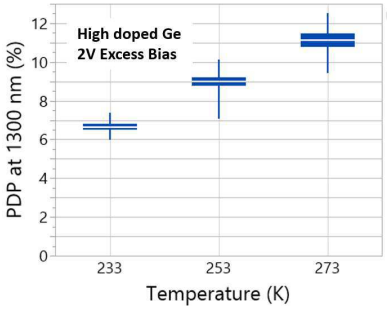

Fig. 13. Evolution of PDP with temperature of the full statistic high Ge doped wafer

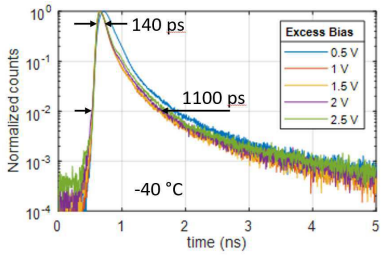

Fig. 14. Jitter measurements at 1300 nm on a SPAD at different excess voltage

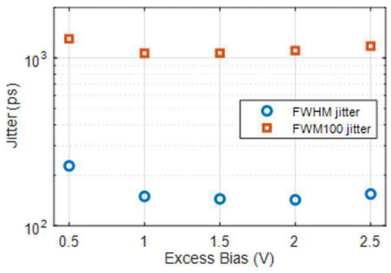

Fig. 15. Jitter at 1310 nm, FWHM and FWHM100 versus Excess bias

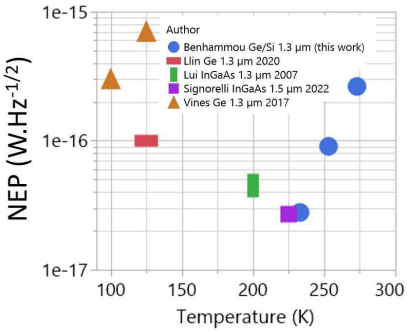

Fig. 16. Noise equivalent power for Ge and InGaAs publications

Doping Engineering for PDP Optimization in SPADs Implemented in 55-nm BCD Process

Feng Liu[1], Claudio Bruschini[1], Eng-Huat Toh[2], Cancan Wu[2], Ping Zheng[2], Louis Lim[2], Elgin Quek[2], Myung-Jae Lee[3], and Edoardo Charbon[1]

[1]EPFL, Neuchâtel, Switzerland [2]GlobalFoundries, Singapore [3]KIST, Seoul, South Korea
Rue de la Maladière 71b, Neuchâtel 2002, Switzerland
Email: feng.liu@epfl.ch, Phone: +41 782322787

***Abstract*—**We introduce a new family of single-photon avalanche diodes (SPADs) with an enhanced depletion region integrated in a 55-nm Bipolar-CMOS-DMOS (BCD) technology. We demonstrate how to systematically engineer doping profiles in the main junction and in deep p-well layers to achieve high sensitivity and low timing jitter. To demonstrate the technique, a family of SPADs was designed and fully characterized. Sensitivity spectra was enhanced at long wavelengths, achieving up to 41.3% at 640nm and 22.3% at 850nm. Timing jitter was reduced to less than 100ps (FWHM). The proposed SPADs are suitable to low-pitch, large-format image sensors for high-speed time-resolved applications.

I. Introduction

Single-photon avalanche diodes (SPADs) in monolithic CMOS technologies have received great attention in recent years for scientific, industrial, and consumer applications, such as time-of-flight (TOF) sensing, LiDAR, low-light photon counting imaging, medical or biomedical imaging, quantum random number generation (QRNG) [1]. However, CMOS SPADs using an advanced technology tend to have limited sensitivity, measured as photon detection probability (PDP), often peaking at 450-550nm. In these SPADs, PDP is usually poor in near-infrared (NIR) spectral range, due to narrow depletion region.

Significant improvements in NIR and an overall wide spectral range has recently achieved in submicron CMOS technologies [2]-[6], however fill factors are often low. The use of electrical microlensing [7], also known as charge focusing [8], has been shown to be useful to improve PDP performance. Electrical microlensing consists of forcing photo-generated carriers drift towards the multiplication region by gradual doping profile or electric field. However, wide and deep depletion regions appear to be the most effective means to improve NIR PDP. For instance, Webster *et al.* have achieved over 40% PDP from 410nm to 760nm at high excess bias by burying the multiplication region in 130nm CMOS technology. Niclass *et al.* have used fully depleted SPAD structure in 180nm CMOS technology achieving a PDP of 64.8% at 610nm and 24% at 850nm at moderate excess bias.

Here we report on a new family of SPADs with a pitch of 8.5µm characterized by different depletion regions. We first demonstrate how to systematically engineer the doping of the main junction and all deep p-well layers, and then fully characterize the impact of doping engineering in small SPADs. The proposed SPAD1 and SPAD2 show less than 50ps timing jitter at 5V excess bias voltage, while SPAD3 shows enhanced PDP in the NIR spectral range, and it maintains a low timing jitter at 3V excess bias voltage.

II. SPAD Structure

Fig. 1 shows the cross-section of the frontside-illuminated SPAD family. The SPAD is based on a shallow N-well (NW) and P-well (PW) junction. A pitch of 8.5µm was implemented for the entire family. All the SPADs were designed and realized in a round shape with an avalanche diameter of 4.4µm, achieving a fill factor of 21%. Based on the achieved results, we expect to achieve higher fill factor in future generations. Fig. 2 shows the doping profile as a function of depth below the surface. The substrate features a gradient of p-type doping in the epitaxial layer, and the SPAD incorporates three different deep P-well (DPW) layers below the junction.

Fig. 3 shows simulations of the relative electric field as well as the depletion layer boundaries. The avalanching junction is engineered through the shallow NW and PW layers and optimized to achieve a high avalanche gain and wide depletion region. With different DPW layers, the depletion region is well defined in depth. The photo-generated carriers in the depletion region can thus quickly drift upward towards the avalanching junction and ensure enhanced PDP in NIR.

III. Results and Discussion

The static current/voltage curves of the proposed SPADs were measured using a semiconductor analyzer, revealing extremely low dark current levels in the pA range for all three variants. The current-voltage curves with illumination are shown in Fig. 4. With different DPW layers, the corresponding breakdown voltages are 17.1, 20.6, and 23.0 V, respectively. As expected, the breakdown voltage is related to both the main junction and the DPW layers for miniaturized fully depleted SPAD. Besides, it is clearly shown that SPAD2 and SPAD3 achieve lower photo-current above breakdown. Fig. 5 shows the breakdown voltage as a function of temperature from -40ºC to

60ºC. The extracted temperature coefficients are 16.7, 44.5, and 56.5mV/ºC, respectively. Temperature coefficients are larger for thicker depletion regions.

The dark count rate (DCR) of 8 samples for each SPADs was measured at room temperature. Fig. 6 shows the median DCR as a function of excess bias voltage. The median DCR of SPAD1 is 132cps at 3V and 290cps at 5V excess bias voltage. DCR can be further reduced through optimization of the guard ring. SPAD2 shows the best DCR performance, with a median DCR of 62.3cps at 3V and 132.2 cps at 5V excess bias voltage. The median DCR of SPAD3 is 474.2cps at 3V excess bias voltage. The temperature dependence of DCR is shown in Fig. 7 for 3V excess bias voltage, whereas SPAD2 and SPAD3 show a strong temperature dependence, indicating that trap-assisted thermal generation is the main source of noise.

Fig. 8 shows the measured PDP from 400nm to 960nm with a step of 10nm for all the SPADs. With different DPW layers, it is clearly shown that the peak PDP migrates from 450nm, to 540nm, and finally settles to 640nm. SPAD1 achieves a peak PDP of 48.9% at 450nm, and 6.7% at 850nm at 5 V excess bias voltage. SPAD2 achieves a peak PDP of 32.4% at 540nm, and 10.7% at 850nm at 5V excess bias voltage. Thanks to the wider depletion region, SPAD3 shows a high PDP over a wide spectral range, with peak PDP of 41.3% at 640nm, and 22.3% at 850nm at 3V excess bias voltage. This broad spectral response from visible to NIR holds great potential for a variety of applications, including time-of-flight imaging, low-light-illumination imaging. The peak PDP as a function of excess bias voltage is shown in Fig. 9. The peak PDP of SPAD3 shows the strongest dependence on excess bias voltage.

A dedicated printed circuit board equipped with a fast comparator was utilized to evaluate timing jitter. A low threshold voltage was applied to detect the SPAD signal at the onset of the avalanche phenomenon. Fig. 10 shows timing jitter at 3V excess bias voltage with an 850-nm laser source. The evolution of jitter as a function of excess bias voltage is shown in Fig. 11. A timing jitter of 42, 70, and 96ps (FWHM) is achieved at 3V excess bias voltage, respectively. Timing jitter at the same excess bias voltage strongly increases with the expansion of the depletion region.

IV. State-of-the-Art Comparison

Fig. 12 shows the PDP and timing jitter comparison of the proposed SPADs with the previously reported N-on-P type SPADs in CMOS technology. The SPAD1 and SPAD2 show less than 50ps timing jitter at 5V excess bias voltage. The SPAD3 shows a high PDP at 850nm, while keeping a low timing jitter at 3V excess bias voltage. Table 1 shows the overall performance of the developed SPADs and a comparison with the state-of-the-art.

V. Conclusions

We demonstrate the role of doping engineering to widen the depletion region in small SPADs with a pitch of 8.5µm implemented in a 55-nm BCD process. To demonstrate it practically, a family of SPADs was designed, realized, and fully characterized in this technology. The doping profiles of the avalanching junction layers were optimized to achieve red- and NIR-enhanced sensitivity. Experimental evaluation of the proposed SPADs revealed that the PDP peak wavelength can be improved with a wider and deeper depletion region. SPAD3 was designed to achieve this goal. It shows a high PDP over a wide spectral range, with a peak PDP of 41.3% at 640nm, and 22.3% at 850nm, and the timing jitter 96ps at 3V excess bias voltage. The technique is suitable for small-pitch SPADs and large-format image sensors, with multi-megapixel resolution, both operating in frontside- and backside-illuminated modes.

Acknowledgment

The authors would like to thank GlobalFoundries for fabricating the devices in 55-nm BCD technology.

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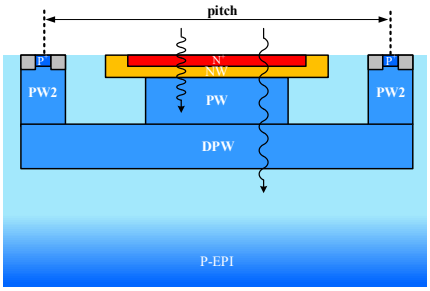

Fig. 1. Simplified cross-section of the SPAD. The structure is based on shallow NW and PW. Three different DPW layers are implemented. All 3 SPADs have same drawn avalanche area and pitch.

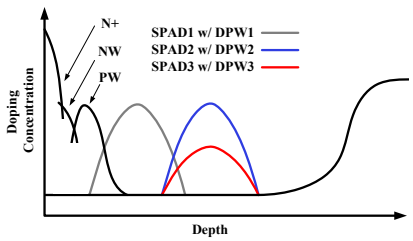

Fig. 2. The simplified doping profile versus distance from silicon surface. The DPW1-3 layers are used in SPAD1-3, respectively.

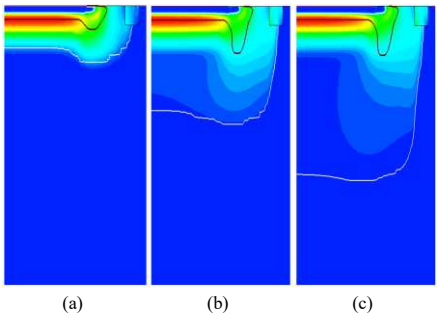

Fig. 3. Simulation results depicting the electric field as well as the depletion layer boundaries for SPAD1 (a), SPAD2 (b), and SPAD3 (c) at 3V excess bias voltage. The junction is engineered to achieve a wide depletion region.

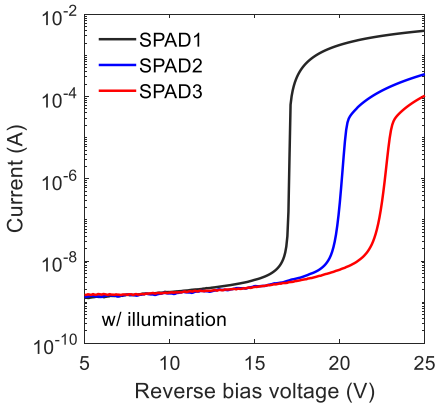

Fig. 4. SPADs current as a function of reverse bias voltage with illumination.

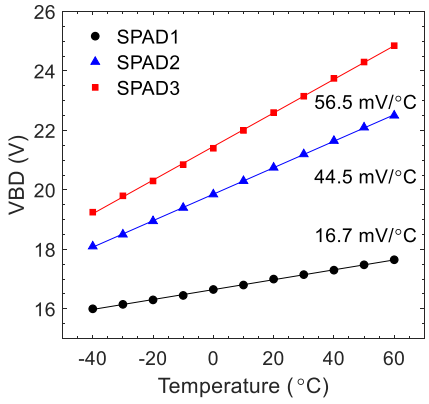

Fig. 5. Breakdown voltage as a function of temperature for 3 different SPADs.

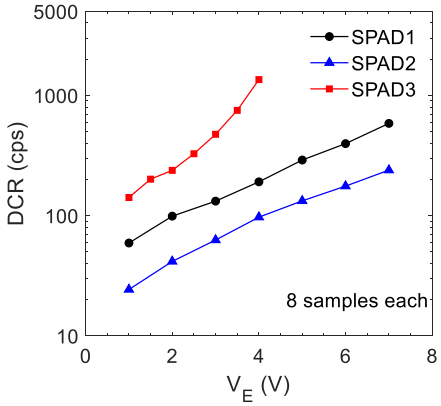

Fig. 6. Median DCR at room temperature. The data is obtained by measuring 8 dies. The corresponding median DCR is 132, 62.3, and 474.2cps at 3V excess bias voltage.

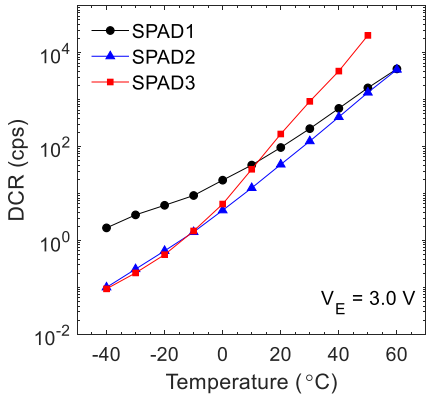

Fig. 7. Temperature dependence of DCR for 3 different SPADs. Measurements were taken from one SPAD sample each from -40 ºC to 60 ºC.

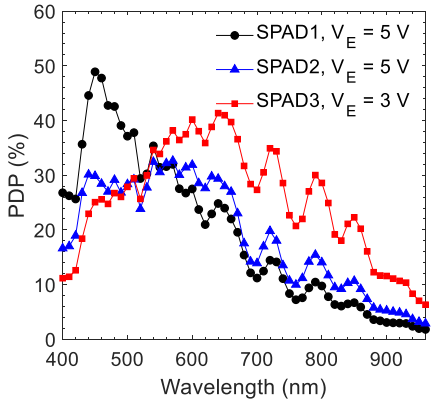

Fig. 8. PDP as a function of wavelength for 3 different SPADs.

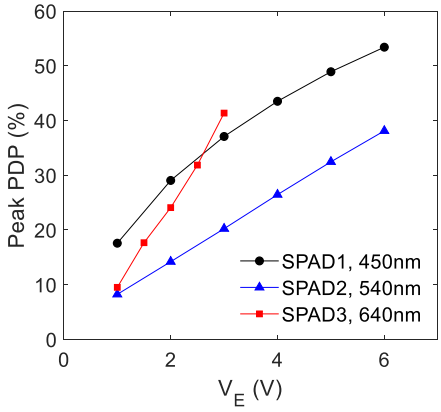

Fig. 9. PDP as a function of excess bias voltage at the peak wavelength for 3 different SPADs.

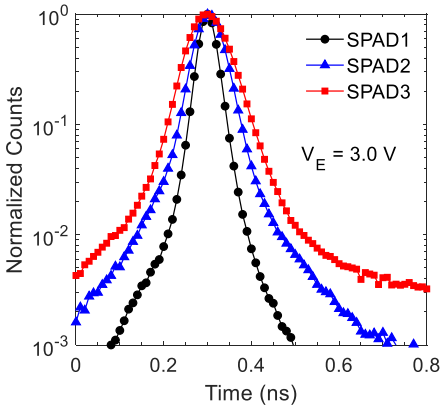

Fig. 10. Timing jitter response for an 850 nm laser at 3V excess bias voltage. The jitter of the laser is 32ps.

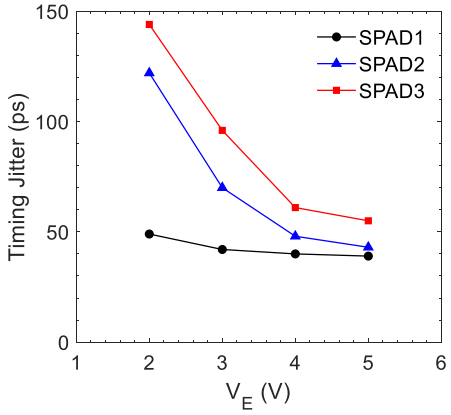

Fig. 11. Timing jitter (FWHM) as a function of excess bias voltage.

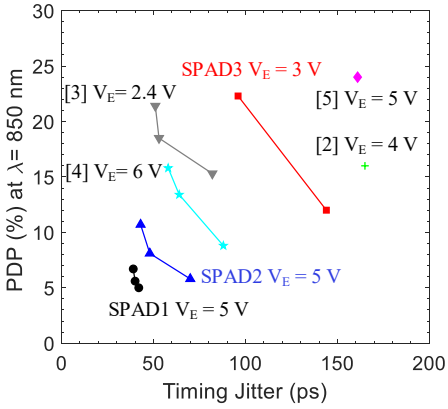

Fig. 12. Performance comparison of the N-on-P SPADs in monolithic CMOS technologies: PDP at 850nm versus timing jitter at similar excess bias voltages.

Table. 1 Performance summary and comparison with N-on-P front-side illuminated SPADs in CMOS technology

Parameter	This work (SPAD 1)	This work (SPAD 2)	This work (SPAD 3)	[2]	[3]	[4]	[5]	[6]
Structure	Shallow NW/PW	Shallow NW/PW	Shallow NW/PW	N+/PW	Deep NW/epi	Deep NW/epi	Deep NW/PW	Deep NW/PW
Technology (nm)	55	55	55	180	90	130	180	180
Pitch (μm)	8.5	8.5	8.5	N/A	N/A	N/A	25	N/A
Avalanche area (μm^2)	15.2	15.2	15.2	78.5	32.1	50.2	206.9	220
Fill Factor (%)	21	21	21	N/A	N/A	N/A	33.1	35
VBD (V)	17.1	20.6	23.0	19.7	14.9	20	20.5	20.0
VE (V)	5	5	3	4	2.4	6	5	5
DCR (cps/μm^2)	19.1	8.7	31.2	30	~4.6	0.36 (V_E = 2 V)	0.6	1.7
PDP Peak (%)	48.9 @450 nm	32.4 @540 nm	41.3 @640 nm	36 @600 nm	44 @690 nm	45.2 @560 nm	64.8 @610 nm	47 @570 nm
PDP (%) @ 850 nm	6.7	10.7	22.3	16	21.4	15.8	24	20
PDP (%) @ 940 nm	2.4	3.7	8.3	N/A	10.1	5.7	8.8	9.7
Afterpulsing probability (%)	3.9[a]	4.5[a]	4.7[a]	50[a]	0.38	0.98	0.49	N/A
Dead time (ns)	100[a]	100[a]	100[a]	750[a]	23	35	24.9	N/A
Timing Jitter (ps) FWHM	39 @850 nm	43 @850 nm	96 @850 nm	165 @790 nm	51 @470 nm	58 @654 nm	161 @635 nm	N/A

[a] This value is significantly overestimated with huge parasitic capacitance due to the lack of integrated circuit.