

A 3.06 μm SPAD Pixel with Embedded Metal Contact and Power Grid on Deep Trench Pixel Isolation for High-resolution Photon-counting

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I. Introduction

Single photon avalanche diode (SPAD) pixels have been developed for time-of-flight (ToF) range image sensors [1–3] and photon counting image sensors [4–6]. Recently, the SPAD pixel size has been reduced to 5 μm or smaller to improve the pile-up problem and resolution of the SPAD-based image sensors [7–9]. However, the dark count rate (DCR) and photon detection efficiency (PDE) in smaller SPAD pixels are significantly worse compared to pixels larger than 6 μm [5,10,11]. This is due to edge breakdown (EBD) in the high electric field region at the pixel edge or the small avalanche region. The latest work can address this issue, achieving over 80% PDE and below 5 cps (count per second) DCR with a 3.0- μm -pitch SPAD pixel [12]. However, the crosstalk is higher compared to a 6- μm SPAD pixel due to the small pitch. Additionally, the power consumption and voltage drop with SPAD multiplication must be improved in high-resolution photon-counting image sensors with large array of such small pixels. In this paper, we present a 3.06- μm -pitch SPAD pixel using the embedded metal contact and power grid on two-step deep trench isolation in the pixel to suppress the EBD, the crosstalk, and the voltage drop, and to maintain the PDE and the DCR simultaneously [13]. Additionally, we demonstrate a reduction in charge per event (CPE) with SPAD multiplication by integrating a polysilicon resistor on the SPAD pixel.

II. Pixel structure

Figure 1(a) shows a schematic diagram of the developed 3.06- μm -pitch SPAD pixel. One of the contacts in the pixel is embedded, with the embedded metal contact on the two-step deep trench isolation. This increases the vertical distance between the two contacts, suppressing both EBD and DCR. The metal filling in the deep trench acts as an optical shield, contributing to optical crosstalk suppression through avalanche multiplication. This two-step trench decreases the total width by integrating two functions of the embedded contact and metal shield into one trench structure. Additionally, the metal acts as low

impedance metal wiring in the SPAD array, as shown in Fig. 1(b). This “embedded power grid” reduces the voltage drop across the wiring even for a significant multiplication current in a large SPAD array and under high light illumination conditions.

A polysilicon resistor, R_k , is integrated on the pixel by inserting it in series with the SPAD and quenching circuit, as shown in Fig. 1(c), and can reduce the amplitude of the voltage swing at the V_{in} node, resulting in SPAD multiplication and contributing to CPE reduction. Figure 1(d) shows a transmission electron microscope (TEM) image of the fabricated 3.06- μm -pitch SPAD pixel. The embedded metal contact and the polysilicon resistor on the pixel are successfully integrated.

III. Pixel potential design

Figure 2 shows the distribution of the electric field on the avalanche multiplication region in the pixel, simulated with the pixel structure using TCAD simulation. Figure 2(a) shows the electric field based on the same design concept for a SPAD pixel larger than 6 μm . The electric field on the pixel edge is high, and edge breakdown can occur in this basic design

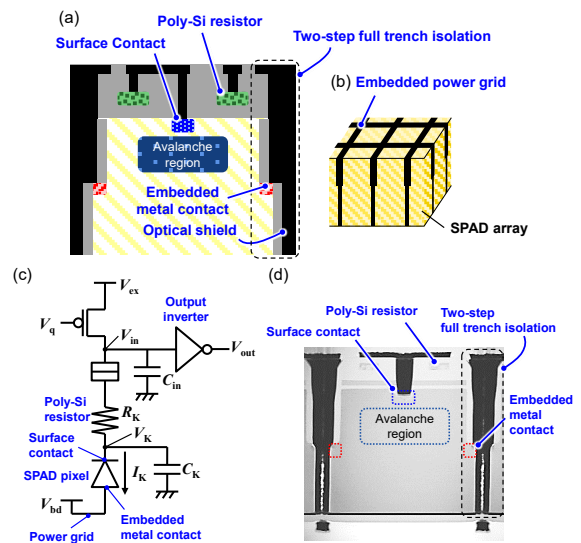


Figure 1. (a) Schematic of 3.06 μm SPAD pixel with embedded metal contact on two-step deep trench pixel isolation and (b) embedded power grid in SPAD array. (c) Circuit diagram for SPAD quenching circuit with polysilicon (Poly-Si) resistor. (d) Cross-sectional TEM image of the 3.06 μm SPAD pixel.

even with the embedded metal contact. We optimized the potential design to decrease the size and increase the depth of the avalanche multiplication region, as shown in Fig. 2(b), resulting in the reduction of the electric field on the pixel edge.

IV. Measurement results of the pixel characteristics

Figure 3 shows a prototype for a proof-of-concept of the 3.06- μm -pitch SPAD pixels. The back-illuminated 3.06- μm -pitch 640 x 1056-pixel array is stacked on a 12.24- μm -pitch 160 x 264 photon counting circuits array with a 14-bit counter via Cu-Cu connections.

Figure 4(a) shows the photon-counting operation with increasing SPAD applied voltage ($V_{\text{ex}} - V_{\text{bd}}$). The counting operation starts at approximately 22.4 V, demonstrating that the 3.06- μm -pitch SPAD pixel successfully works as a photon-counting pixel. The median breakdown voltage (V_{bd}) of the pixel can be calculated as 20.9 V with 1.5 V of the threshold voltage (V_{th}) in the output inverter. Figure 4(b) shows the variation of the V_{bd} through the whole pixel array. The variation is 72 mV, which is less than 100 mV, thus successfully demonstrating stable operation of the 3.06- μm -pitch pixel array.

Figure 5 shows the measurement results of DCR with the basic and optimized potential designs from Fig. 2. The DCR is 15.8 cps at 25 $^{\circ}\text{C}$ with the optimized design and 313 cps with the basic design.

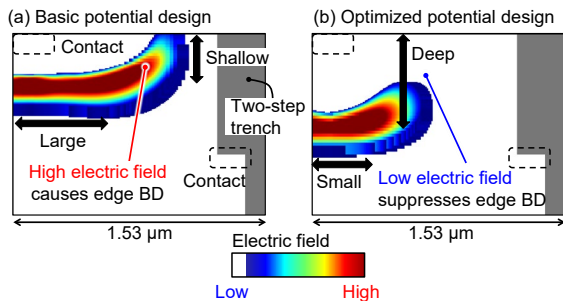


Figure 2. Contour plot of electric field on multiplication region estimated by TCAD simulation with (a) basic potential design and (b) optimized potential design.

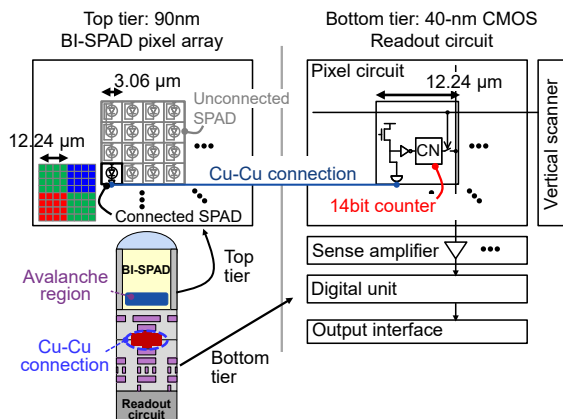


Figure 3. Implementation of prototype for proof-of-concept of the 3.06- μm -pitch SPAD pixels.

The DCR in the optimized design is improved by a factor of 10 compared to the basic design. This result shows that the optimized design can successfully reduce the electric field on the pixel edge, as estimated with the potential simulation in Fig. 2.

Figure 6 shows a measured PDE at various wavelengths. The pixel array of the prototype has a Bayer array of on-chip color filters, and the PDE is measured through each color filter. The peak PDE obtained through the green color filter is 57% with 3 V of V_{ex} . This can be achieved by optimizing the potential slope in the SPAD pixel for electron transfer [14].

Figure 7 shows the measurement results of crosstalk probability with and without full trench isolation. For the crosstalk measurement, a special pixel connection is used where adjacent 3.06- μm -pitch 3×3 pixels are connected to the 12.24- μm -pitch photon counting circuit by metal wiring. Figure 7(a) shows that the crosstalk probability is less than 0.4% with the two-step full trench isolation, while Fig. 7(b) shows that the

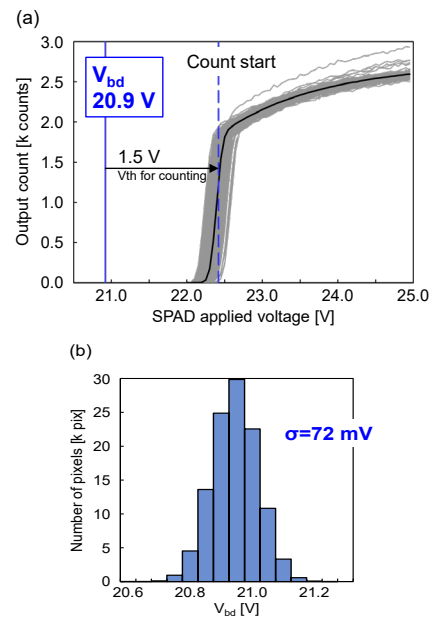


Figure 4. Measurement results of SPAD breakdown operation V_{bd} and its variation at 25 $^{\circ}\text{C}$.

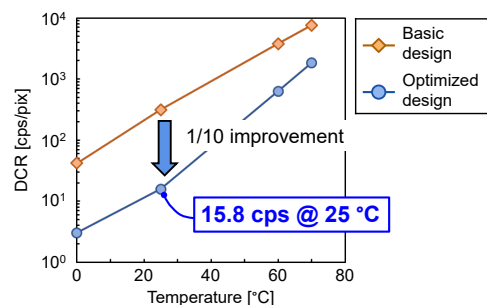


Figure 5. Measurement results of DCR at 25 $^{\circ}\text{C}$ and 3 V of V_{ex} with the two different avalanche potential designs depicted in Fig. 2.

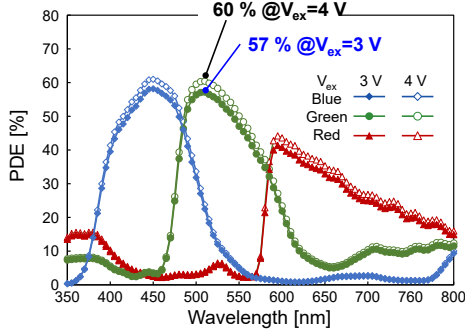


Figure 6. Measurement results of PDE at 25 °C and 3 V and 4 V of V_{ex} .

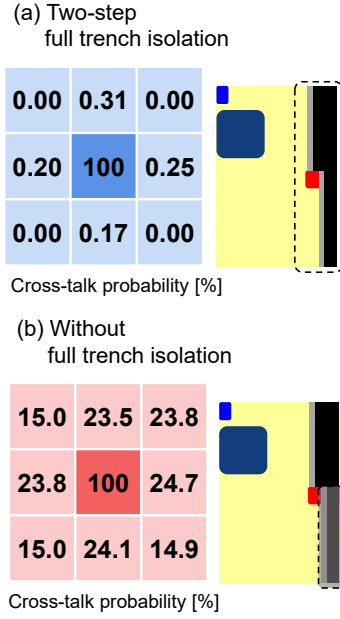


Figure 7. Measurement results of crosstalk probability at 25 °C and 3 V of V_{ex} (a) with and (b) without full trench isolation.

crosstalk probability is greater than 20% without the full trench isolation under the embedded contact. These results highlight the advantage of the two-step full trench isolation, where the embedded metal contact is combined with the full trench isolation.

A color image was successfully captured with only a few defects by using the prototype 3.06- μm -pitch SPAD pixel array as shown in Fig. 8.

V. CPE reduction with polysilicon resistor

The polysilicon resistor on the SPAD pixel can reduce CPE Q_{CPE} with SPAD multiplication using the following equation:

$$Q_{CPE} = C_K V_{ex} + C_{in}(V_{ex} - R_K I_K) \quad (1)$$

Here, C_K is the capacitance at the SPAD cathode before the polysilicon resistor, and C_{in} is the total parasitic capacitance after the resistor to the input node of the output inverter. R_K is the resistance of the polysilicon resistor, and I_K is the current at the SPAD cathode. C_{in} is much larger than C_K because of the Cu-Cu connection and the metal wiring in the CMOS

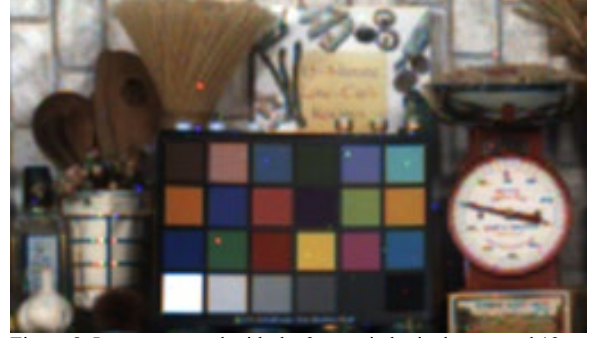


Figure 8. Image captured with the 3- μm -pitch pixel array and 12- μm -pitch photon counting circuit.

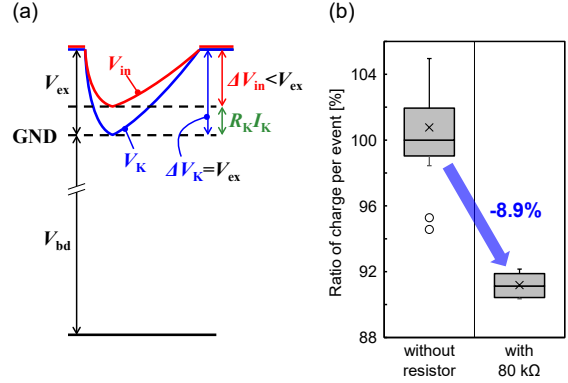


Figure 9. (a) Schematic potential diagram of V_K and V_{in} with SPAD multiplication. (b) Ratio of CPE with 80 k Ω resistor to those without the resistor. The median of the CPE without resistor is 100%.

circuits, and it dominates the CPE. The contribution of C_{in} can be reduced with R_K because the amplitude of the voltage swing at the input node of the inverter (ΔV_{in}) by SPAD multiplication is reduced by the voltage drop with R_K and I_K , as shown in Fig. 9(a). Figure 9(b) shows the measurement results of the ratio of the CPE with an 80 k Ω polysilicon resistor to those without the resistor. The CPE decreased by 8.9% with the resistor.

VI. Conclusion

Table I and Fig. 10 show a comparison of the pixel characteristics of this work with those of previous works. The PDE obtained in this work is significantly higher than that of previous works with 5- μm -pitch or smaller pixels[7–9], while the DCR is comparable to that of previous works with 6- μm -pitch pixels [5,10,11]. The PDE and DCR are worse than those with 3.3- or 3- μm -pitch pixels [12], while the crosstalk is lower than those of [12]. This is because of the full trench isolation with embedded metal and the extension of the metal over the silicon surface, as shown in Fig. 1(a) and (d). Additionally, the integration of a power grid and the polysilicon resistor on SPAD pixels can contribute to a reduced voltage drop in anode power supply and reduced power consumption with SPAD multiplication, respectively, in a large SPAD pixel array for a high-resolution photon-counting image sensor.

References

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Table I. Characteristics comparison with previous works.

	Unit	[5]	[10]	[11]	[7]	[8]	[9]			[12]			This work
Pixel pitch	μm	6.12	6	6.39	5	3	4	3	2.2	3.3	3.0	2.5	3.06
Array size	-	160 X 264	N/D	2072 X 1548	N/D	4 x 4	4 x 4			N/D			160 X 264
Technology	-	BI-3D 90 nm	BI-3D 90 nm	BI-3D 90 nm	FI	FI 130 nm	FI 180 nm			BI-3D 90 nm			BI-3D 90 nm
V _{bd}	V	N/D	22	30	N/D	15.8	22.1	23.6	32.35	19	19	18	20.9
V _{ex}	V	3	3	2.5	5.8 ^{*3}	1.2	6	6	6	3	3	3	3
Peak PDE	%	58	69.4 ^{*1}	69.4	12 ^{*2*3}	6 ^{*3}	14.2	5.6	2	82.5	78.3	76.1	57
DCR @25°C	cps	35.4	19	1.8	17.3 ^{*3}	1343	2.5	1.6	751	2.2	2.2	173	15.8
Cross-talk	%	N/D	0.5	N/D	4.9 ^{*3}	<0.2 ^{*4}	3.57	2.75	2.97	0.85	0.95	1.0	<0.4

*1 Referred from [12]

*2 No data for peak PDE. The largest value in the article is used.

*3 No numerical value is expressed in the articles. The author calculated the value from the graphs in the articles.

*4 V_{ex} = 1V.

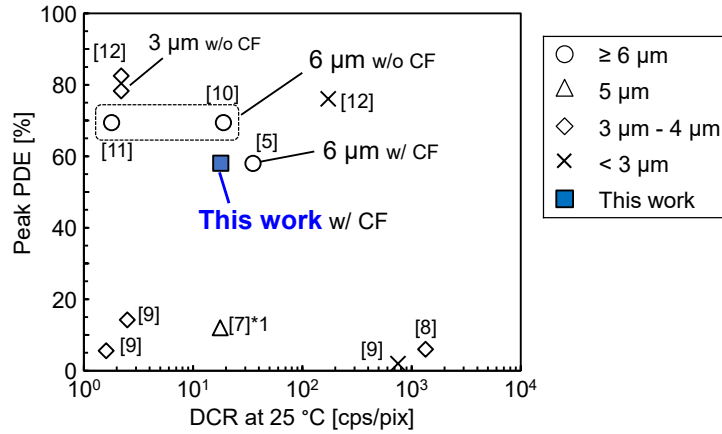


Figure 10. Comparison of PDE and DCR with previous works.

*1 No data for the peak PDE. The largest value in the manuscript is used.