A high PDE and high maximum count rate and low power consumption 3D-stacked SPAD device for Lidar applications

B. Mamdy[1] ; R. A. Bianchi[1] ; D. Golanski[1] ; B. Rae[2] ; T. M. Bah[1] ; D. Rideau[1] ; F. Twaddle[2]; R. Helleboid[1] ; C. Buj[3] ; N. Moussy[3] ; R. Fillon[1] ; Y. Henrion[1] ; E. Lacombe[1] ; R. Neri[1] ; F. Brun[1]; I. Nicholson[2] ; M. Agnew[2] ; B. Murray[2] ; M. Basset[1] ; R. Perrier[1] ; M. Al-Rawhani[2] ; S. Jouan[1] ; A. Lopez[2] ; L. Stark[2] ; S. Pellegrini[2]

[1]*STMicroelectronics, 850 rue J. Monnet BP16, 38926 Crolles cedex, France*
E-mail: bastien.mamdy@st.com Tel : +33 6 78 36 43 12
Email: raul-andres.bianchi@st.com Tel : +33 7 64 40 92 79
[2] *STMicroelectronics, 1 Tanfield, Inverleith Row, Edinburgh EH3 5DA, UK*
[3] *CEA LETI, 17 Av. des Martyrs, 38054, Grenoble, France*

***Abstract*—We present a 10.17µm pitch 3D-stacked backside illuminated Single Photon Avalanche Diode (SPAD). The wafer stack features a fully custom top tier process which is highly optimized for optical performance and a 40nm bottom tier which enables dense and low-power signal processing, local to the pixel array. State-of-the-art pixel performance is presented with a specific focus on high-sensitivity, low power, and high-speed operation. With a minimum operating voltage of 19.1V (at 60°C) a PDE of 18.5% is obtained at 940nm, with a 2.5V excess bias (which rises to 22% at 3.5V), with low DCR and low Jitter. This is achieved while consuming only 70fC of charge per pulse. The combination of low breakdown voltage and low charge per pulse minimizes power consumption which is essential for array scaling and for enabling low-power portable applications. With the selected sensing circuit design, tailored for high frequency performance, 85Mcps Max Count Rate is achieved, with a 2.5V excess bias (rising to >110Mcps at 3.5V), significantly reducing the pressure on pixel pitch reduction to cope with high illumination levels.**

Keywords— SPAD pixel, 3D 40nm SPAD technology, Low Power, High Count Rate, LIDAR, portable applications.

I. INTRODUCTION

Three-dimensional technology has revolutionized the field of electronics by enabling the development of more compact and more performant devices and pixels. Single-Photon Avalanche Diodes (SPADs) are a critical component in the field of imaging applications. The use of 3D technology in SPAD fabrication allows for the creation of smaller, more sensitive devices [2][3][4], but also faster and more power efficient devices, making them ideal for applications such as medical imaging, time-of-flight (TOF) ranging, and 3D imaging; most of them operate in the Near Infra-Red (NIR) and can require large pixel arrays (>100Kpixels) with specific requirements in terms of low power consumption and high dynamic range.

The pixel diodes and their driving/data-processing circuits presented are realized in-house on separate wafers, joined together through a standard wafer bonding technique and back-side processed. For the top-tier imaging technology, silicon remains the best choice for SPADs due to the maturity, reliability, and production costs of 300mm silicon process platforms, although III-V materials have superior optical properties in the infrared. Special care has been taken at SPAD design & process levels to maximize sensitivity, in the NIR, together with low power consumption.

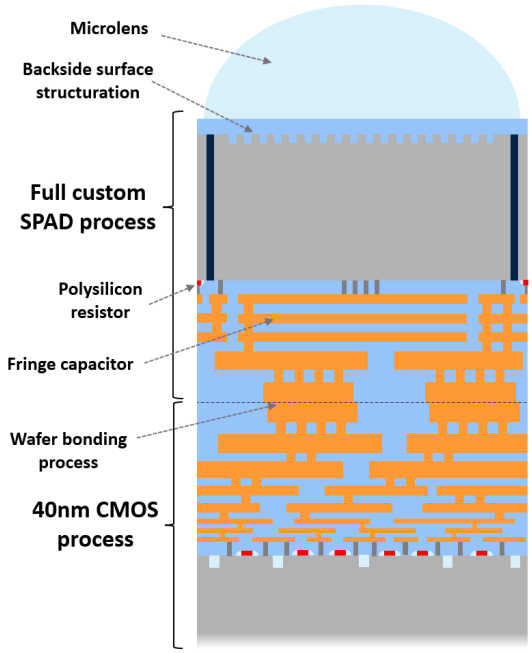

Fig. 1. Cross-section of our 3D-stacked backside illuminated SPAD pixel.

For the bottom-tier, a 40nm CMOS technology has been selected, which offers high circuit density, low cost and high silicon processing and chip design maturities. Special care has been taken in the design of the sensing circuitry of the pixel to ensure very high-count rates.

In this paper, we will explore the development of this SPAD in 3D 40nm technology, discussing the benefits of the technology and the pixel design, the challenges faced during its development, and potential advantages for applications demanding high-sensitivity together with low-power and high-count rates.

II. SPAD Pixel 3D Architecture

Fig. 1 shows the whole pixel structure: a 10.17µm pitch 3D-stacked backside illuminated SPAD architecture optimized for high sensitivity. It is composed of a 40nm CMOS, bottom-tier technology with 7 interconnect layers, and a 65nm top-tier imaging technology with 4 interconnect layers. Both are realized in-house on separate wafers and joined together by a standard hybrid bonding process performing electrical connections at pixel level. Back-side processing consists of surface structuration, anti-reflective coatings, micro lenses, and passivation layers.

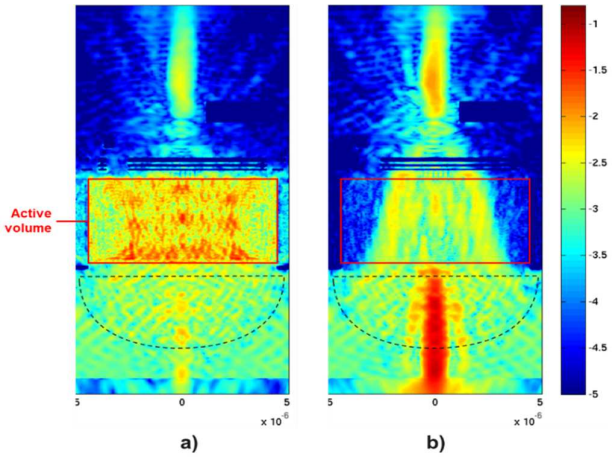

Fig. 2. Cross-section of a 3D-FDTD optical simulation showing the Poynting vector amplitude (log scale) for light at 940nm for our SPAD with (a) and without (b) back-side structuration.

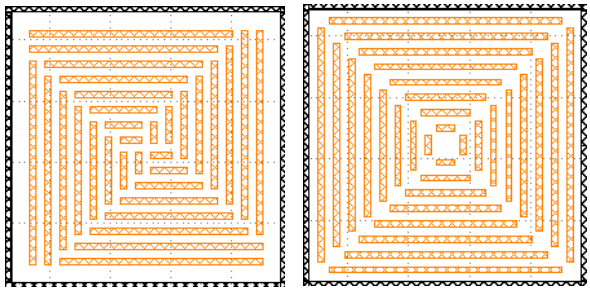

Fig. 3. Top view of the back-side structuration patterns used to significantly increase the optical absorption of the SPAD.

The 3D back-side illuminated structure allows high fill factor and isolates a large carrier collection volume. The resulting NIR sensitivity increase is in the order of a factor 10, compared to previous front-side 2D SPAD technologies. To maximize the photon absorption within the active volume, a back-side structuration pattern has been optimized through 3D-FDTD simulations (see Fig. 2). It has been implemented with a dedicated etch process, different than the conventional wet process leading to inverted pyramid shapes [1]. Trench-like shapes are produced, allowing a large variety of structuration pattern designs (see Fig. 3) and specific optimizations.

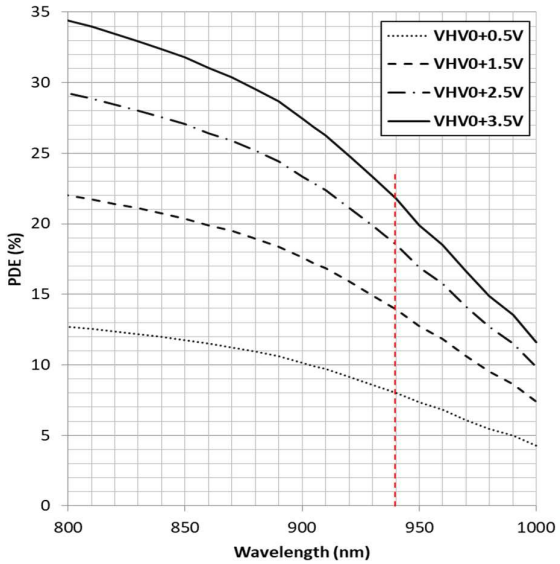

Fig. 4. Photon Detection Efficiency vs wavelength and excess bias at 60°C.

III. SPAD Pixel Standard Performances

The back-side structuration, plus the highly reflective interfaces, induces multiple reflections within the silicon volume and hence increases the effective silicon path-length that light travels through (See in Fig. 2-a, that an almost full pixel illumination is obtained when back-side structuration is added). This, combined with the action of the backend metal reflector, results in an additional sensitivity increase in the order of a factor 4, allowing us to reach never seen before Photon Detection Efficiency (PDE, illustrated in Fig. 4) densities of 0.04%/µm3 of silicon at 940nm, almost twice as high as the value reported in state-of-the-art SPAD devices [2][3].

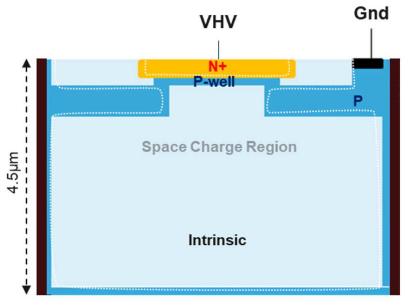

Fig. 5. Diode cross-section with doping scheme.

The diode architecture and implantation scheme are described in Fig. 5. The diode is an N+ over PWell junction

built on a very lightly doped substrate. The PWell depth and doping level are optimized such as to maximize the junction's breakdown probability, maintain ~18.6V breakdown voltage (VBD), at 60°C, and allows for the entire PWell depth to be depleted at breakdown voltage. Indeed, at the standard operating condition, the space charge region extends deeply within the 4.5µm thick substrate volume. A P-doped guard ring implant is designed and fabricated to prevent edge breakdown and redirect photogenerated carriers towards the central avalanche region.

With a minimum operating voltage (also called VHV0) of 19.1V , at 60°C, a PDE of 18.5% is achieved at 940nm, at 2.5V excess bias (which rises to 22% at 3.5V excess bias, as shown in Fig. 4), together with a low Dark Count Rate (DCR) of 0.81kcps and low Jitter of 119ps Full Width at Half Maximum (FWHM).

IV. Low Power and High Count Rate

The SPAD pixel performances quoted above are achieved while consuming less than 70fC of Charge per Pulse (CPP) at nominal 2.5V excess bias, as illustrated in Fig. 6. The combination of low breakdown voltage and low charge per pulse greatly minimizes array power consumption which is essential for array scaling and for enabling low-power portable applications.

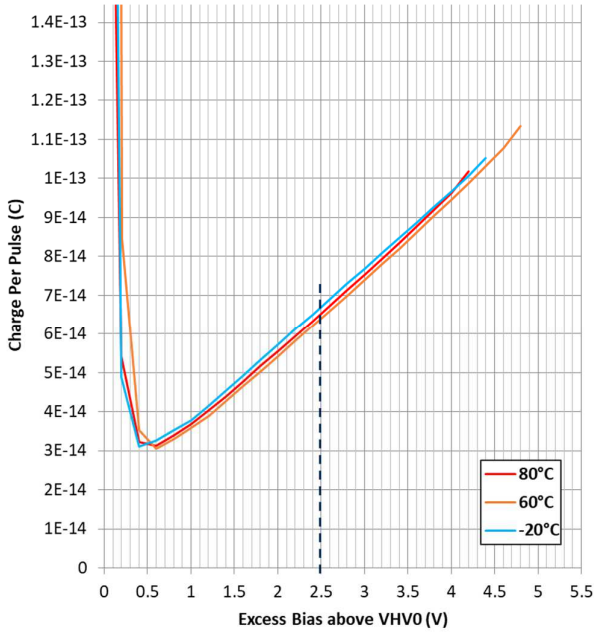

Fig. 6. Quantity of charges generated per avalanche as a function of excess bias and temperature.

This optimized diode architecture is associated to a novel readout circuit described in Fig. 7. Unlike regular SPAD devices [4][5], both the quenching and the detection of the avalanche is performed on the high voltage node (the cathode), as its low capacitance minimizes the pixel power consumption. Similarly, on the high voltage side, a very highly resistive, high voltage compatible, resistor R_Q, is implemented for quenching purposes and to passively limit the power consumption in case of SPAD paralysis, at excessively high illumination levels.

Finally, a combination of a high-voltage cascode N-type MOSFET, a low-voltage N-type enable MOSFET, and a V_{PULLUP} clamp diode, all connected to the anode of the SPAD, allows full disable of selected pixels. When EN is set to V_{SUB}, the anode voltage is allowed to rise more than the excess bias, putting the SPAD safely out of Geiger mode. This is a necessary feature for two reasons: to disable the few defective pixels exhibiting high DCR during BIST system runs, and to disable the array sectors that are not addressed or that are non-illuminated, allowing both very significant power savings, at SPAD array level.

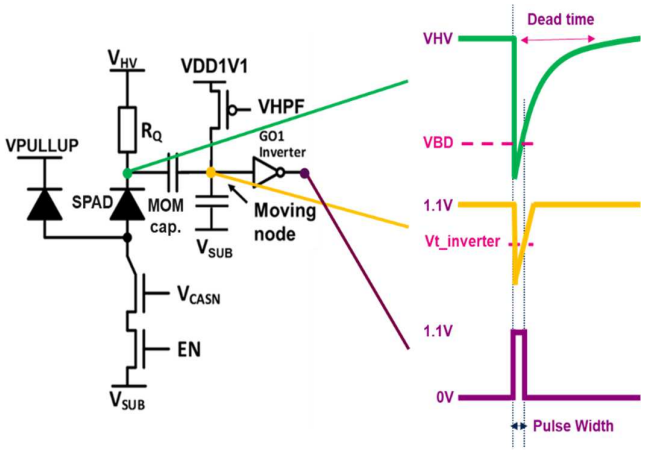

Fig. 7. Pixel schematics including the SPAD diode, the quenching resistor RQ, the Metal-Oxide-Metal coupling capacitor, the readout circuitry, and the disabling circuitry. Expected voltage swing observed at the SPAD cathode (green), the pulse shaping node (yellow) and after the inverter (purple).

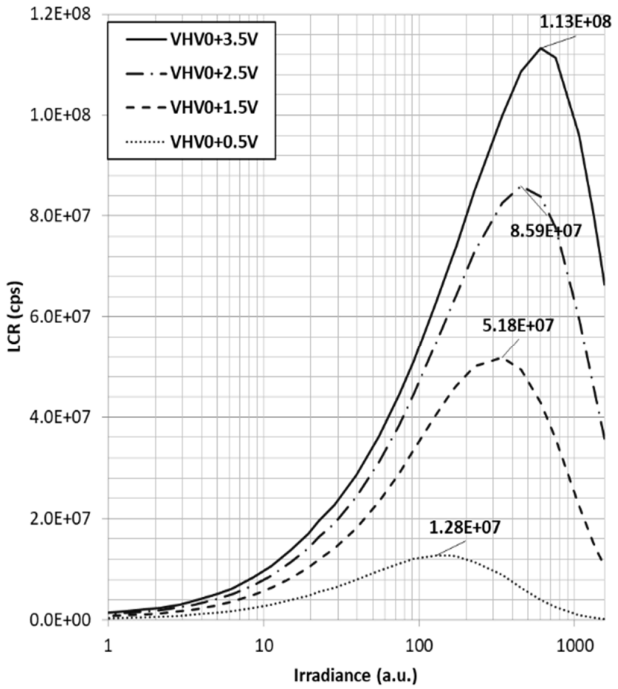

Fig. 8. Light Count Rate (LCR) measurement vs excess bias at 60°C. Max Count Rate (MCR) values correspond to the peak of each LCR curve.

For high frequency performance reasons, the detector is AC-coupled, through a 25V Metal-Oxide-Metal capacitance that also acts as a capacitive voltage divider, as shown in Fig. 7, between the cathode of the SPAD and the input of the inverter; the latter being used to generate the pulsed output signal of the pixel. A pulse shaper transistor is also embedded and connected to the input of that inverter, as a pull-up element. In standard operating conditions, Vhpf is set to 0V to obtain an additional high pass band action that maximizes the bandwidth of the whole detection circuit.

This high frequency detection scheme, that to the best of our knowledge has never been reported, enables very high Max Count Rates (MCR), beyond 100Mcps, as illustrated by Fig. 8. This feature is essential for dynamic range, as PDE increases. In addition, it significantly reduces the pressure on pixel pitch reduction [4], to cope with high illumination levels.

V. Comparison with the State-of-the-Art

TABLE I. summarizes main pixel performance, at 60°C, and for different excess bias conditions along with a comparison to state-of-the-art. Performance at 2.5V excess bias, are comparable to state-of-the-art for 940nm PDE, DCR and Jitter and beyond state-of-the-art for power consumption (CPP, VBD, Ve) and for maximum quench/recharge speed related metrics (MCR, DT).

TABLE I. Pixel Performance Comparison

Parameters	Unit	This work			[2]	[4]
BI Technology	nm	65/40			90/40	90/22
Pixel Pitch	um	**10.17**			10	6
VBD @ 60°C	V	**18.6**			20	22
Excess Bias (Ve)	V	1.5	**2.5**	3.5	3.0	3.0
PDE @ 940nm	%	14	**18.5**	22	14.2	20.2
DCR @ 60°C	kcps	0.57	**0.81**	1.27	0.22	0.3
Jitter FWHM	ps	143	**119**	103	173	137
Max Count Rate	Mcps	52	**85**	113	50	60
Dead Time (DT)	ns	6.9	**4.3**	3.3	8.0	6.3
Charge per Pulse	fC	48	**68**	92	-	-

Even higher sensitivity and speed can be obtained at 3.5V excess bias, at the cost of a higher CPP. Conversely, at a low excess bias of 1.5V, a significant CPP reduction is obtained, while maintaining very good PDE, Jitter, MCR and DT performances.

In TABLE II. pixel performance versus temperature, from -20°C to 80°C, is presented. The VBD and DCR exhibit classical thermal coefficients, of +25.6mV/°C and x2 each 7°C (at high temperature) respectively; while PDE, Jitter, MCR, DT and CPP remains almost unaffected by temperature variations over a very wide range, at constant 2.5V excess bias.

TABLE II. Pixel Performance vs Temperature

Parameters, at 2.5V Ve	Unit	-20°C	**60°C**	80°C
Breakdown Voltage (VBD)	V	16.6	**18.6**	19.2
PDE @ 940nm	%	17.6	**18.5**	18.2
Dark Count Rate (DCR)	cps	8.6	**810**	6923
Jitter FWHM	ps	118	**119**	185
Max Count Rate (MCR)	Mcps	72	**85**	88
Dead Time (DT)	ns	5.1	**4.3**	4.2
Charge per Pulse (CPP)	fC	76	**68**	67

VI. Conclusions

Technology and pixel performance has been presented for a 10.17µm pitch SPAD pixel implemented in a 40nm 3D-stacked backside illuminated technology that represents a significant advancement in the field of single-photon detection, especially for large array applications, requiring low-power consumption and high count-rates. State-of-the-art sensitivity at 940nm (PDE) and noise figures (DCR, Jitter) have been achieved, together with a very significant progress in VBD, CPP, MCR and DT, maximizing pixel dynamic range, thanks to the introduction of specific and novel features at technology, avalanche diode design and sensing circuit design levels.

Specific focus on low-power pixel and array design is essential to enable large array scaling, especially for portable applications. The high-frequency performance of the pixel driving and sensing circuitry enables very high count-rates, which is necessary to sustain high illumination operation. As the demand for high-performance, low-power single-photon detectors continue to grow, this 3D 40nm SPAD technology represents a high performant and cost-effective solution.

[1] I. Oshiyama, et al., "Near-infrared Sensitivity Enhancement of a Back-illuminated Complementary Metal Oxide Semiconductor Image Sensor with a Pyramid Surface for Diffraction Structure," IEDM 2017, pp.16.4.1-16.4.4

[2] K. Ito, et al., "A Back Illuminated 10µm SPAD Pixel Array Comprising Full Trench Isolation and Cu-Cu Bonding with Over 14% PDE at 940nm," IEDM 2020, pp. 16.6.1-16.6.4

[3] K. Morimoto, et al., "3.2 Megapixel 3D-Stacked Charge Focusing SPAD for Low-Light Imaging and Depth Sensing," in IEDM, 2021.

[4] S. Shimada, Y. Otake and S. Yoshida, "A Back Illuminated 6 µm SPAD Pixel Array with High PDE and Timing Jitter Performance," in IEDM, 2021.

[5] S. Pellegrini et al., "Industrialised SPAD in 40 nm technology," in IEDM 2017, pp. 16.5.1-16.5.4