A NIR Enhanced SPAD Fabricated in 110 nm CIS Technology with 78% PDP at 500 nm

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***Abstract*—In this work, we demonstrate a 10 µm diameter single-photon avalanche diode (SPAD) fabricated in 110 nm CMOS Image Sensor (CIS) technology with enhanced near-infrared (NIR) sensitivity. Thanks to the electric field engineering with the numerical simulations, the electric field is kept high throughout a wide depletion region by the existence of the extra second peak in the profile. Consequently, this favors the absorption of NIR photons and augments the avalanche triggering probability. The measurement results show that at an excess bias voltage of 4 V, the device reaches a photon detection probability (PDP) of 50% at a wavelength of 500 nm with a normalized dark count rate (DCR) of 0.76 cps/µm^2. At 5.5 V, PDP at 500 nm reaches 78%, while DCR stays at 3.7 cps/µm^2 with an afterpulsing probability of 3%. Furthermore, at 850 nm, the device achieves a PDP of 13% and 25.5% at the same excess bias voltages. To the best of our knowledge, these results are among the highest NIR and visible PDPs obtained in any CMOS SPAD. The jitter of the device is 115 ps at 850 nm at 5.5 V excess bias, which makes the device a great candidate for single-photon sensing at red and NIR wavelengths.**

I. Introduction

Applications such as light detection and ranging (LiDAR), optical tomography, and fiber optic communications require high-sensitivity photodetection in the NIR [1]–[3]. Therefore, there has been an increasing effort towards improving NIR efficiency in solid-state photodetectors. In this category of detectors, SPADs exhibit photon-counting capability and low jitter in a compact and generally low-cost format. In order to enhance sensitivity in the NIR, deeper junctions and wider depletion regions have been investigated to be able to collect deeply absorbed NIR photons in silicon [4]–[11]. Deep multiplication regions are very effective at shifting peak detection wavelengths to NIR while causing a sensing efficiency loss in visible. In wide depletion regions, the electric field magnitude becomes relatively low, and it decays from the multiplication regime to the opposite end of the junction. Therefore, wide depletion devices require high excess bias voltages (∼10 V) to increase the electric field magnitude and avalanche triggering probability. However, high excess biases can increase band-to-band (BTB) and trap-assisted tunneling (TAT) contributions to DCR and lead to noisier devices. Besides, it might complicate the pixel circuit design when the excess bias becomes higher than the allowed rail-to-rail voltage range.

In this study, we propose a new SPAD device to address the high excess bias requirement in the wide depletion region approach. To be able to augment the electric field magnitude and avalanche triggering probability, extensive numerical simulations on TCAD were conducted, which enabled us to design a double-peaked electric field profile and keep the electric field magnitude high throughout a wide depletion volume. This new double-peaked profile is in contrast to the previously designed wide depletion and NIR enhanced SPADs, where the devices only have one peak and the magnitude of the electric field stays low in the remaining depletion region. Owing to this electric field engineering and designing a non-isolated device, we expected to increase NIR PDP while not sacrificing sensitivity in the visible spectrum. The device, afterwards, was fabricated in 110 nm CIS technology node and has an active area with a diameter of 10 µm.

II. Device Design and TCAD Simulations

To create a double-peaked electric field profile and enhance the multiplication rates of the carriers in the depletion region, we utilized a technology-specific deep p-well layer/high-voltage n-well junction where the p-well layer has double peaks in its doping concentration. Thanks to these double peaks in the p-well layer, we also achieved two peaks in the electric field profile. The chosen p-well layer is also relatively lightly doped, which allowed us to obtain a wide depletion region. Moreover, the high-voltage n-well layer was extended to form a guard ring around the main junction and prevent the device from suffering premature edge breakdown. The cross section of the device is provided in Fig. 1.

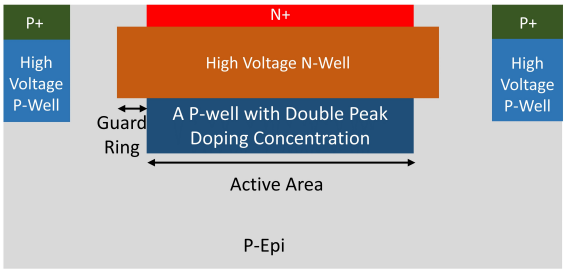

Fig. 1. The cross section of the proposed device.

The electric field simulations of this device can be seen in Fig. 2. The simulations were performed on TCAD numerical tool. Exact doping profiles of the layers used in the cross section were imported into the simulation environment. Then, coupled Poisson and electron-hole drift-diffusion equations

were solved to calculate the electric field magnitude under various voltages. As illustrated in Fig. 2a, in addition to the first electric field peak indicated with red, the second peak appears in the proposed device's field profile at 1 V excess bias, which is depicted with yellow. The variation of the electric field from 1 V to 5 V excess bias voltage is also given, where the second peak becomes more obvious with its emerging red color. Besides, the magnitude of the electric field at the center of the device along the y axis from 1 V to 5 V excess bias is provided in Fig. 2b. It demonstrates that the electric field profile indeed has double peaks, and its magnitude is kept high almost in the entire depletion region, which will result in boosting avalanche triggering probabilities for the electrons and holes and the PDP accordingly. In fact, the electric field magnitude of the second peak is also above the critical avalanche breakdown field in silicon, which is $3x10^5$ V/cm. Therefore, the second peak will behave as a second multiplication center for the carriers, which is a new concept for SPAD design and can be utilized to enhance PDPs in any CMOS technology.

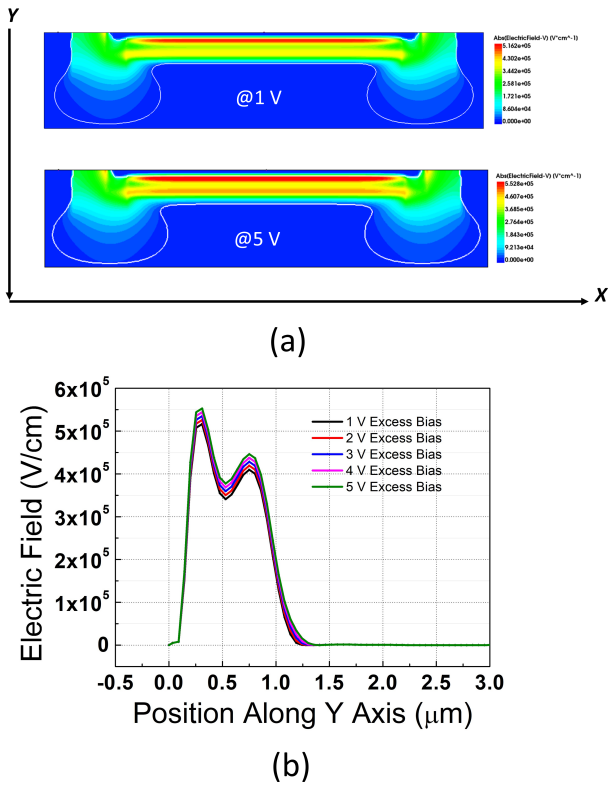

Fig. 2. (a) Electric field simulations of the proposed device on TCAD. (b) Electric field magnitude acquired at the center of the device along the y axis. *Note: White lines on electric field simulations correspond to the depletion region boundaries.*

III. Characterization Results

A. I-V Measurements and Light Emission Tests

Fig. 3a shows the I-V characteristics of the device under ambient light and at room temperature. The breakdown voltage, which is displayed by the sharp increase in the current, occurs at 29.8 V. To verify that the device does not suffer from premature edge breakdown, light emission tests were performed at 3 V and 5 V excess bias voltages. Fig. 3b shows that there is no edge breakdown effect in the proposed device, thanks to the implemented guard ring structure in the design. These results prove that the device functions properly in Geiger mode.

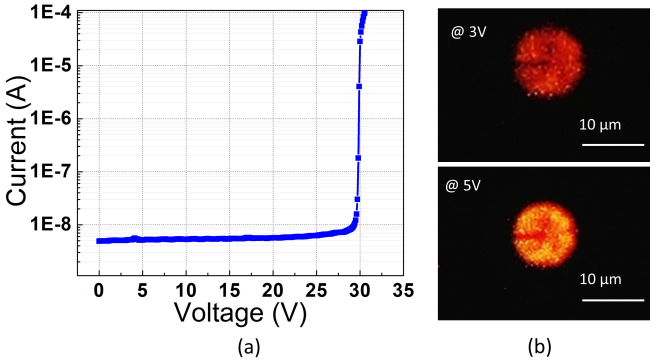

Fig. 3. (a) I-V measurement of the SPAD under ambient light and at room temperature. (b) Light emission tests of the device at 3 V and 5 V excess bias voltages.

B. DCR Measurements

The DCR measurements were taken with an externally connected 660 kilo-ohm resistor to quench and recharge the SPADs. We have measured the same SPAD from different dies to collect statistics about the noise. Fig. 4 demonstrates the DCR measurements belonging to five devices with respect to the excess bias voltage. According to this graph, Device 3 was selected as a reference since it corresponds to the median in the noise measurements. The DCR of this device changes from 8 cps at 1 V to 295 cps at 5.5 V excess bias and at room temperature. The DCR per unit area at 5.5 V excess is 3.7 cps/μm^2, which is among the lowest noise in NIR enhanced SPADs fabricated with CMOS technologies. In the rest of the paper, we will present the characterization results of Device 3.

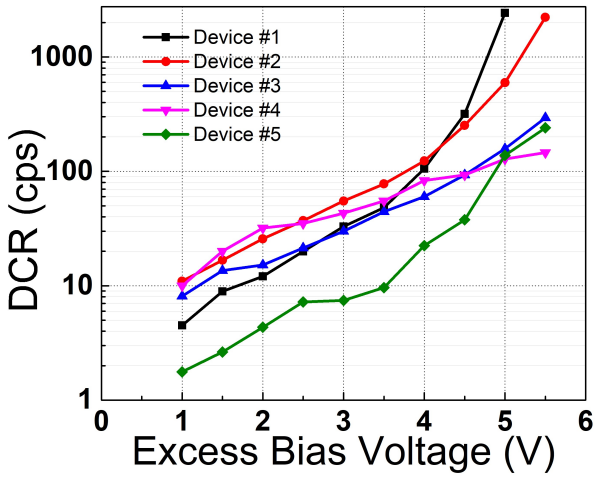

Fig. 4. DCR characterization of the proposed device with respect to the excess bias voltage from five different dies.

C. Afterpulsing Probability Measurement

The afterpulsing histogram of the device was obtained with the inter-avalanche time method. To measure the time interval between the pulses, a high-speed digital oscilloscope (Teledyne LeCroy WavePro 760Zi-A) was utilized. An afterpulsing histogram obtained under dim light is shown in Fig. 5. As the SPAD was passively quenched and recharged through an external resistor, the dead time of the SPAD was around 7 µs. The afterpulsing probability of the device is 3% at 5.5 V excess bias, which is calculated as the ratio of the area between the measured and fitted curves to the area beneath the fitted curve. Hence, this low afterpulsing probability indicates that the defect concentration in the fabricated device is likewise expected to be low.

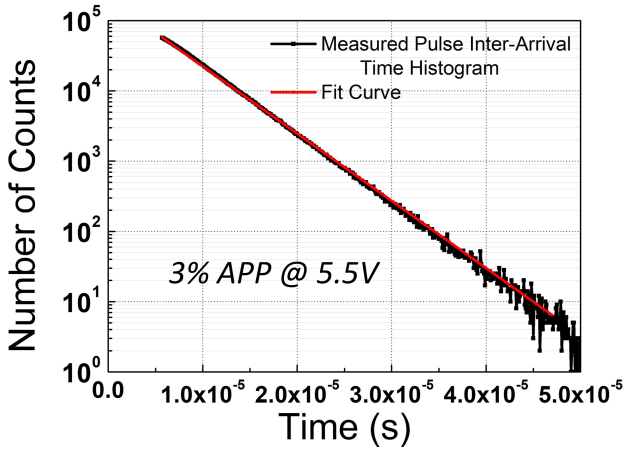

Fig. 5. Inter-arrival avalanche timing histogram with an exponential fit and afterpulsing probability at the excess bias voltage of 5.5 V.

D. PDP Measurements

The PDP of the device was measured via a monochromator setup where a Xenon lamp emits broad-band light and a monochromator selects each wavelength through the gratings. Then, an integrating sphere was used to provide spatially uniform light onto the SPAD and a calibrated reference detector to precisely assess the impinging photon count. Under this configuration, the measured PDP of the device was obtained as shown in Fig. 6, from 1 V to 5.5 V excess bias voltage. As is more obvious at 5.5 V, the peak PDP actually occurs at two different wavelengths, which are 450 nm and 500 nm. We think that this is related to the two-peak nature of the electric field profile of the device, which thereby forms two multiplication regions favoring the detection of these wavelengths the most. At an excess bias voltage of 4 V and 500 nm wavelength, the device has a PDP of 50%, and at 5.5 V excess, PDP at 500 nm reaches 78%. Furthermore, thanks to the high electric field achieved throughout the depletion region, NIR sensitivity of the device is also enhanced. At 850 nm, the SPAD has a PDP of 13% and 25.5% at 4 V and 5.5 V excess bias voltages, respectively. To the best of our knowledge, these PDP values are the highest reported for visible and NIR wavelengths.

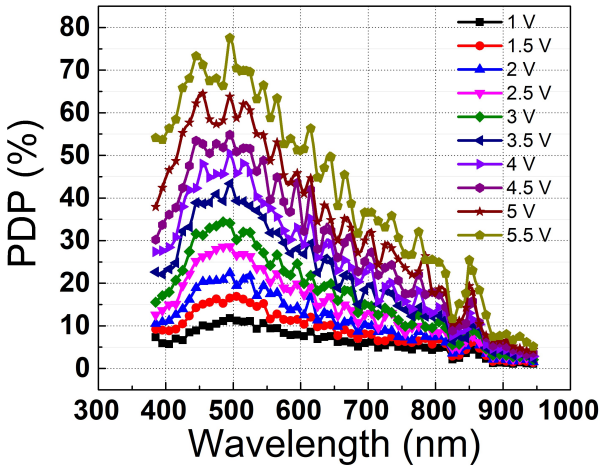

Fig. 6. PDP measurement of the device from 1 V to 5.5 V excess bias voltage.

E. Jitter Measurement

To measure the timing jitter, the time-correlated single-photon counting (TCSPC) technique was employed. The device was illuminated with a 850 nm (A.L.S. GmbH) pulsed laser operating at 100 kHz, and incident power was reduced to single-photon regime with the absorptive neutral density filters. To detect the time difference between the laser clock signal and the positive edge of each avalanche pulse, we used the same high-speed digital oscilloscope. The jitter histograms acquired at 850 nm and at 3 V and 5.5 V excess biases are provided in Fig. 7. The jitter is calculated as full width at half maximum (FWHM), which is 200 ps at 3 V excess bias and reduces to 115 ps at 5.5 V excess bias voltage.

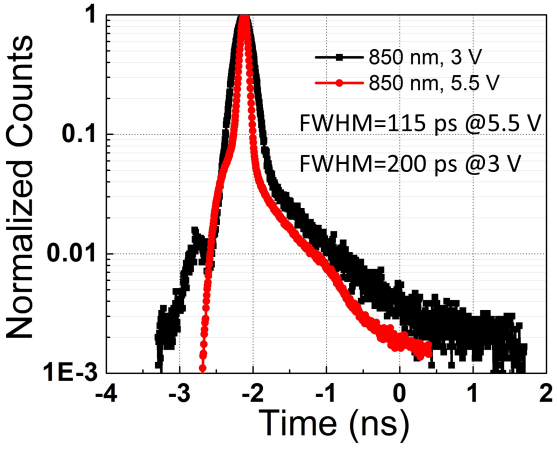

Fig. 7. Timing jitter histogram of the device, which was obtained at 850 nm and for 3 V and 5.5 V excess bias voltages.

IV. Comparison with State-of-the-Art

In Fig. 8, we have chosen the best-performing front-side-illuminated (FSI) CMOS SPADs having a wide depletion and NIR enhanced sensitivity to compare our device with. Fig. 8a indicates the peak PDP achieved with these SPADs versus the normalized DCR with the active areas. As can be seen, our device attains the highest PDP ever reported, along with

one of the lowest DCR per unit area. Fig. 8b shows the PDP comparison at 850 nm wavelength with respect to the excess bias voltage. It demonstrates that our device indeed eliminates the high excess bias needed in wide depletion devices, owing to the double-peaked electric field engineered in this work that increases avalanche triggering probability. Fig. 8b also illustrates that our device reaches one of the highest PDPs at NIR.

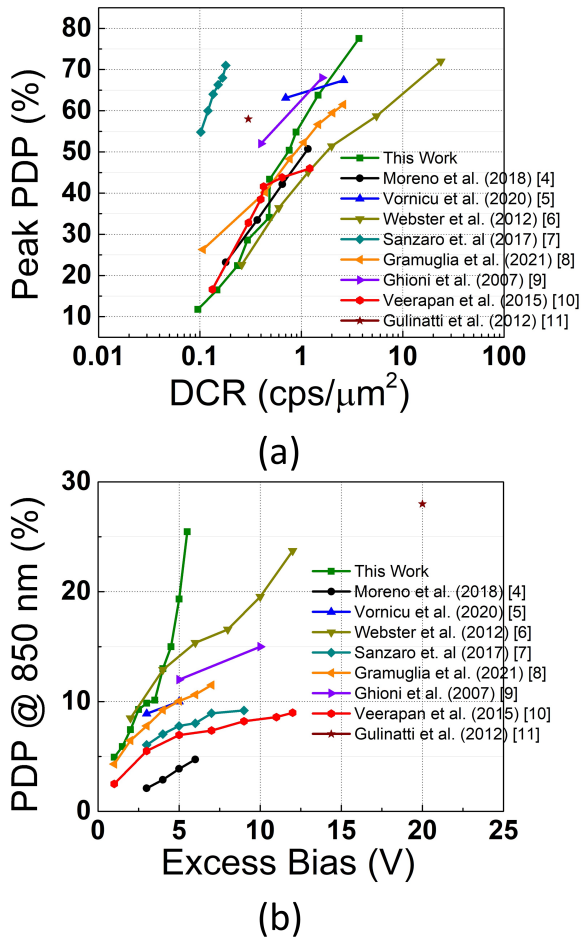

Fig. 8. (a) Peak PDP vs. DCR per unit area, (b) PDP at 850 nm vs. excess bias voltage comparisons of the state-of-the-art FSI SPADs fabricated in the same and other CMOS technology nodes.

V. Conclusion

In this work, we presented a new SPAD design with low noise and enhanced NIR PDP. A double-peaked electric field formed inside the wide depletion region of the device, enabling it to increase the avalanche triggering probability and hence the PDP of the SPAD, which reaches 78% at 500 nm and 25.5% at 850 nm at 5.5 excess bias voltage. The noise of the SPAD remains at 300 cps or 3.7 cps/μm^2 at the same voltage. We believe that this new concept of designing SPADs will pave the way to the design for novel red and NIR enhanced SPADs in near future.

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