Doping Engineering for PDP Optimization in SPADs Implemented in 55-nm BCD Process

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***Abstract*—**We introduce a new family of single-photon avalanche diodes (SPADs) with an enhanced depletion region integrated in a 55-nm Bipolar-CMOS-DMOS (BCD) technology. We demonstrate how to systematically engineer doping profiles in the main junction and in deep p-well layers to achieve high sensitivity and low timing jitter. To demonstrate the technique, a family of SPADs was designed and fully characterized. Sensitivity spectra was enhanced at long wavelengths, achieving up to 41.3% at 640nm and 22.3% at 850nm. Timing jitter was reduced to less than 100ps (FWHM). The proposed SPADs are suitable to low-pitch, large-format image sensors for high-speed time-resolved applications.

I. Introduction

Single-photon avalanche diodes (SPADs) in monolithic CMOS technologies have received great attention in recent years for scientific, industrial, and consumer applications, such as time-of-flight (TOF) sensing, LiDAR, low-light photon counting imaging, medical or biomedical imaging, quantum random number generation (QRNG) [1]. However, CMOS SPADs using an advanced technology tend to have limited sensitivity, measured as photon detection probability (PDP), often peaking at 450-550nm. In these SPADs, PDP is usually poor in near-infrared (NIR) spectral range, due to narrow depletion region.

Significant improvements in NIR and an overall wide spectral range has recently achieved in submicron CMOS technologies [2]-[6], however fill factors are often low. The use of electrical microlensing [7], also known as charge focusing [8], has been shown to be useful to improve PDP performance. Electrical microlensing consists of forcing photo-generated carriers drift towards the multiplication region by gradual doping profile or electric field. However, wide and deep depletion regions appear to be the most effective means to improve NIR PDP. For instance, Webster *et al.* have achieved over 40% PDP from 410nm to 760nm at high excess bias by burying the multiplication region in 130nm CMOS technology. Niclass *et al.* have used fully depleted SPAD structure in 180nm CMOS technology achieving a PDP of 64.8% at 610nm and 24% at 850nm at moderate excess bias.

Here we report on a new family of SPADs with a pitch of 8.5µm characterized by different depletion regions. We first demonstrate how to systematically engineer the doping of the main junction and all deep p-well layers, and then fully characterize the impact of doping engineering in small SPADs. The proposed SPAD1 and SPAD2 show less than 50ps timing jitter at 5V excess bias voltage, while SPAD3 shows enhanced PDP in the NIR spectral range, and it maintains a low timing jitter at 3V excess bias voltage.

II. SPAD Structure

Fig. 1 shows the cross-section of the frontside-illuminated SPAD family. The SPAD is based on a shallow N-well (NW) and P-well (PW) junction. A pitch of 8.5µm was implemented for the entire family. All the SPADs were designed and realized in a round shape with an avalanche diameter of 4.4µm, achieving a fill factor of 21%. Based on the achieved results, we expect to achieve higher fill factor in future generations. Fig. 2 shows the doping profile as a function of depth below the surface. The substrate features a gradient of p-type doping in the epitaxial layer, and the SPAD incorporates three different deep P-well (DPW) layers below the junction.

Fig. 3 shows simulations of the relative electric field as well as the depletion layer boundaries. The avalanching junction is engineered through the shallow NW and PW layers and optimized to achieve a high avalanche gain and wide depletion region. With different DPW layers, the depletion region is well defined in depth. The photo-generated carriers in the depletion region can thus quickly drift upward towards the avalanching junction and ensure enhanced PDP in NIR.

III. Results and Discussion

The static current/voltage curves of the proposed SPADs were measured using a semiconductor analyzer, revealing extremely low dark current levels in the pA range for all three variants. The current-voltage curves with illumination are shown in Fig. 4. With different DPW layers, the corresponding breakdown voltages are 17.1, 20.6, and 23.0 V, respectively. As expected, the breakdown voltage is related to both the main junction and the DPW layers for miniaturized fully depleted SPAD. Besides, it is clearly shown that SPAD2 and SPAD3 achieve lower photo-current above breakdown. Fig. 5 shows the breakdown voltage as a function of temperature from -40ºC to

60ºC. The extracted temperature coefficients are 16.7, 44.5, and 56.5mV/ºC, respectively. Temperature coefficients are larger for thicker depletion regions.

The dark count rate (DCR) of 8 samples for each SPADs was measured at room temperature. Fig. 6 shows the median DCR as a function of excess bias voltage. The median DCR of SPAD1 is 132cps at 3V and 290cps at 5V excess bias voltage. DCR can be further reduced through optimization of the guard ring. SPAD2 shows the best DCR performance, with a median DCR of 62.3cps at 3V and 132.2 cps at 5V excess bias voltage. The median DCR of SPAD3 is 474.2cps at 3V excess bias voltage. The temperature dependence of DCR is shown in Fig. 7 for 3V excess bias voltage, whereas SPAD2 and SPAD3 show a strong temperature dependence, indicating that trap-assisted thermal generation is the main source of noise.

Fig. 8 shows the measured PDP from 400nm to 960nm with a step of 10nm for all the SPADs. With different DPW layers, it is clearly shown that the peak PDP migrates from 450nm, to 540nm, and finally settles to 640nm. SPAD1 achieves a peak PDP of 48.9% at 450nm, and 6.7% at 850nm at 5 V excess bias voltage. SPAD2 achieves a peak PDP of 32.4% at 540nm, and 10.7% at 850nm at 5V excess bias voltage. Thanks to the wider depletion region, SPAD3 shows a high PDP over a wide spectral range, with peak PDP of 41.3% at 640nm, and 22.3% at 850nm at 3V excess bias voltage. This broad spectral response from visible to NIR holds great potential for a variety of applications, including time-of-flight imaging, low-light-illumination imaging. The peak PDP as a function of excess bias voltage is shown in Fig. 9. The peak PDP of SPAD3 shows the strongest dependence on excess bias voltage.

A dedicated printed circuit board equipped with a fast comparator was utilized to evaluate timing jitter. A low threshold voltage was applied to detect the SPAD signal at the onset of the avalanche phenomenon. Fig. 10 shows timing jitter at 3V excess bias voltage with an 850-nm laser source. The evolution of jitter as a function of excess bias voltage is shown in Fig. 11. A timing jitter of 42, 70, and 96ps (FWHM) is achieved at 3V excess bias voltage, respectively. Timing jitter at the same excess bias voltage strongly increases with the expansion of the depletion region.

IV. State-of-the-Art Comparison

Fig. 12 shows the PDP and timing jitter comparison of the proposed SPADs with the previously reported N-on-P type SPADs in CMOS technology. The SPAD1 and SPAD2 show less than 50ps timing jitter at 5V excess bias voltage. The SPAD3 shows a high PDP at 850nm, while keeping a low timing jitter at 3V excess bias voltage. Table 1 shows the overall performance of the developed SPADs and a comparison with the state-of-the-art.

V. Conclusions

We demonstrate the role of doping engineering to widen the depletion region in small SPADs with a pitch of 8.5µm implemented in a 55-nm BCD process. To demonstrate it practically, a family of SPADs was designed, realized, and fully characterized in this technology. The doping profiles of the avalanching junction layers were optimized to achieve red- and NIR-enhanced sensitivity. Experimental evaluation of the proposed SPADs revealed that the PDP peak wavelength can be improved with a wider and deeper depletion region. SPAD3 was designed to achieve this goal. It shows a high PDP over a wide spectral range, with a peak PDP of 41.3% at 640nm, and 22.3% at 850nm, and the timing jitter 96ps at 3V excess bias voltage. The technique is suitable for small-pitch SPADs and large-format image sensors, with multi-megapixel resolution, both operating in frontside- and backside-illuminated modes.

Acknowledgment

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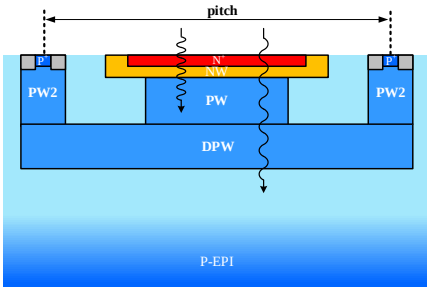

Fig. 1. Simplified cross-section of the SPAD. The structure is based on shallow NW and PW. Three different DPW layers are implemented. All 3 SPADs have same drawn avalanche area and pitch.

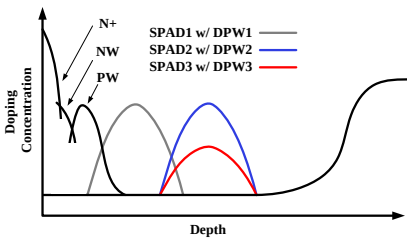

Fig. 2. The simplified doping profile versus distance from silicon surface. The DPW1-3 layers are used in SPAD1-3, respectively.

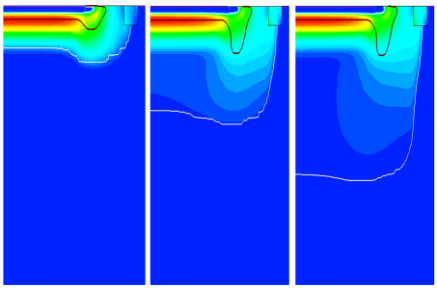

Fig. 3. Simulation results depicting the electric field as well as the depletion layer boundaries for SPAD1 (a), SPAD2 (b), and SPAD3 (c) at 3V excess bias voltage. The junction is engineered to achieve a wide depletion region.

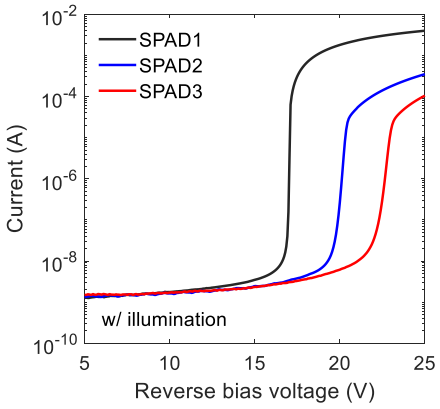

Fig. 4. SPADs current as a function of reverse bias voltage with illumination.

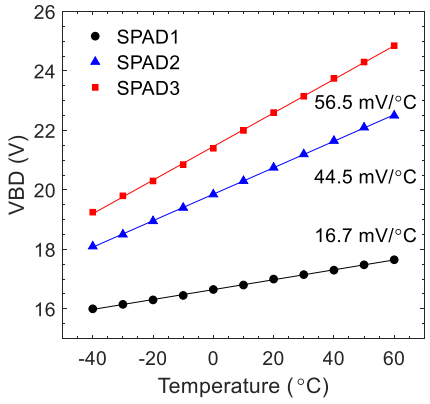

Fig. 5. Breakdown voltage as a function of temperature for 3 different SPADs.

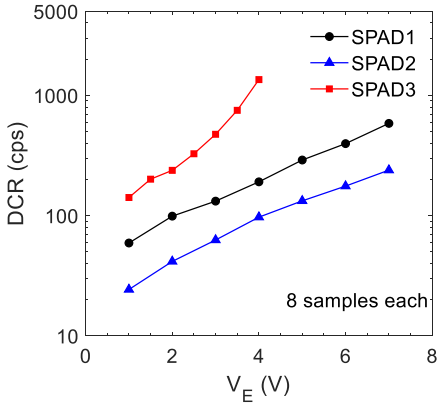

Fig. 6. Median DCR at room temperature. The data is obtained by measuring 8 dies. The corresponding median DCR is 132, 62.3, and 474.2cps at 3V excess bias voltage.

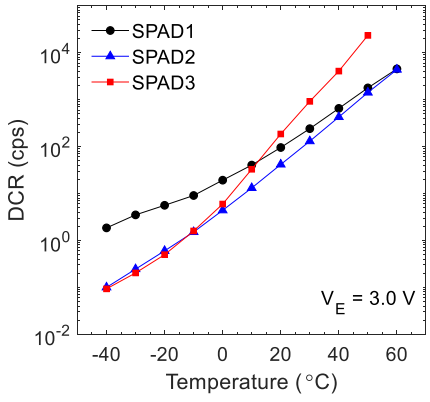

Fig. 7. Temperature dependence of DCR for 3 different SPADs. Measurements were taken from one SPAD sample each from -40 ºC to 60 ºC.

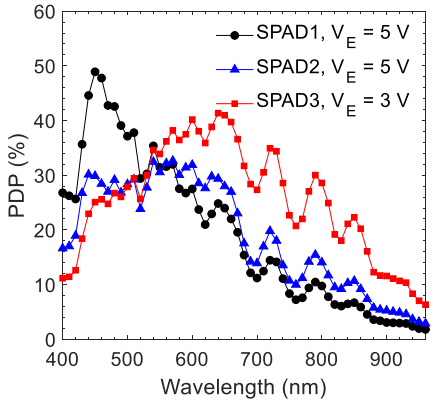

Fig. 8. PDP as a function of wavelength for 3 different SPADs.

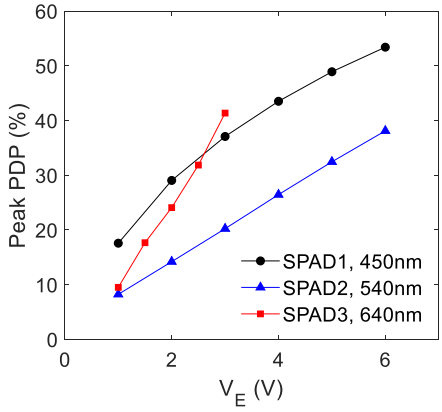

Fig. 9. PDP as a function of excess bias voltage at the peak wavelength for 3 different SPADs.

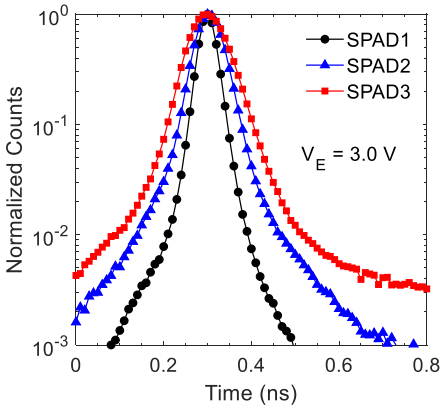

Fig. 10. Timing jitter response for an 850 nm laser at 3V excess bias voltage. The jitter of the laser is 32ps.

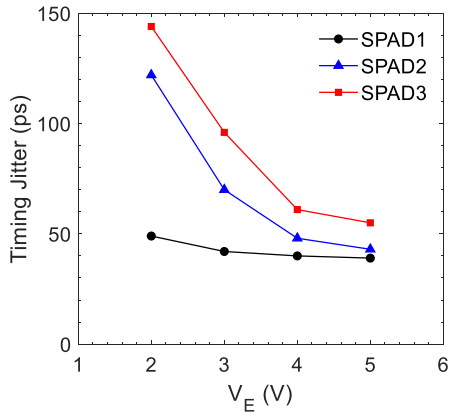

Fig. 11. Timing jitter (FWHM) as a function of excess bias voltage.

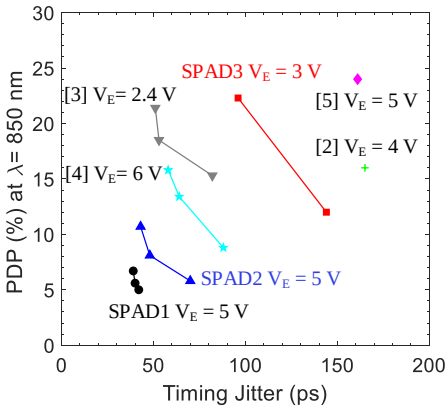

Fig. 12. Performance comparison of the N-on-P SPADs in monolithic CMOS technologies: PDP at 850nm versus timing jitter at similar excess bias voltages.

Table. 1 Performance summary and comparison with N-on-P front-side illuminated SPADs in CMOS technology

Parameter	This work (SPAD 1)	This work (SPAD 2)	This work (SPAD 3)	[2]	[3]	[4]	[5]	[6]
Structure	Shallow NW/PW	Shallow NW/PW	Shallow NW/PW	N+/PW	Deep NW/epi	Deep NW/epi	Deep NW/PW	Deep NW/PW
Technology (nm)	55	55	55	180	90	130	180	180
Pitch (μm)	8.5	8.5	8.5	N/A	N/A	N/A	25	N/A
Avalanche area (μm^2)	15.2	15.2	15.2	78.5	32.1	50.2	206.9	220
Fill Factor (%)	21	21	21	N/A	N/A	N/A	33.1	35
VBD (V)	17.1	20.6	23.0	19.7	14.9	20	20.5	20.0
VE (V)	5	5	3	4	2.4	6	5	5
DCR (cps/μm^2)	19.1	8.7	31.2	30	~4.6	0.36 (V_E = 2 V)	0.6	1.7
PDP Peak (%)	48.9 @450 nm	32.4 @540 nm	41.3 @640 nm	36 @600 nm	44 @690 nm	45.2 @560 nm	64.8 @610 nm	47 @570 nm
PDP (%) @ 850 nm	6.7	10.7	22.3	16	21.4	15.8	24	20
PDP (%) @ 940 nm	2.4	3.7	8.3	N/A	10.1	5.7	8.8	9.7
Afterpulsing probability (%)	3.9[a]	4.5[a]	4.7[a]	50[a]	0.38	0.98	0.49	N/A
Dead time (ns)	100[a]	100[a]	100[a]	750[a]	23	35	24.9	N/A
Timing Jitter (ps) FWHM	39 @850 nm	43 @850 nm	96 @850 nm	165 @790 nm	51 @470 nm	58 @654 nm	161 @635 nm	N/A

[a] This value is significantly overestimated with huge parasitic capacitance due to the lack of integrated circuit.