A 320×232 LiDAR Sensor with 24dB Time-Amplified and Phase-Revolved TDC

Chin Yin, Shang-Fu Yeh, Chiao-Yi Huang, Hon-Yih Tu, Meng-Hsiu Wu, Tzu-Jui Wang, Kuo-Chin Huang and Calvin Yi-Ping Chao
Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, ROC
Tel: (886) 3-5636688 ext 797-8127, email: cyin@tsmc.com

***Abstract*—This paper presents a 320×232, 6.84μm SPAD 3D-stacked BSI LiDAR sensor. With a 24dB Time Amplifier pre-amplifying the Time-of-Flight and a TDC performing phase-revolved conversion, a 3.81ps TDC resolution with [-0.3, 0.4] DNLs is verified. By utilizing time-correlated single-photon counting with the proposed TDC, a 4-bit data compression is demonstrated without sacrificing the image quality. The prototype depth imager achieves 0.5cm distance accuracy and 24 frames/s ToF image rate.**

Keywords—SPAD, LiDAR, ToF, TDC, Time Amplifier

I. Introduction

Depth imaging using light detection and ranging (LiDAR) technology is a key feature in many emerging applications, e.g., autonomous driving, industrial modeling, and interactive AR/VR systems. Direct time-of-flight (D-ToF) method can achieve long-range detection and high frame rates. With powerful pulsed laser and 3D-stacked back-side illumination (BSI) single-photon avalanche diode (SPAD) technology, low system jitter contributed from optics and silicon is achieved. To further realize high depth resolution with large image format, a highly accurate, parallel time-to-digital converter (TDC) is the key component. Flash systems adopt pixel-parallel or group-parallel TDC to reach high frame rates, sacrificing the pixel pitch [1-4], TDC dynamic range and uniformity control. Column-parallel TDC configuration is suitable for narrow pixel pitch, uniform readout quality and practical data throughput.

The flash TDC structure receives multiple time-resolved clock phases from a global delay-locked loop (DLL) block. However, the systematic clock skew decreases the TDC linearity, and the time resolution is limited by the DLL frequency. The conventional D-ToF sensor targets several-centimeters distance accuracy. Time-correlated single photon counting (TCSPC) is utilized to suppress the ambient light interference and jitter distribution, at the cost of huge data oversampling and histogramming. There is a trade-off between TDC dynamic range and the subsequent data processing effort.

In this paper, we propose a column-parallel 24dB time-amplified and phase-revolved (PR) TDC structure optimized for sub-centimeter distance accuracy and data processing reduction. Fig. 1 shows the conceptual architecture, composed of an optical module with uniformly diffused pulsed laser and near Infrared (NIR) lens, a SPAD detector, a front-end time-amplifier (TA) with 24dB gain, and a latch-based TDC circuit. The TDC receives multiple clock phases from the global DLL, and the phase orders are revolved per TDC conversion. Because of the PR multiplexer, we implemented two modes optimized for linearity boost and data compressive.

II. Operation Modes and Principle

A. Linearity Boost Mode

In the linearity boost mode (Fig. 2), all the latch cells in TDC circuit are enabled. The latches sample the monotonic phases from DLL, and reconstruct the latched thermometer codes to binary digits. The intrinsic clock skews from M-stage DLL delay cells cause the differential non-linearity (DNL) of TDC. Then the DLL phase orders are revolved one step in the next TDC conversion, results in one digit shift of DNLs. The DNLs form a fixed pattern cycle due to the nature of DLL that locks the clock in with the clock out of the delay chain. Therefore, after M steps revolution, the DNL cycle finishes a full round of shifts. Because of the oversampling feature of TCSPC, the system collects M multiple times of TDC codes, and the DNLs are self-calibrated to zero after histogram testing theoretically.

B. Data Compressive Mode

In the data compressive mode (Fig. 3a), only one latch cell is enabled. The TDC latches only one phase as least significant bits (LSBs) part, and truncate the lower $\log_2 M$ bits. Then the DLL phase orders are revolved one step at next TDC conversion, which results in TDC intervals shifting by one phase offset. After M multiple times of TDC codes histogramming, a simple average process reconstructs the histogram peak as nominal TCSPC. The data compressive mode effectively reduces the data throughput without TDC LSB codes, and the pre-average process suppresses the front-end jitter represented as full-width half maximum (FWHM) of the histogram (Fig. 3b). The suppression trend follows the oversampling theory. By choosing M=16 and adopting an

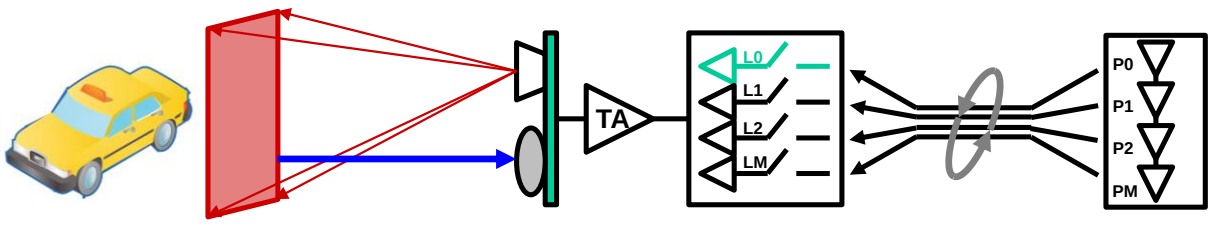

Figure 1. Concept of proposed LiDAR sensor.

averaging process, 4 bits data length is truncated and the FWHM is reduced by 4 times.

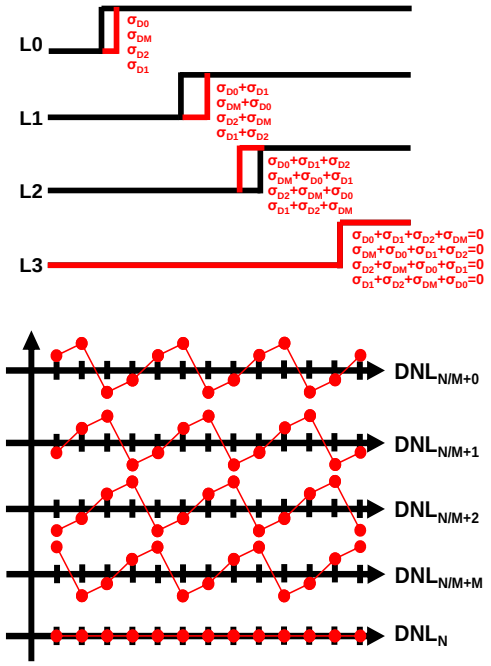

Figure 2. Linearity boost modes

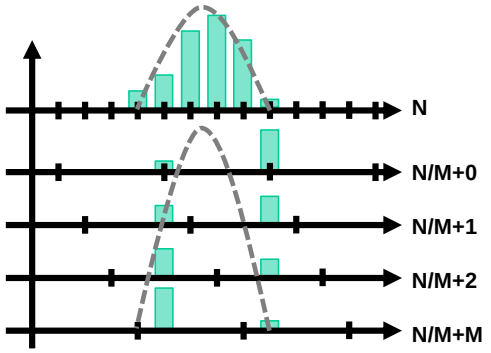

Figure 3a. Data compressive mode

III. Proposed LiDAR Sensor Circuits

Fig. 4 shows the system block and the key circuit component diagrams of this LiDAR sensor. The detector array includes 320×232 6.84μm SPADs fabricated in 45nm BSI CIS node. With 3D stacked technology, the top layer SPADs are pixel-wise bonded with the bottom layer of active quenching and re-charging (AQRC) circuits in 22nm logic process. The peripheral parts include a column-parallel digital timer co-operated with AQRC pixel for SPAD hold-time control, a row selector for D-ToF line scanning, a column TA to extend the succeeding TDC dynamic range, a column PR TDC and counter receiving the multiplexed clock phases from global PLL and DLL, the column serializer controlled by APR processor, and a low-voltage differential signaling (LVDS) interface transferring data for off-chip processing.

A. Active Quenching and Re-Charging

In the pixel-parallel AQRC (Fig. 5), the effective quench resistance is controlled by a quench bias voltage, and the hold-time is controlled by either the internal switch-capacitance integrator or the column AQRC timer.

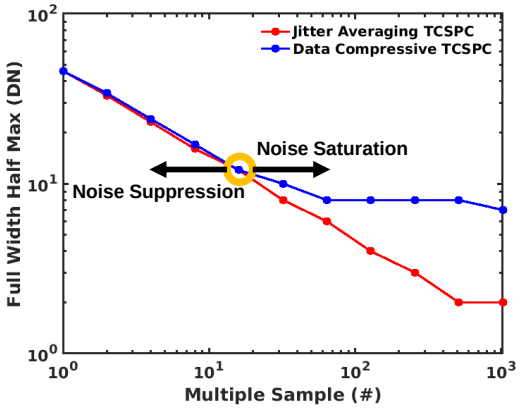

Figure 3b. Data compressive mode jitter

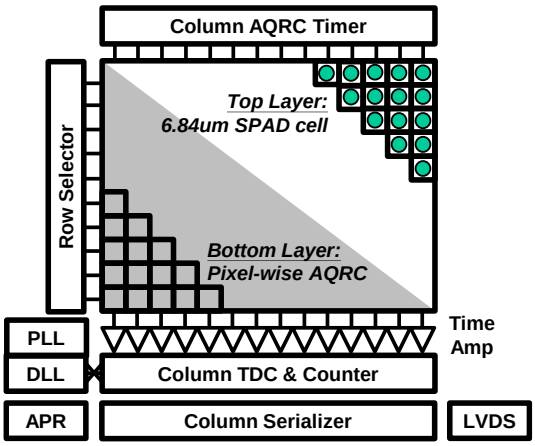

Figure 4. System block diagram

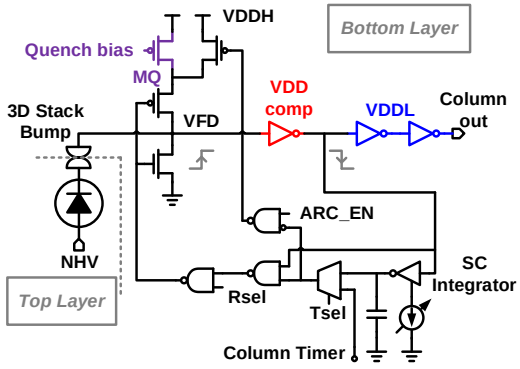

Figure 5. Pixel-parallel AQRC

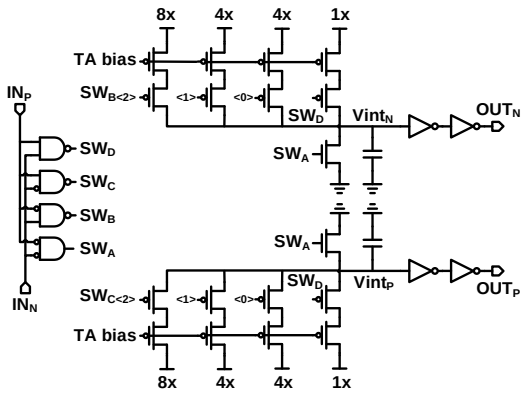

Figure 6. Time amplifier

B. *Time Amplifier*

At the initial state of time amplifier (Fig. 6), both $Vint_P$ and $Vint_N$ are reset to low. Once the IN_N receives a rising edge first, the SW_B turn on and $Vint_N$ start to be integrated by a large current. After certain time-of-flight interval, IN_P is triggered to high, controlling both $Vint_P$ and $Vint_N$ to be integrated by a small current (SW_D). $Vint_N$ reaches the inverter threshold first followed by $Vint_P$, and the time amplification ratio between $OUT_{P/N}$ and $IN_{P/N}$ is proportional to the current ratio between SW_B and SW_D. We choose 4×, 8×, 16× gain ratios in this design.

C. *Phase-Revolved TDC*

In the proposed PR TDC circuit (Fig. 7), 1GHz differential clocks CK_{INP} and CK_{INN} are delayed and locked by the 8-stage global DLL block, providing total 16 equivalent delayed phases. The 16 phases are multiplexed to each column TDC circuit, which includes 16 latch cells as LSBs part and 8-bit ripple counters as MSBs part. The latches are event-driven by the preceding SPAD event, and the latched thermometer codes are combined with MSB parts to form a 12-bit TDC output. Two identical TDC circuits per column are used to achieve digital corelated double sampling (DCDS) purpose. The multiplexed 16 phase orders are revolved according to the frame index signal, to realize either linearity boost or data compressive functions.

D. *Operation Timing diagram*

Fig. 8 is the timing diagram of the proposed LiDAR sensor with TA and PR TDC. The 232 lines are scanned sequentially into one frame. In one line period, a LASER pulse is emitted and reflected, triggering the SPAD to avalanche at V_{FD}. The V_{FD} falling edge enable the hold time control, which limits only one pulse within TDC window. A reference LASER starts (IN_N) and the SPAD column-out (IN_P) inputs to the TA, and the time interval is amplified by up to 16× times. The amplified signals ($OUT_{P/N}$) are sent to the TDC. Two input signals are converted by dual TDC circuits separately, and processes the DCDS result. In mode 1, all the latches are enabled, while in mode 2, only the first latch is activated. The DLL outputted phase orders are revolved with frame index, effectively flattening the clock skew. The TDC 12-bit result is then stored into line buffer, and output through LVDS driver serially at next line time.

IV. Measurement and Specification

Fig. 9 presents the measurement setup. The LiDAR system applies 940nm 100W 20° beam angle pulsed VCSEL diode and the sensor part is assembled with F1.4 8mm lens and 940nm BPF. The in-lab targets under test and environment are limited to a range of a few meters.

A. *Linearity Boost Mode*

Fig. 10 shows the characterization result. After the proposed PR self-calibration, the DNLs are improved from [-0.9, 0.9] to [-0.3, 0.4]. The clock-induced skews are flattened and the DNLs are only limited by the clock tree routing mismatch. The transfer curves of the proposed TDC without and with TA in 4×, 8×, 16× gains are measured. The gain slopes follow the TA current design, with saturation levels slightly shifted by switch coupling effect. In the ground-truth distance measurement, 0.5cm depth accuracy is achieved across 100 centimeters measured range.

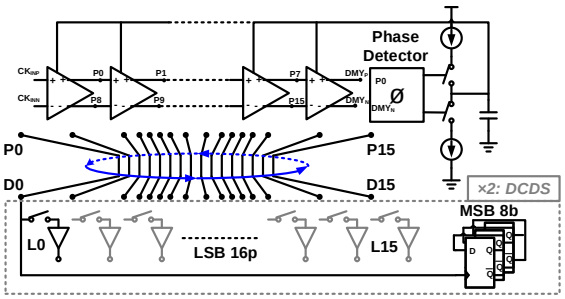

Figure 7. Phase-revolved TDC

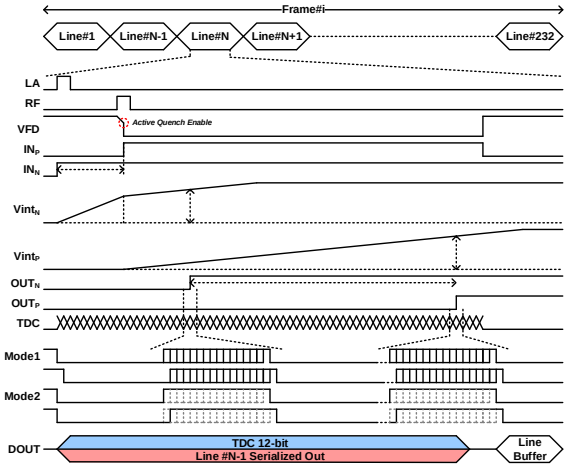

Figure 8. Timing diagram

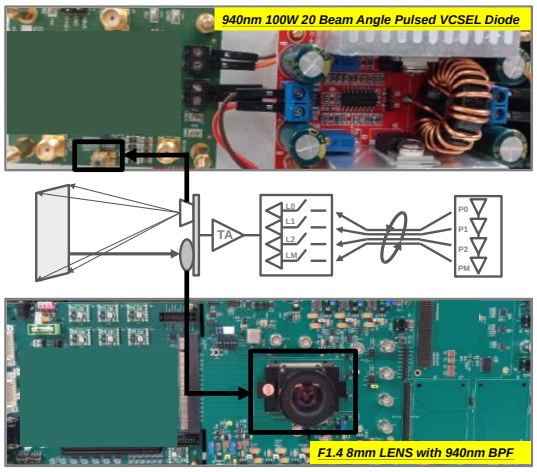

Figure 9. Measurement setup

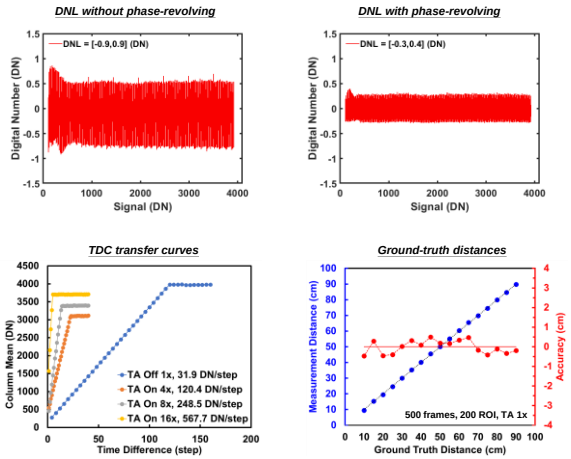

Figure 10. TDC characterization, Time-amp linearity, ground-truth

B. *Data Compressive Mode*

Fig. 11 collects 10000 frames for depth image and histogramming demonstration. Comparing to nominal TCSPC depth image, the PR TDC reconstruct the 16× (4-bit) data compression depth image without sacrificing the image quality.

C. *Performance*

The performance compared with state-of-the-arts are listed in Fig. 12. The 6.84μm pitch 320×232 LiDAR sensor reaches a 3.81ps TDC resolution with [-0.3, 0.4] DNLs by proposed time-amplified and phase-revolved functions. Fig. 13 shows the micrograph of this 3D stacking LiDAR sensor and the performance summary, a total 96dB dynamic range, a 0.5cm distance accuracy and 24 frames/s ToF image rate are achieved.

V. Conlusion

This 320×232, 6.84μm SPAD 3D-stacked BSI LiDAR sensor integrates AQRC circuit, 24dB Time Amplifier and a 3.81ps resolution with [-0.3, 0.4] DNLs TDC for TCSPC operation. The 4-bit data compression depth image is demonstrated, and the 0.5cm distance accuracy with 24 frames/s ToF image rate are measured. The 3D depth model presents sub-centimeter depth resolution (Fig. 14).

Acknowledgment

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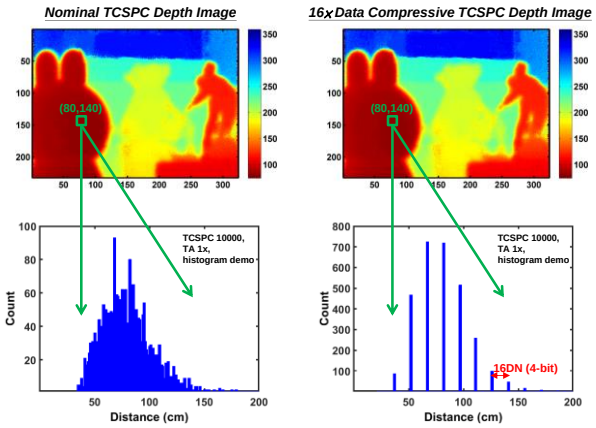
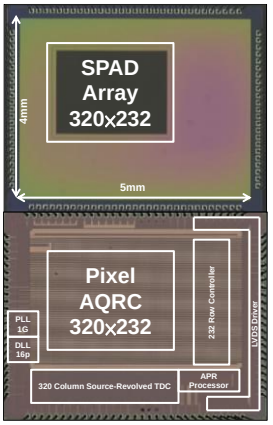


Figure 11. Demo of of TCSPC depth images wo/wi data compression

Parameter	Unit	This Work	[1]	[2]	[3]	[4]
Technology	nm	45/22 SPAD CMOS	45/22 SPAD CMOS	90/40 SPAD CMOS	110	110
TOF format (H×V)	-	320×232	256×128	168×63	80×60	64×64
TOF method	-	Direct	Direct	Direct	Hybrid	Direct
Pixel pitch	μm	6.84	7	10	75	48
SPAD structure	-	AQ+ARC	Coin.	Coin.	Hist	Coin.
TDC architecture	-	Column	256-to-1	9-to-1	6-to-1	Pixel TDC
TDC depth	bit	12 & TimeAmp	14	12	13	16
TDC resolution	ps	Intrinsic:61 TA 4×:15.25 TA 8×:7.63 TA 16×:3.81	60	1000	100	250
TDC linearity (DNL)	DN	+0.4/-0.3	±0.05***	N/A	N/A	+0.79/-0.61
LASER projection	-	Flash	Flash	Flash	Flash	Flash
Wavelength	nm	940	780	905	905	905
Distance range	m	256/10*	100	200/150	45	8.2
Distance accuracy	cm	0.5	7	15-30	2.5	15
Repetition rate	Hz	2400	500k	N/A	100k	6250
TOF image rate	fps	24**	N/A	20	30	25

* Optical limitation
** 100 frames TOF
*** After Calibration

Figure 12. Comparison table



Process		45nm 0P4M SPAD 22nm 1P7M Logic
Supply voltage		NHV SPAD 2.5V AQRC 0.9V Digital
Number of pixels		320 x 232
Pixel size		6.84μm x 6.84μm
TDC depth		12-bit
TDC resolution	1x	61ps
	4x	15.25ps
	8x	7.63ps
	16x	3.81ps
TDC jitter		0.9DN
Dynamic range		72+24dB @ 16x
TDC DNL, 12-bit		-0.3 < DNL < 0.4 LSB
TDC INL, 12-bit		-3.3 < DNL < 2.6 LSB
Distance accuracy		0.5cm
TOF image rate		24fps
Die size		5mm x 4mm

Figure 13. Chip micrograph and summary

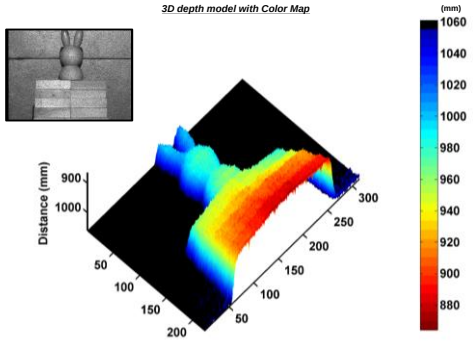


Figure 14. 3D depth model