Recent advances in SPAD sensor technology: Pixel size shrinking and PDE enhancement

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Abstract: Recent advances in SPAD device technology and photon-counting architecture for small pixel sizes are introduced herein. Pixel sizes have been reduced to 3 μm while the peak PDE is increased to 82.5 % and the DCR is maintained at 2.2 cps. The PDE at a wavelength of 940 nm is further increased to 36.5 % for 6-μm-pitch pixels by implementing shallow trenches on the front side of Si surface and an optimized pyramid structure on the back side of Si surface, a 2 × 2 on-chip lens, and full trench isolation. Meanwhile, 3.36-μm pixel-pitch photon-counting is achieved using only an 8-bit in-pixel counter by employing clustered multicycle clocked recharging, intermediate most-significant-bit read out, and amplitude limitation achieved using a clipping transistor. More advanced device structures increase robustness against voltage drops with large multiplication currents via an embedded metal contact, a power grid on deep-trench pixel isolation, and a poly-Si resistor on SPAD.

I. Introduction

SPAD pixels have been developed for time of flight (ToF) range image sensors [1-3] and photon-counting image sensors [4-6] through the exploitation of their single photon sensitivity and sub-nanosecond-level timing resolution. Recently, back-illuminated SPAD stacked with a pixel- front-end (PFE) circuit via Cu–Cu connection has been proposed, which allows the SPAD pixel fill factor and photon detection efficiency (PDE) to be increased by reducing the SPAD pixel size and integrating more advanced PFE circuits.

K. Ito and O. Kumagai reported back-illuminated 10 μm SPAD pixels [7] and their application for ToF depth sensor [3]. The above mentioned SPAD pixel comprises a 7-μm-thick silicon layer, an on-chip micro-lens (OCL), a metal reflector, and full trench isolation (FTI) with buried metal. The structure combined with drift potential optimization can improve the PDE to 14 % at a wavelength of 940 nm with 0.30 % optical-crosstalk suppression. The dark count rate (DCR) is approximately 3 cps at room temperature and the timing jitter is 173 ps with 3 V excess bias. The LiDAR system was developed by integrating an advanced circuit constructed using SPAD pixels. The system can detect objects 150 m ahead with less than 0.1 % measured error even if the reflectance is less than 10 % under day light.

II. Pixel-size reduction and PDE enhancement

S. Shimada and Y. Fujisaki have attempted to decrease the SPAD pixel size to 6 [8], 3, and 2.5 μm [9] while enhancing the PDE [10]. The peak PDE was increased to 82.5 %, the PDE at a wavelength of 940 nm exceeded 26.5 %, and the DCR was 2.2 cps at room temperature under 3.3 μm pixels and 3 V of excess bias. The high PDE was achieved by implementing a gapless OCL and a pyramid surface for diffraction (PSD) structure. The sufficiently low DCR was achieved by optimizing the multiplication layout design to increase avalanche guard ring width (Fig. 1). The small SPAD improve the robustness of depth sensing against ambient light by decreasing the count loss under a high incident optical power.

The PDE at a wavelength of 940 nm was further enhanced to 36.5 % for a 6-μm-pitch pixel by implementing a shallow trench for diffraction (STD) on the front side of Si surface, a 2 × 2 OCL, an optimized PSD, and optimized FTI (Fig. 2) [10]. The optimized PSD and STD can increase the optical path in the SPAD pixel. The 2 × 2 OCL enhances the effect of the STD as its layout is highly compatible with the STD layout. The optimized FTI can reduce light absorption on the FTI interface, thus enhancing the PDE by more than 5 %.

III. Photon-counting image sensor

High-resolution and high-dynamic-range (DR) photon-counting image sensors have been reported by reducing the SPAD pixel size and power consumption. J. Ogi demonstrated an extrapolating architecture that can decrease the in-pixel counter bit and power consumption by limiting the counting number, even under a high incident optical power with a 12.24-μm-pitch pixel [4].

T. Takatsuka reduced the pixel pitch to 3.36 μm using only an 8-bit in-pixel counter by employing clustered multicycle clocked recharging (CMCR), intermediate most-significant-bit read out (MSB-Read), and amplitude limitation achieved using a clipping transistor (Fig. 3) [11]. The CMCR can limit the maximum number of counting photons with nonlinear counting response, thus increasing the DR while reducing power consumption. The MSB-Read expands the counter bit by detecting the number of in-pixel counter saturation and then storing the number in the SRAM outside the pixel array. This can increase the SNR to more than 30 dB under bright light. The clipping transistor limits the amplitude to less than 0.8 V by maintaining the SPAD bias voltage at approximately 3 V. Most PFE circuits can be constructed using low-voltage transistors with the amplitude limitation and a minimized circuit area via the 22-nm-node logic process. The 3.36-μm-pitch photon-counting image sensor indicated a 120-dB DR under a frame rate of 150 fps as well as 104 mW of power consumption under a frame rate of 60 fps.

IV. Challenge of reducing pixel via new structure

J. Ogi has developed more advanced structures to reduce the pixel pitch and increase robustness against voltage drops with large multiplication currents for high-resolution photon counting. An embedded metal contact, a power grid on deep-trench pixel isolation, and a poly-Si resistor on SPAD have been reported (Fig. 4) [12]. The embedded metal contact suppresses edge breakdown by separating the anode and cathode regions vertically. The embedded power grid decreases the resistance of the power-supply wiring and suppresses voltage drops via multiplication currents, even in a large scale SPAD pixel array for high-resolution photon counting. The poly-Si resistor decreases the multiplication current by reducing the voltage-swing amplitude at the input node of the output inverter.

V. Conclusion

Table I shows a comparison of the SPAD pixel performance, and Table II shows a comparison of the performance of photon-counting image sensors. 3 - 6 μm pitch SPAD pixels have been reported with the high PDE and a low DCR. Additionally, T. Takatsuka achieved the smallest pitch for a photon-counting image sensor, with competitive characteristics.

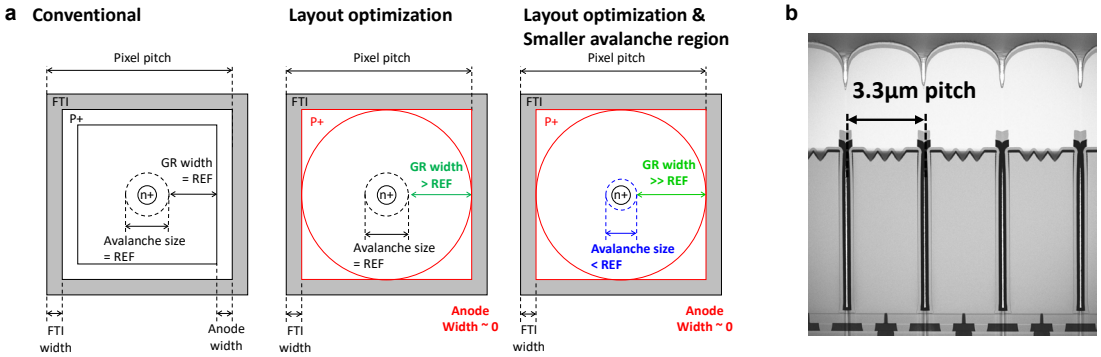

Fig. 1 (a) Concept of the layout optimization less than 3.3-μm-pitch pixel and (b) cross-sectional TEM image of fabricated SPAD pixel.

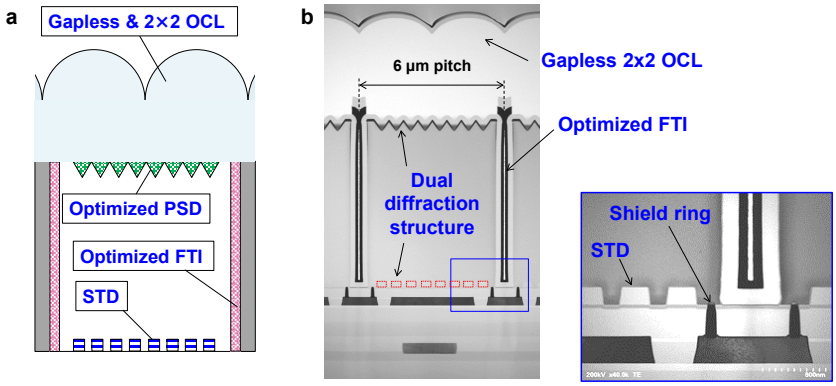

Fig. 2. (a) Concept of the PDE enhancement at 940nm wavelength and (b) cross-sectional TEM image of fabricated SPAD pixel

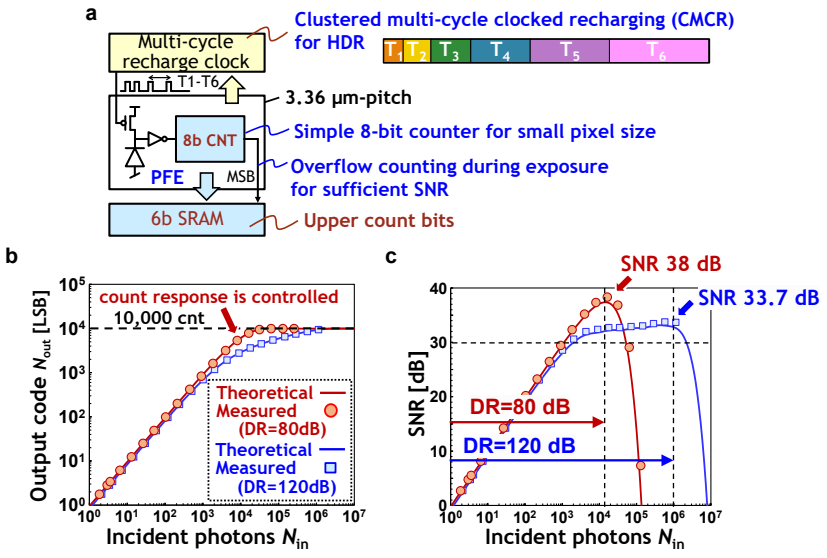

Fig. 3. (a) Concept of the 3.36-μm-pitch photon counting image sensor and measurement results of (b) counting response and (c) SNR.

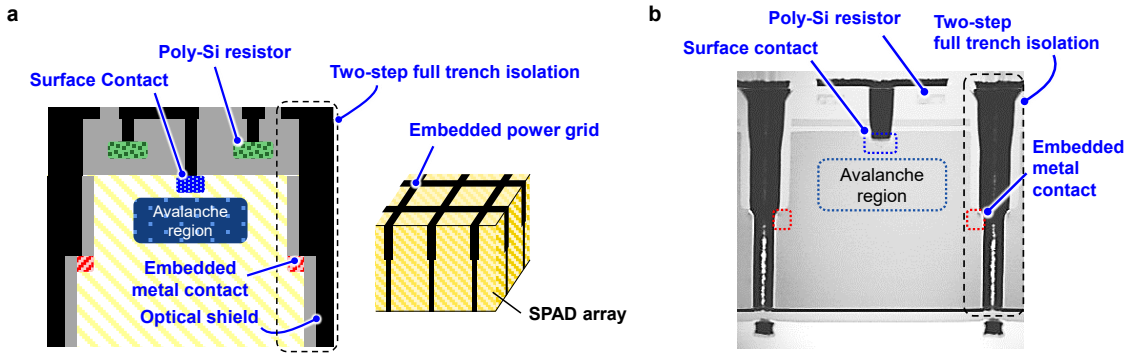

Fig. 4. (a) Concept of the 3.36-μm-pitch pixel with embedded metal contact, embedded power grid and poly-Si resistor on SPAD pixel, and (b) cross-sectional TEM image of the fabricated pixel

Table I Comparison of pixel performance.

	Unit	IEDM 2016 [13]	IISW 2017 [14]	JSTQE. 2018 [15]	ISSCC 2019 [2]	Optics 2020 [16]	IEDM 2021 [17]	IISW 2023 [18]	IEDM 2020 [7]	IEDM 2021 [8]	IEDM 2022 [9]		VLSI 2023 [10]	IISW 2023 [12]
Pixel pitch	μm	7.83	3	5	9.2	4	6.39	10.17	10	6	3.3	2.5	6.0	3.06
Array size	-	128 × 120	4 × 4	N/D	256 × 256	4 × 4	2072 × 1548	N/D	N/D	N/D	N/D		N/D	160 × 264
Techno-logy	-	BI-3D 65nm	FI 130nm	FI	BI-3D 90nm	FI 180nm	BI-3D 90nm	BI-3D 65nm	BI-3D 90nm	BI-3D 90nm	BI-3D 90nm		BI-3D 90nm	BI-3D 90nm
V_{bd}	V	12	15.8	N/D	28.5	22.1	30	18.6	20	22	19	18	22	20.9
V_{ex}	V	3	1.2	5.8*3	2.5	6	2.5	3.5	3.0	3	3	3	3.0	3
Peak PDE	%	11.6	6*3	12*2*3	23	14.2	69.4	34.4*2*3	53.5*1	69.4*1	82.5	76.1	88.4	57
PDE at 940nm	%	3.2	~1	N/D	N/D	N/D	24.4	22	14.2	20.2	22.5	20.4	36.5	N/D
DCR @25°C	cps	10974	1343	17.3*3	20.3	2.5	1.8	8.6*3	3	19	2.2	173	10	15.8
Jitter FWHM	ps	205	185	N/D	N/D	72	100	103	172	137	196	214	209	N/D
Cross-talk	%	N/D	<0.2*4	4.9*3	N/D	3.57	N/D	N/D	N/D	0.5	0.85	1.0	1.12	<0.4

*1 Referred from [12], *2 No data of the peak PDE. The largest value in the article is used.
*3 No numerical value is expressed in the article; Author estimates the value from the graphs in the article. *4 V_{ex} = 1 V.

Table II Performance comparison of SPAD photon counting image sensor.

	Unit	Sensors2018 [19]	ISSCC2019 [2]	Optica2020 [20]	ISSCC2022 [6]	ISSCC2021 [4]	VLSI2023 [11]
Pixel pitch	μm	8.25	36.8 x 9.2	9.4	9.585	12.24	3.36
Pixel array	Pix	96 × 40	64 × 256	1024 × 1000	960 × 960	264 × 160	748 × 448
CMOS Technology	Nm	40	Stacked 90 / 40	180	Stacked 90 / 40	Stacked 90 / 40	Stacked 90 / 22
In-pixel counter	Bit	12	28	1	11+3bit latch	9	8
Max. frame rate	fps	60	30	0.45	90	250	150
Dynamic range	dB	109	129	108.1	143	124	120
SNR Max.	dB	~40	>40	30.5	33	40	33.7
SNR dipped	-	30	No dip	29.5	24	No dip	No dip
Motion artifact Suppression	N/A	No	Yes	No	No	Yes	Yes
Power	mW	N/D	N/D	284 @0.45fps	370 @30fps	N/D	104 @60fps
Normalized at 1Mpix, 60fps				73,958	803		310

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