A 55nm BCDLite® FSI SPAD with Improved NIR Sensitivity and DCR

Francesco Gramuglia, Eng Huat Toh, Ping Zheng, Yongshun Sun, Yew Tuck Chow, Deepthi Kandasamy, Li Fei Tan, Alban Zaka, Vinit Dhulla, Sally Chwa, and Elgin Quek

***Abstract*—In this paper, we introduce a first-generation industrialized CMOS SPAD utilizing standard GlobalFoundries 55 nm BCDLite® technology. Addressing challenges associated with advanced technology nodes, we focus on enhancing device sensitivity, reducing noise, and maintain timing performance. Engineered doping profiles result in a notable performance boost compared to the previous SPAD generation in this technology, yielding a 12 μm diameter device with an 18 V breakdown voltage and ∼167.0 mcps/μm^2 median DCR at 25°C with 1 V excess bias. The upgraded structure achieves a PDP of 2.0% at 940 nm, and a timing jitter of <150 ps FWHM when measured with external resistor quenching at 1 V excess bias.**

***Index Terms*—Single-photon avalanche diodes (SPADs), BCDLite® technology, single photon timing, single-photon counting, time-of-flight, ranging**

I. Introduction

THE increasing demand for performance, cost reduction, and continuously emerging new applications is driving the attention of semiconductor device ecosystem in spending energy developing single-photon avalanche diodes (SPAD) in a variety of standard technology nodes [1]–[8]. Following this trend, GlobalFoundries (GF) exploited the potential of its 55BCDLite® technology, starting from [8], to develop the first generation of devices in 55 nm. In the presented work we provide details on the device structure and its achieved performance, in terms of breakdown voltage (VBD), Photon detection probability (PDP), dark count rate (DCR), and timing jitter. All the measurements have been performed on single devices with external quenching resistor, at wafer level.

II. The Device

The SPAD tested by GF in 55 nm BCDLite® technology is based on a cross section similar to what was presented in [8]. The top part of Fig. 1 shows the 2D distribution of doping concentration (*a*) and electric field (*b*) obtained from TCAD simulations. The avalanche multiplication region is located at the junction between a deep-PWell (DPW) and a deep-NWell (DNW) implants. To prevent premature edge breakdown, we adopted a virtual guard ring (GR) strategy.

Francesco Gramuglia, Eng Huat Toh, Ping Zheng, Yongshun Sun, Yew Tuck Chow, Deepthi Kandasamy, Li Fei Tan, Alban Zaka, Sally Chwa, and Elgin Quek are with GlobalFoundries Ltd. e-mail: (francesco.gramuglia@globalfoundries.com, enghuat.toh@globalfoundries.com, ping.zheng@globalfoundries.com, yongshun.sun@globalfoundries.com, yewtuck.chow@globalfoundries.com, deepthi.kandasamy1@globalfoundries.com, lifei.tan@globalfoundries.com, alban.zaka@globalfoundries.com, vinit.dhulla@globalfoundries.com, siowlee.chwa@globalfoundries.com, elgin.quek@globalfoundries.com).

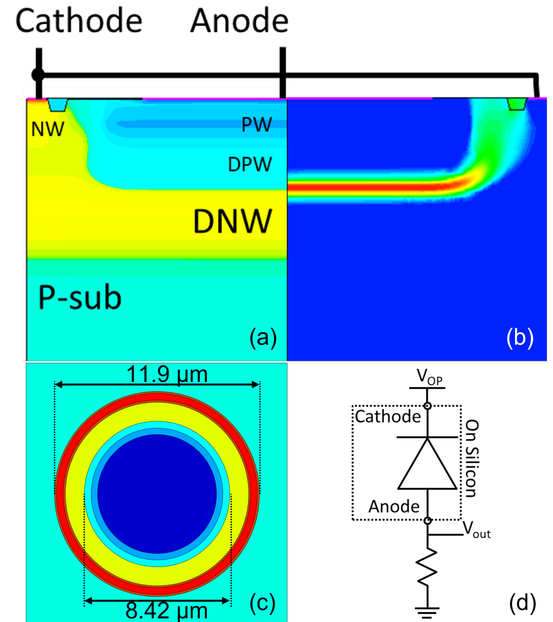

Fig. 1. On the *top*: doping concentration (*a*) and electric field (*b*) 2D profile. On the *bottom*: schematic device top view (*c*) and measurement setup with external quenching resistor (*d*).

The SPAD we present has circular shape with a diameter of ∼12 μm, and a geometrical fill factor of ∼50% (Fig. 1 *(c)*).

III. Measurement Results

As clear from the TCAD simulation results (Fig. 1b), the high electric field is uniformly distributed along the primary junction, showing the effectiveness of the GR. This result is also confirmed by the light emission test (Fig. 2a), where a uniform light emission is observable from the whole device active area.

The breakdown voltage (VBD) was extracted from the I-V characteristic, measured on the devices without quenching load, at several temperature points.

A profile optimization yielded a substantial reduction of VBD, resulting in a room temperature value of ∼18 V (compared to the ∼32 V of [8]). Further, Fig. 2b show the VBD median trend over temperature of our device. The VBD temperature coefficient results 15.3 mV/K, significantly improved with respect to what reported in [8] (∼30 mV/K).

The other device parameters were characterized at wafer level using the passive quenching configuration shown in Fig. 1 *(d)*, where an external quenching resistor is connected in series

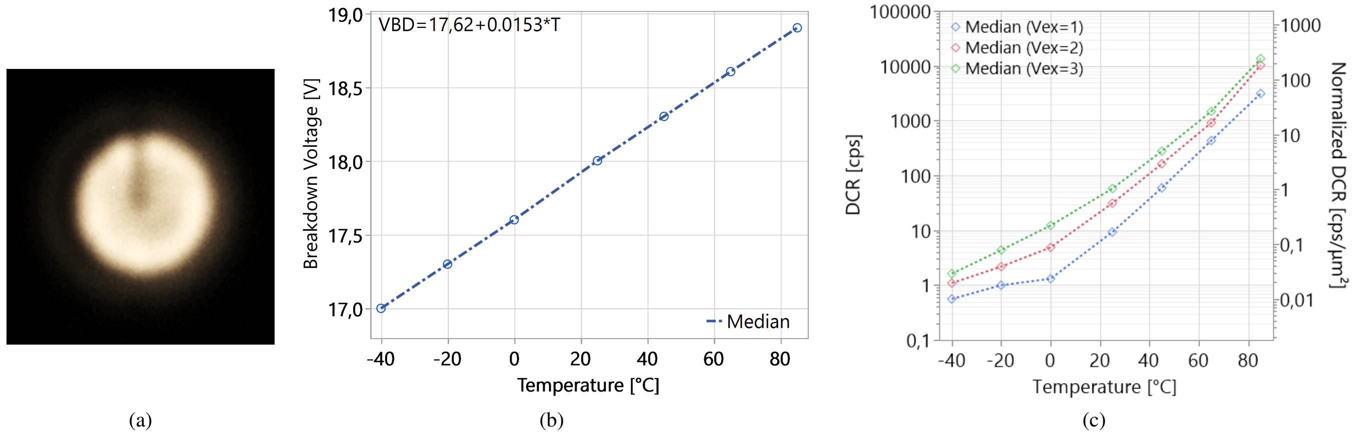

Fig. 2. *(a)*: Light emission test (LET) of the device. The measurement is performed with a constant bias of 4 V Vex. *(b)*: VBD trend over temperature. *(c)*: Median DCR dependency over temperature for three bias points.

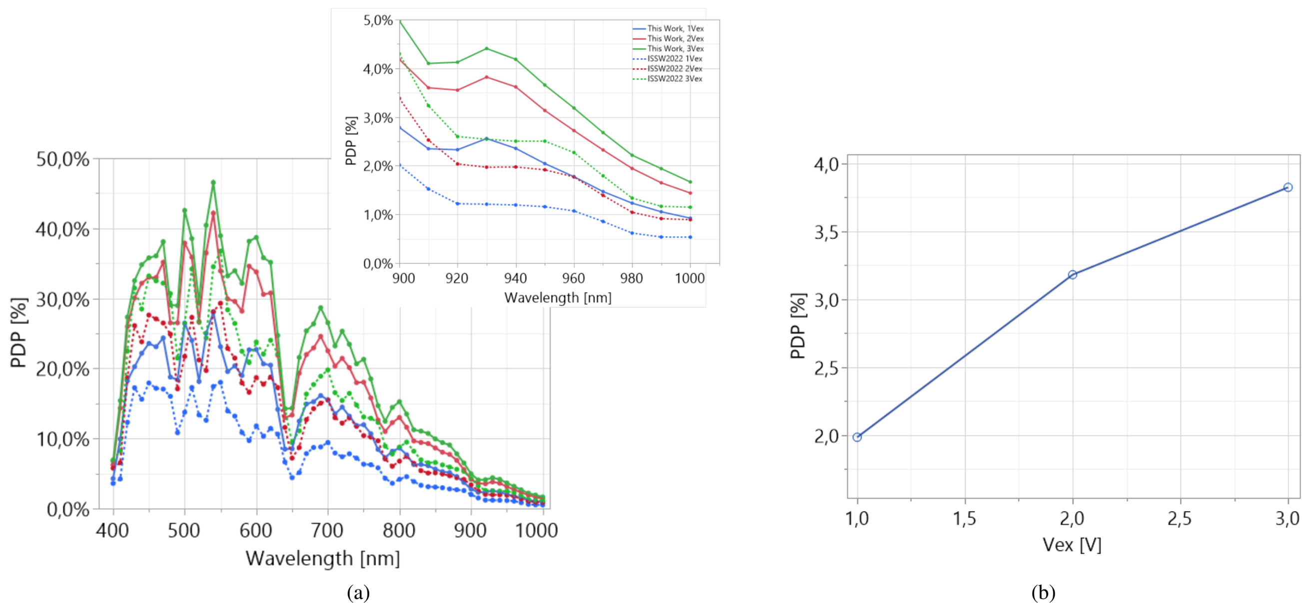

Fig. 3. Full spectrum PDP comparison with ISSW2022 performed on a single device (*a*), and the median PDP at 940 nm for three bias conditions from wafer-level testing (*b*).

with the SPAD anode.

The DCR was measured at 1 V, 2 V, and 3 V excess bias (V_{ex}) and the median results are shown in Fig. 2c. The DCR show a clear dependency on the temperature, highliting a knee point (point from where the tunneling contribution becomes dominant) at approximately 0°C. Morever, the device shows a low noise that does not exceed 1 kcps up to about 65°C.

The full spectrum PDP was measured on one sample and compared with the same device presented in [8]. The results are shown in Fig. 3a, and a considerable boost of performance in the order of 50% is noticeable for both 550 nm and 940 nm. The tested device reaches, indeed, a PDP of 47% at 550 nm and 3 V Vex and about 4.2% at 940 nm.

We also present the median value of the PDP for our device, measured with 940 nm monochromatic continuous light at wafer level on a pool of 15 sample devices, and the results are shown in Fig. 3. The median PDP reaches 2% at 1 V V_{ex}, arriving to almost 4% at 3 V V_{ex}. It is worth noting that for the presented devices was not implemented the *canyon* structure presented in [9]. The use of this solution is expected to boost even more the PDP performance, making the spectrum smoother and eliminate the dip at 650 nm.

Finally, Fig. 4 shows the timing jitter results, defined as the FWHM of the instrument response function (IRF). The measurement was performed with a 940 nm picosecond laser and it reaches a value of 149 ps at 1 V V_{ex}. As expected, the results improves increasing with the bias, reaching ∼136 ps at 3 V V_{ex}. It is important to note that the measurement was performed with an external quenching resistor. The use of an integrated pixel circuit is expected to improve significantly these results.

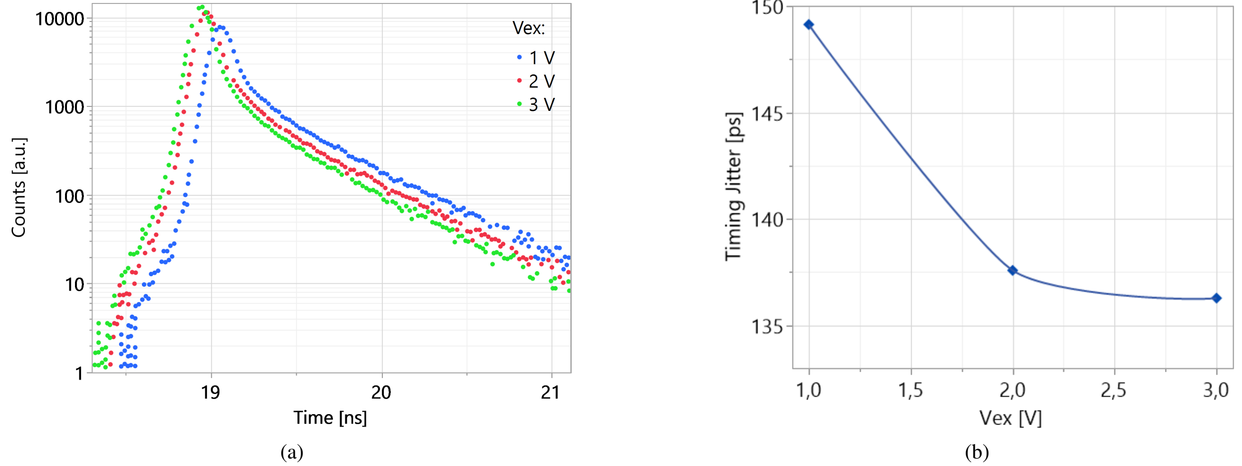

Fig. 4. Device IRF at three different Vex (*a*), and the corresponding timing jitter values (*b*). The jitter is measured as the FWHM of the IRF.

IV. Conclusion

In this work we presented our first generation of SPADs evaluated in 55 nm BCDLite® technology. The presented device, taking [8] as starting point, went through an optimization process to boost its performance beyond the level of its precursor. This new SPAD shows a breakdown voltage of 18 V at room temperature with a temperature coefficient of 15.3 mV/K, making it a good candidate for consumer applications, also considering the reasonably high integration degree provided by the 55 nm node used. Moreover, the uniformity of the LET shows absence of premature edge breakdown, and the device functionality was demonstrated in the range of temperature from -40°C to 85°C.

Table I summarizes the performance of the industrially available FSI isolated [10] SPADs compared to this work. Considering the use of a sub-65 nm technology, our SPAD ranks well within the state-of-the-art. It shows low noise at room temperature (9 cps or 0.16 cps/μm^2, at 1 V V_{ex}), and remaining below 1 kcps (17.9 cps/μm^2) up to about 65 °C. Moreover, the median PDP witout *canyon* and without microlenses results 2.0%, 3.3%, and 3.7% at 1 V, 2 V, and 3 V V_{ex} respectively. Finally, the timing jitter, measured with an external resistor for passive quenching, is 149 ps at 1V V_{ex}. The optimization of optical stack and the possible use of microlenses, and the integration of an active pixel circuit can definitely improve the device performance well beyond the reached level.

Further measurement campaigns are currently ongoing and the results will be shown at the time of the conference.

	Units	**This Work**	**ISSW2022** [8]	[5]	[4]	[11]
Technology node	nm	**55**^{a}	55^a	130	40	55
Pixel size	μm	**11.9**	11.9	∼20.5	na	na
Fill factor	%	**∼50**	∼50	∼15.2	70^a	25
VBD	V	**18**	32	13.82	15.5	17.7
VBD Temp. coeff.	mV/K	**15.4**	30.8	9.4	na	16
DCR (25°C, 1 V)	cps	**9**	90	∼80	50	na
DCR (25°C, 2 V)	cps	**30**	200	∼400	na	na
DCR (25°C, 3 V)	cps	**56**	350	∼1000	na	0.28 / μm^2
PDP (1V, 940nm)	%	**2.0**	0.8	1.4	1.7^b/2.2^a	na
PDP (2V, 940nm)	%	**3.3**	1.2	na	na	∼1.3
PDP (3V, 940nm)	%	**3.7**	1.8	na	na	1.5
Timing jitter (1 V)	ps	**149**	95	>140^c	170	>126^d
Integrated pixel	-	**no**	yes	yes	yes	no
Microlenses	-	**no**	no	no	yes	no

^{a} with microlenses; ^{b} without microlenses; ^{c} reported at 1.2V; ^{d} reported at 1.5V.

TABLE I
Performance summary comparison.

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