Transient Measurements of Avalanche Dynamics and Quenching in SPADs

Wilfried. Uhring^{1*}, Dolatpoor Lakeh¹, F. Calmon², A. Bianchi³, D. Rideau³, G. Gouget³, A. Dartigues³, R. Neri³; F. Brun³, S. Rink^{1,3}, J-B. Kammerer¹, J-B. Schell¹, C. Lallement¹, D. Goloanski³, A. Juge³, E. Lacombe³

¹ICube, University of Strasbourg and CNRS, UMR CNRS 7357, 67440 Strasbourg, France

² Univ Lyon, INSA Lyon, CNRS, Ecole Centrale de Lyon, Université Claude Bernard Lyon 1, CPE Lyon, INL,

UMR5270, 69621 Villeurbanne, France

³ STMicroelectronics, Crolles, France & United Kingdom

Abstract—It is crucial to understand the avalanche phenomenon in SPADs in order to optimize their design and implementation. This phenomenon is well described in static operation in the literature, but its dynamic and stochastic aspect is much less so. In order to create a more realistic behavioral model, it is necessary to be able to finely observe the transient and random aspect of the phenomenon. Unfortunately, very few studies show exploitable measurement results, especially in the case of small SPADs integrated into standard CMOS technology. In this article, we describe solutions that allow direct electrical measurements of the behavior of a SPAD made in standard CMOS technology processes within a pixel. The technique has been applied to several versions of SPADs and pixels with or without active quenching. The measurement results obtained help to better understand the behavior of SPADs and to model their stochastic behavior.

Index Terms— SPAD, wideband analog characterization, buffer transient measurement, SPAD avalanche dynamics, Quenching, Characterization of stochastic responses

I. INTRODUCTION

Observing physical phenomena is a key step in understanding and modeling them. SPADs are components whose behavior is strongly stochastic by the very nature of the avalanche phenomenon. The macroscopic behavior is governed by interactions at the particle level. SPADs are generally characterized by high-level abstract figures of merit such as dark count rate (DCR), quantum efficiency, after pulsing (AP), or photon detection efficiency (PDE). Unfortunately, usual performance parameters, even jitter, do not provide indications on the temporal behavior of the SPAD, and very few studies focus on the fine characterization of the transient response. In this article, we describe solutions that allow direct electrical measurements of the behavior of SPADs made in standard CMOS technology processes within a pixel.

II. PRINCIPLE

Several articles [1][2] discuss the transient TCAD simulation of SPAD avalanche. The results indicate that the buildup of the avalanche current is a very fast process with a rise time of a few picoseconds. Therefore, directly measuring the SPAD terminal's current and voltage is a challenging task. This is because it requires a high bandwidth and a low added parasitic capacitance. For instance, in [3], a pad for a pico-probe was integrated on the chip, leading to a total capacitive load of 275 fF in the 90 μ m diameter large SPAD's node, almost twice the SPAD capacitance of 150fF. This solution is clearly not feasible for a small SPAD of a few fF. In order to measure the SPAD terminal voltage with both high bandwidth and low parasitic capacitance, we embedded an analog wideband buffer within the pixel. To achieve this goal, a simple yet robust method is to use a cascade of source followers. Four cascaded source followers with alternate N and P types are used. The size of the transistors and current sources is increased from an almost minimal value to a large enough value to drive a 50 Ohm wideband oscilloscope input. The current can be extracted from the analog voltage across the SPAD.

Figure 1 provides a first example of the technique with measurements of both the anode and cathode voltage. The anode voltage can be directly connected to the analog buffer input since its dynamic is compatible with the maximum rating voltage. On the contrary, the cathode as to be AC coupled due to the presence of the high voltage VHV not compatible with the maximal rating voltage of the analog buffer. The cathode voltage is, by the way, attenuated thanks to the capacitive bridge divider. The offset, analog buffer gain and capacitive bridge divider attenuation are compensated by post processing in order to determine the real SPAD terminal voltages.



Fig. 1. First example of an on-pixel analog buffer implementation. One analog buffer is dedicated to one pixel only.



Fig. 2. Second example of a on pixel analog buffer implementation. An analog multiplexer allows to connect an analog buffer input to a required pixel.

Figure 2 shows another configuration where the SPAD is quenched from the bottom. In this case, the cathode is directly connected to a static high voltage, which is not required to monitor. Multiple pixels can be monitored with the same analog output by selecting the pixel thanks to an analog multiplexer. The first stage of the analog buffer is integrated in a pixel that shares the same last stages of the analog buffer.



Fig. 3. Example of a cathode measurement with the first example

Figures 3 to 7 depict the measurement of two avalanche events for the circuit shown in Figure 1. The behavior of the avalanche can be accurately described, and the avalanche current can be assessed. The avalanche dynamic is in the order of a few hundred picoseconds. The cycle of the avalanche depicted in Figures 7 and 8 shows that the start of the avalanche cycle exhibits little dispersion, while the extinction of the avalanche can be very noisy.



Fig. 4. Two avalanches event of a complete diode voltage measurement with the first example



Fig. 5. Temporal zoom of two avalanche events of a complete diode voltage measurement with the first example.



Fig. 6. Reconstructed avalanche current of the two avalanche events depicted in fig 5.



Fig. 7. Cycle of the avalanche tracing the current as a function of the voltage of the SPAD.



Fig. 8. 250 superposed of the PSnode voltage measurement In the first example configuration (cf. Figure 1), afterpulsing, as well as the stochastic behavior of the quenching process, are particularly visible in the 250 measurements shown in Figure 8. The avalanche current does not turn off immediately after the SPAD reaches its breakdown voltage. Instead, it holds the SPAD to an equilibrium state that can last for up to a few nanoseconds.



Fig. 9. Measurement of the anode voltage of circuit depicted in fig 2 with active quenching for different avalanche sensing sensitivity circuit.

Figure 9 shows the measurement of the SPAD's anode voltage carried out with the second circuit (cf. Figure 2). The curves are obtained with circuits of increasing sensitivity from red, green to yellow. The purely passive quenching process is visible and equivalent for the three circuits from 1 to 1.5 ns. The most sensitive circuit detects the avalanche and starts a faster

transition to actively quench it.



Fig. 10. Oscilloscope screen shot of the anode voltage transition of circuit depicted in fig 2 when the oscilloscope is in the persistence mode. Three levels of excess bias can be observed.

The SPAD integrated in the second circuit is not optimized and uses only the layers of the standard CMOS process. Two levels of passive quenching, PQ1 and PQ2, are clearly identified with a breakdown voltage difference of about 200 mV on the measurement shown in Figure 10. This indicates that the electric field is not homogeneous along the junction leading to a local variation in the breakdown voltage, with preferentially two triggering locations associated with these two distinct levels observable experimentally. A third level of breakdown voltage is also observable below PQ2.

CONCLUSION

In this study, we successfully demonstrated a technique to observe the transient measurements of avalanche dynamics and quenching in SPADs. The temporal behavior of the SPAD can be accurately determined, and the first experimental results allow for the characterization of very interesting stochastic effects. This leads to a much better understanding of the SPAD operation.

ACKNOWLEDGMENT

The authors would like to thank the Nano2022 research program, the French national research agency ANR (ANR-18-CE24-0010) and CIME-P (Grenoble) for IC prototyping services. W. U. and F.C Authors thanks STMicroelectronics for providing access to the CMOS technology.

REFERENCES

- [1] Issartel, D., Gao, S., Pittet, P., Cellier, R., Golanski, D., Cathelin, A., & Calmon, F. (2022). Architecture optimization of SPAD integrated in 28 nm FD-SOI CMOS technology to reduce the DCR. Solid-State Electronics, 191, 108297.
- [2] T. Klauner, I. S. Alirezaei, N. Roisin, N. André and D. Flandre, "SPICE Model of SPAD Transient Intrinsic Response Validated using Mixed-Mode TCAD Simulations," ESSDERC 2023 - IEEE 53rd European Solid-State Device Research Conference (ESSDERC), Lisbon, Portugal, 2023, pp. 136-139.
- [3] A. Dervić, B. Goll, B. Steindl and H. Zimmermann, "Transient measurements and mixed quenching, active resetting circuit for SPAD in 0.35 μm high-voltage CMOS for achieving 218 Mcps," 2019 26th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Genoa, Italy, 2019, pp. 819-822,