A PVT-Insensitive Body-Biased Time-to-Digital Converter in 28nm FD-SOI CMOS Technology

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***Abstract*—This paper presents a novel body-biased time-to-digital converter (TDC) pixel integrated with a delay locked loop (DLL) in 28nm FD-SOI CMOS technology, specifically designed to enhance the robustness against process, voltage and temperature variations in single photon avalanche diode (SPAD) based short-range time-of-flight systems. The 16-bin TDC resolution is adjustable between 54.6, 110.1, and 140.5ps. Experimental results validate the DLL delay chain's robustness in maintaining locking against 10% voltage and frequency variations. It is confirmed that the TDC bin width remains consistent despite the changes in voltage. Additionally, related electrical characterization results are presented.**

I. Introduction

RECENTLY, there have been promising developments in single photon avalanche diode (SPAD) based direct time-of-flight (dToF) sensors, attributed to its high sensitivity, fast response time and compatibility with complementary metal-oxide-semiconductor (CMOS) technologies. Within these sensors, time-to-digital converters (TDCs) play a vital role, timestamping individual photons with picosecond resolution, which can be subsequently processed to depth information. Applications in biomedical imaging, such as time-domain near-infrared spectroscopy [1], demand high reliability over a fine temporal range. However, achieving consistent fine resolution becomes challenging due to process, voltage and temperature (PVT) variations. Therefore, a PVT-insensitive high-resolution TDC is essential.

Fully depleted silicon on an insulator (FD-SOI) CMOS technology, featuring an ultra-thin channel and an insulation layer of buried oxide (BOX), presents several advantages. These include enhanced design flexibility with a body terminal beneath the BOX, low leakage current due to the small parasitic source-drain capacitance and intrinsic stackability. Recent works [2][3] have successfully fabricated SPAD pixels in 28nm FD-SOI, placing the diode between the P-well and deep N-well below the BOX, with the associated front-end electronics integrated above BOX. Subsequently, [4] has proposed an ultra-fast active quenching circuit in the same process node. These advancements in SPAD development motivate further integration with a TDC circuit on the same die.

This paper presents the first histogramming TDC pixel for a SPAD-based dToF system fabricated in the 28nm FD-SOI CMOS technology. We propose a novel body-biased tuning delay line TDC based on a delay-locked loop (DLL) to ensure robust performance across various PVT conditions, exploiting the fourth terminal offered by the technology. The remainder of the paper is organized as follows: Section II illustrates the chip structure, the body-biased tuning technique in FD-SOI and the DLL-based TDC pixel architecture. Section III presents the experimental results, verifying that the TDC delay chain is locked with the DLL. Finally, Section IV concludes.

II. Chip Architecture

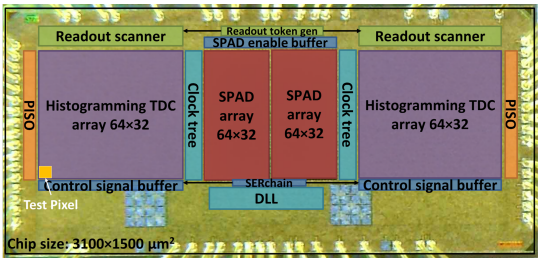


Figure 1: Chip floorplan with highlighted main functional blocks.

Figure 1 shows the floorplan of the chip. It is composed of a 64×64 SPAD array with front-end circuits, 1:1 histogramming TDC arrays, a DLL circuit, ***STOP*** reference clock trees shared for a row of 32 pixels, a serial interface and readout circuitry. This paper focuses on the TDC pixel and the DLL module, whose structure is shown in Figure 2. Each pixel contains a 64-element delay-line TDC, 11-bit x 16-bin histogram counter, and STOP control circuits. The DLL synchronises itself with around 100M/66.66MHz ***STOP***, generating two control voltages to lock TDC bin sizes.

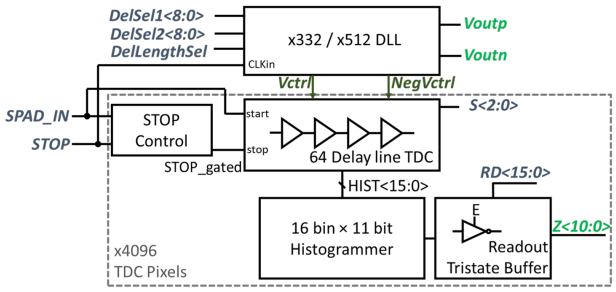


Figure 2: Overview of a DLL-based TDC pixel array.

A. TDC Pixel Architecture

The detailed schematic of the implemented delay line TDC is shown in Figure 3. The body-tuning technique is deployed in all delay units, which are implemented with four regular-Vt (RVT) transistors and consist of an inverter coupled with a transmission gate. By symmetrically applying a positive voltage ***Vctrl*** to the RVT-PMOS body and a negative voltage ***NegVctrl*** to the RVT-NMOS body, fine modulation of the delay time is achieved. Compared to common gate-biasing delay elements implemented by capacitive shunting or current-starving inverters, this scheme eliminates the need for extra transistors and achieves lower power consumption due to reduced leakage current [5].

The 64-element delay chain is composed of 128 pairs of the proposed body-biased delay units. ***SPAD_IN*** serves as the input to the chain, with its falling edge indicating the detection of a photon event. To generate rising-edge triggered delayed

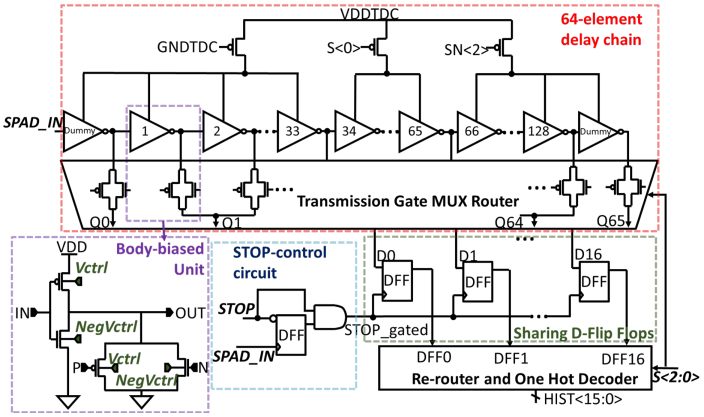


Figure 3: Schematic of the histogramming TDC pixel.

pulses, the first transmission gate in each pair is deactivated. All the second gates form a MUX router, mapping 66 delayed outputs to 17 inputs of shared D-Flip Flops (DFFs). Different combinations of delayed outputs ***Q<*>*** can be selectively activated based on a TDC range configured, of which there are three in total. Then, selected delays are sampled by a ***SPAD_IN*** gated version of ***STOP***. This gating design ensures that clock cycles are passed only when a photon is detected, thus avoiding continuous triggering of the DFFs. Finally, a re-router and one-hot decoder are applied to timestamp each rising edge in the corresponding histogram bin.

B. DLL Architecture and Operating Principle

The DLL circuit includes a digital phase detector, a level shifter, a charge pump, an inverted body-biased voltage generator and a 512-element delay chain as shown in Figure 4. Delay elements implemented here are identical to those in the TDC delay chain. ***Vctrl*** and ***NegVctrl*** are generated within the DLL by aligning the feedback clock with ***STOP*** clock to simultaneously tune the delay time of each delay element in both DLL and all TDC pixels against PVT variations. Two control voltages can be supplied externally in an open-loop if ***ExtVctrl*** is activated. A similar programmable MUX Router is applied here so that ***DelSel1*** and ***DelSel2*** can respectively select a rising edge ***Voutn*** and a falling edge ***Voutp*** from the DLL delay chain for testability.

In the closed-loop configuration, the phase difference between the input clock signal and the clock feedback from the delay chain, selectable between the 332nd or 512th edge for 10ns/15ns ranges, generates ***Up*** and ***Down*** signals. These signals are level shifted from 1V to 1.8V domain to cover a wider control voltage range, before telling the analogue charge pump to pump up or pull down ***Vctrl***.

Compared to the typical gate-driven DLL, one extra module is implemented to mirror ***Vctrl*** to ***NegVctrl*** referring to the forward back-bias generator proposed in [6]. As shown in Figure 5(a), the negative voltage generator comprises one amplifier and two replica body-biased inverters as those used in the delay chain. One inverter ***Inv1*** has both body terminals biased to ground, generating a self-locked stable midpoint. The other inverter ***Inv2*** is body-tuned by ***NegVctrl*** and ***Vctrl***. Once ***PowerDown*** is triggered, ***Vctrl*** is charged up from ground, ensuring the delay chain is adjusted from the fasted speed to avoid false locking. ***Amp*** then forces the midpoint of ***Inv2*** to

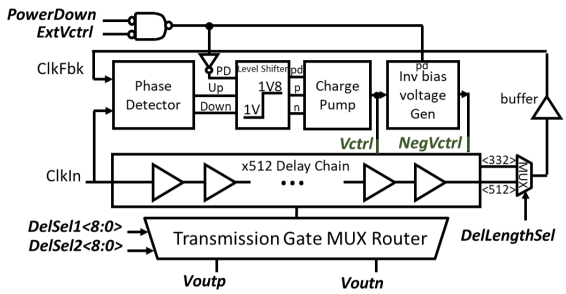


Figure 4: Architecture of the DLL circuit.

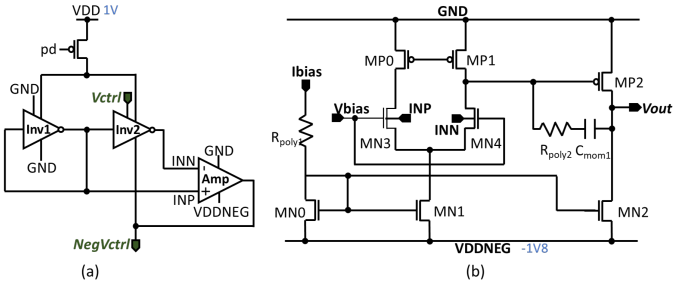


Figure 5: (a) Block diagram of the negative body-biased generation module; (b) Schematic of the body-driven RC Miller amplifier [6].

approach that of ***Inv1***, thus modulating ***NegVctrl*** according to ***Vctrl***. Note that in Figure 5(b) the power grid of ***Amp*** operates from 0 to -1.8V, while ***INP*** and ***INN*** are around 0.5V, so the input low-Vt (LVT) NMOS pair is designed as positive body-driven which ensures voltage compatibility between ***Inv2*** and ***Amp***, eliminating a level shifter.

III. Experimental Results

Electrical characterisation of the DLL and TDC is presented in this section. ***Voutp*** is always configured to the first falling edge as a reference and ***Voutn*** is swept among rising edges to be tested in DLL. Unless stated otherwise, for all measurements herein the DLL was locked to a 100MHz clock and the delay range is selected as 10ns.

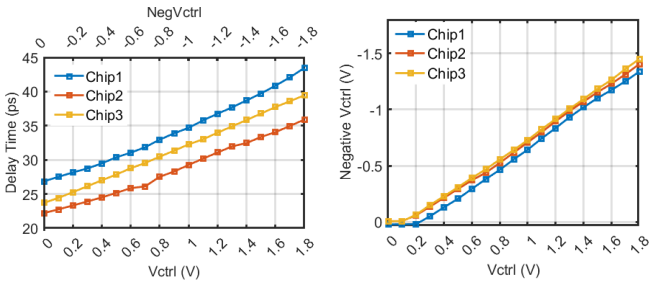
A. DLL Characterisation

The tunability of a single delay element is characterised by simultaneously sweeping Vctrl from 0 to 1.8V and NegVctrl from 0 to -1.8V in an open-loop test. Figure 6(a) demonstrates a linear correlation between the propagation delay time of a single element and the body-biased voltage, with a maximum range of 15.5ps. It proves that the body-biasing technique provides a wide room for PVT variations.

To test the negative control voltage generation module, a DC sweep is conducted with ***Vctrl*** externally driven, while all other modules are turned off. Figure 6(b) shows that the negative control voltage linearly follows the positive control voltage with an average offset of 0.13V.

B. DLL Locking Verification

Verifying the phase alignment between ***ClkIn*** and ***ClkFbk*** is not feasible due to absence of a direct testing method for both signals. Hence, the experiment measures the variation in delay offset between the 1st and the 333rd rising edges under varying voltage supply and input clock frequency conditions. This offset, primarily due to delays in the range selection MUX



(a) Delay time against control voltages (b) NegVctrl against Vctrl

Figure 6: Characterisation of (a) body-biased delay elements; (b) negative control voltage generation module.

and the buffer preceding the phase detector, should be invariant to prove the DLL's locked state. Figure 7 illustrates the offset varies heavily in open-loop test with external voltages, while in closed-loop delay offset variation considerably decreases 14 times, thanks to the self-tuned control voltage. Figure 8 shows that the delay offset does not vary with STOP. The variation is 16.5 times smaller than the 2ns period change, further demonstrating the loop is locked.

C. TDC Locking Test with the DLL

A test pixel is measured with ***SPAD_IN*** externally driven to check if the TDC is locked with the DLL. The delay of input pulses can be controlled in a step of 15ps to build up two histogram peaks in a certain distance. Figure 9 shows the estimated bin sizes within three ranges obtained from the centroid of mass (CoM), demonstrating that the TDC is well-locked with the closed-loop DLL and insensitive to 10% voltage variation.

D. TDC Linearity

Figure 10 shows the average non-linearity of three TDC ranges extracted from histograms measured by exposing the left 32×64 SPAD array to a stabilized broadband light source for 10s. The worst DNL among these ranges is +0.31/-0.11LSB and the worst INL is +0.22/-0.26LSB over all 2048 TDCs.

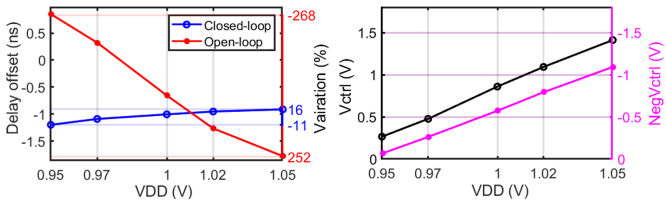


Figure 7: Delay offset variation against changing VDD in ±0.9V biased open and closed-loop test (left); Control voltages change measured in the closed-loop test (right).

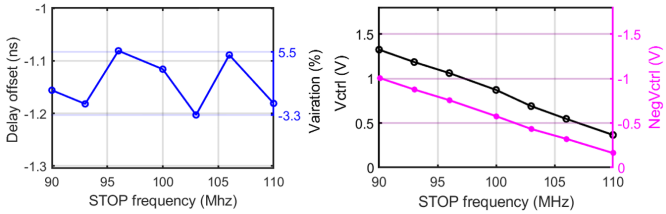
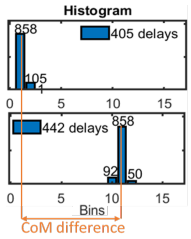


Figure 8: Delay offset variation against changing clock frequency in closed-loop test (left); Control voltages change measured (right).



	TDC Range	VDD		
		0.97V	1V	1.03V
Closed-loop estimated bin size* (ps)	Short	52.46	54.61	51.418
	Middle	110.02	110.13	110.15
	Long	140.68	140.58	140.51
Open-loop estimated bin size* (ps)	Short	55.20	47.47	41.15
	Middle	110.57	105.90	99.20
	Long	147.99	140.37	127.57

*Estimated bin size = CoM difference/# of delays

Figure 9: Illustration of a CoM measurement example (left); Bin size measurement in open/closed loop (right).

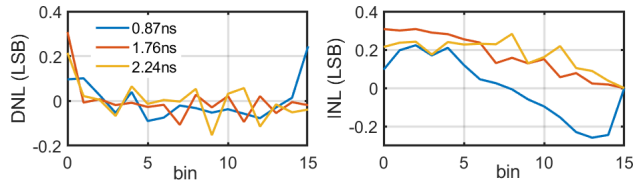


Figure 10: Average non-linearity measured from code density test in three TDC ranges for 2048 TDCs.

IV. Conclusion

The paper demonstrates a body-biased TDC in 28nm FD-SOI CMOS technology, successfully addressing PVT variations with a custom-designed DLL. Within this loop, a negative voltage generator has been innovatively introduced to generate two control voltages. Experimental results confirm that correctly generated voltages facilitate the locking of the TDC delay chain with the DLL. This ensures stability against voltage and frequency variations, highlighting the TDC's robustness in short-range applications.

TABLE I: Characterisation Summary

Techno.	28nm FDSOI		
Histogram Bins	16		
TDC resolution (ps)	54.6	110.1	140.5
TDC range (ns)	0.87	1.76	2.24
TDC DNL (LSB)	+0.24/-0.09	0.21/-0.15	+0.31/-0.11
TDC INL (LSB)	+0.22/-0.26	+0.28/0	+0.31/0

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