Cascaded Vernier Time-to-Digital Converter : Toward Integration in an Array

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***Abstract*—Time-to-digital converters (TDC) play a crucial role in applications such as particle physics and medical imaging, facilitating precise measurement of the time of arrival of photons. Among TDC architectures, the Vernier TDC stands out for its power efficiency and compact design. This paper presents a cascaded-stage Vernier TDC architecture, featuring a feedthrough reference circuit. This design enables successive Vernier measurements, leading to a reduced number of cycles for the same dynamic-range-to-resolution ratio, decreasing conversion time and jitter. To validate this architecture, a test chip was fabricated in 180 nm, comprising four versions of cascaded Vernier TDCs. Experimental results showcase improvement in precision, linearity, total cycle counts and average dead time. Furthermore, the paper discusses the implementation of the proposed architecture in 65 nm. Simulations suggest promising outcomes, including low power consumption, short conversion times and compact design.**

***Index Terms*—ASIC, CMOS, multi-Vernier architecture, photon-to-digital converter (PDC), radiation instrumentation, time-to-digital converter (TDC)**

I. Introduction

The time of arrival (ToA) of a photon is a critical measurement in many systems based on silicon photomultipliers (SiPM). It is used in quantum key distribution to secure data transmission [1] or in time-of-flight computed tomography to improve scanner performance [2]. Timestamping of ToA is performed by a time-to-digital converter (TDC) associated with SiPMs capable of detecting single photons. While in many systems a TDC is integrated with an array of photodiodes, in digital SiPMs, TDCs are associated with one or a few single photon avalanche diodes (SPADs). The key considerations for implementing the converter in a array are small area and power efficiency. The ring oscillator (RO) based Vernier TDC is a promising architecture in regards to those criteria, yet it is not ideal for fine resolution due to the increasing cycle count and associated cycle-to-cycle jitter [3]. We propose a RO-based cascaded Vernier TDC that reduces the total cycle counts required to achieve the same resolution, thus maintaining the conversion time and jitter low [4]. This architecture is build upon a reference oscillator that is fed through all Vernier stages, thereby reducing the space required by the additional Vernier stages.

II. Architecture

A RO Vernier TDC typically estimates a time interval by activating two oscillators: a reference oscillator, whose number of cycles is counted to the end of the interval and gives off a coarse measurement of the interval, and a fine oscillator, whose cycle count, needed to catch up with the reference, provides a finer measurement of the residual time. The resolution is determined by the period difference of the two oscillators (*reference* and *fine*) of the Vernier stage. The smaller the difference between the periods of the two oscillators, the finer the resolution of the TDC. However, with a finer resolution or with the extension of the dynamic range, the number of cycles of the oscillators increases considerably, thus generating jitter (i.e. imprecision in the measurement).

To reduce the number of cycles, the proposed solution is to add multiple Vernier stages to consecutively divide the time interval at each stage [5], [6], thus distributing the cycles

across each stage. As such, the first Vernier stage, with a coarser resolution, undergoes fewer cycles; its time residual is then measured by the second Vernier stage. Hence, the second stage LSB is finer without increasing the number of oscillator cycles, and the dynamic range to resolution ratio (DRRR) remains constant between stages. As a general rule for this consecutive Vernier architecture, the dynamic range of each subsequent stage is determined by the resolution of the preceding stage. Decreasing the total number of oscillator cycles mitigates the impact of cycle-to-cycle jitter on the precision while reducing the TDCs dead time.

Finally, the proposed cascaded Vernier architecture shares the reference oscillator signal of the first stage with all the Vernier stages, instead of triggering a separate reference oscillator for each Vernier stage. This reference feedthrough leads to minimal area expansion since each addition of a Vernier stage requires only one oscillator instead of two. The block diagrams for a single Vernier TDC and a double Vernier TDC are illustrated in Figure 1 and Figure 2, respectively.

III. Proof of concept in 180 nm

An ASIC was fabricated in 180 nm technology (Figure 3). It implements four types of Vernier TDCs from a 1–Vernier TDC (2 oscillators) to a 4-Vernier TDC (5 oscillators). Two copies of each TDC were implemented to perform correlated tests, removing the impact of common-mode noise. To stabilize the RO frequency, the current flowing in the delay element of the RO is controlled by shared integrated phase-lock loops (PLL) or an external digital-to-analog converters (DAC). The TDCs were characterized using the code density method, sending uncorrelated start and stop signals, ensuring a uniform code distribution.

Figure 4 shows that the optimal precision for the 2–Vernier architecture is significantly lower than that of the 1–Vernier for the same dynamic range. The difference between the 2- and 3- Vernier architectures is less pronounced.

Table I outlines the characteristics of each architecture with a common dynamic range of 20 ns and an LSB of 50 ps. Figure 5 shows a noticeable decrease in dead time with a three-fold reduction of the conversion time from 1–Vernier to 2–Vernier. The standard deviation drop is due to a conversion time shift from a uniform distribution to a much finer normal distribution. Figure 6 shows the significant improvement in the non-linearity from 1–Vernier to 2–Vernier.

These results expose a significant improvement in both mean and standard dead time while also improving precision and linearity between the single and double Vernier.

IV. Implementation of the architecture in an array in TSMC 65 nm (upcoming results)

Considering the results of the 180 nm ASIC, only the 2–Vernier architecture has been implemented in a new ASIC built in TSMC 65 nm. The new TDC occupies an area of 35×43 μm^2.

The TDC is implemented in an array of 4×4 individually quenched SPADs. A ratio of one TDC to four quench circuits (QCs) was chosen to optimize the available area for digital processing considered for a large detector.

For characterization purposes, a set of two TDCs that share the same start were implemented to get correlated results. Figure 7 shows how the TDC pair is implemented in the array. Furthermore, all ROs in each TDC are individually controlled.

As of December 2023, the ASIC is still in fabrication and simulations show a power consumption of 112 μW for an event rate of 1 MHz with an LSB of 10 picoseconds and a dynamic range of 4 ns. Moreover, the mean conversion time (from the event onset to the end of conversion), with this DRRR, is 9 ns while the maximum value is 16 ns.

V. Conclusion

The results of the 180 nm ASIC have demonstrated the performance enhancement of the cascaded Vernier TDC architecture. In these TDCs, the signal from the reference oscillator is propagated to all the subsequent stages, removing an extra RO. Since the main performance enhancement arises from the addition of a second stage, only this architecture was implemented in an array in TSMC 65 nm. We will present these results, in depth undergoing characterization and comment further on the use of such TDCs in a large SPAD based photon counting detector.

References

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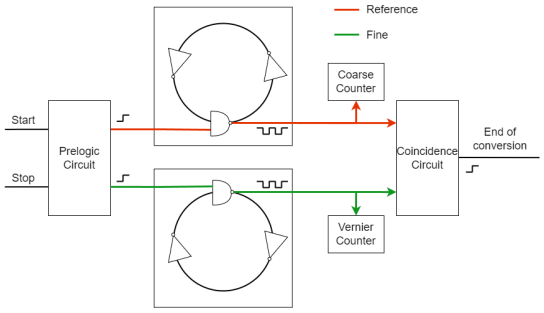


Fig. 1: 1–Vernier architecture diagram.

TABLE I: RESULTS OF TDCS FROM ASIC MANUFACTURED IN TSMC 180 NM TECHNOLOGY. POWER VALUES ARE EXTRACTED FROM SIMULATIONS, WHILE THE OTHER RESULTS ARE BASED ON LABORATORY MEASUREMENTS.

	LSB	DNL (std)	INL (max)	Deadtime (mean)	Deadtime (std)	Precision	Max count	Area	Power @ 1 Mhz
1-Vernier	50 ps	0.05 LSB rms	0.51 LSB	264.2 ns	139.4 ns	26.8 ps rms	110	0.070 mm²	1.9 mW
2–Vernier	50 ps	0.04 LSB rms	0.15 LSB	77.5 ns	19.3 ns	16.6 ps rms	25	0.089 mm²	2.2 mW
3-Vernier	50 ps	0.03 LSB rms	0.13 LSB	74.2 ns	11.9 ns	24.0 ps rms	18	0.100 mm²	2.9 mW

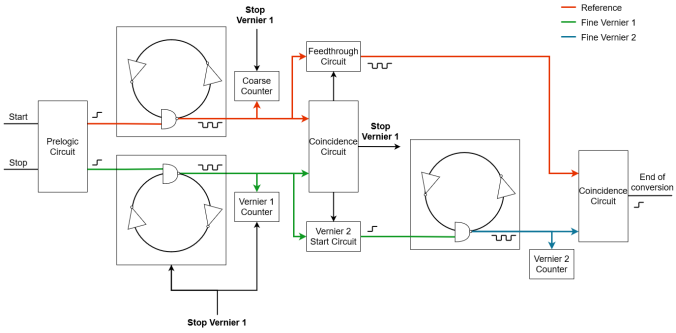


Fig. 2: Cascaded 2–Vernier architecture diagram.

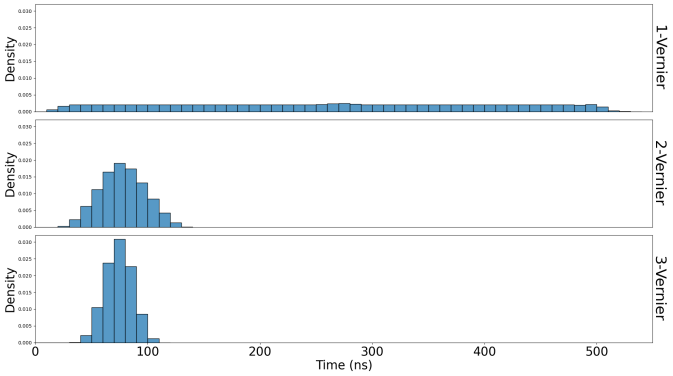
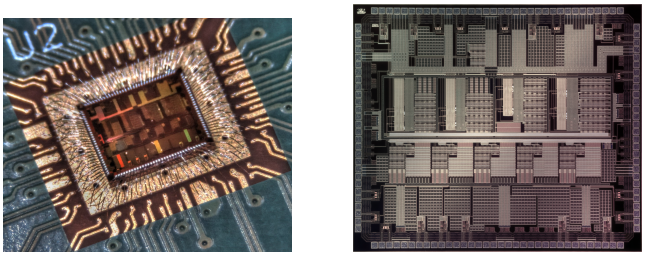


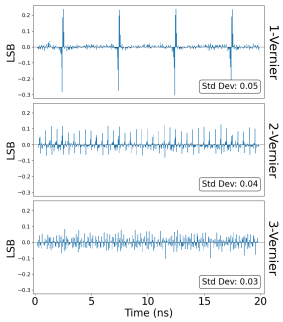
Fig. 5: Conversion Time of TDCs in TSMC 180 nm.



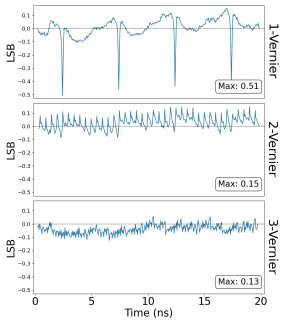
(a) ASIC wirebonded

(b) View from the top (x10)

Fig. 3: Picture and micrograph of the ASIC made in 180 nm.



(a) Differential Non-Linearity



(b) Integral Non-Linearity

Fig. 6: Non-Linearity across the dynamic range for TDCs in TSMC 180 nm.

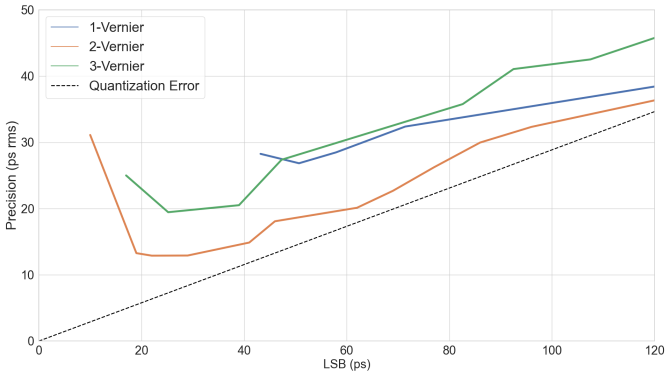


Fig. 4: Precision function of LSB for TDCs in TSMC 180 nm.

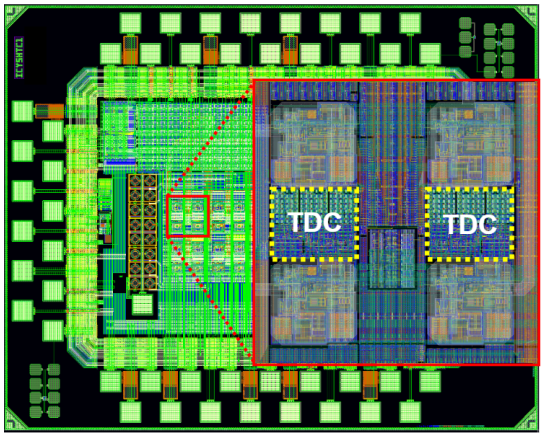


Fig. 7: Layout of the chip in 65 nm technology. Inset show the integration of two TDCs in a 2x2 quench array.