

Introduction

[Wafer Probing] [Pad-SPAD-Pad Package]

Disadvantages

1. Too long Measurement time
2. Requirement of Manual adjustments

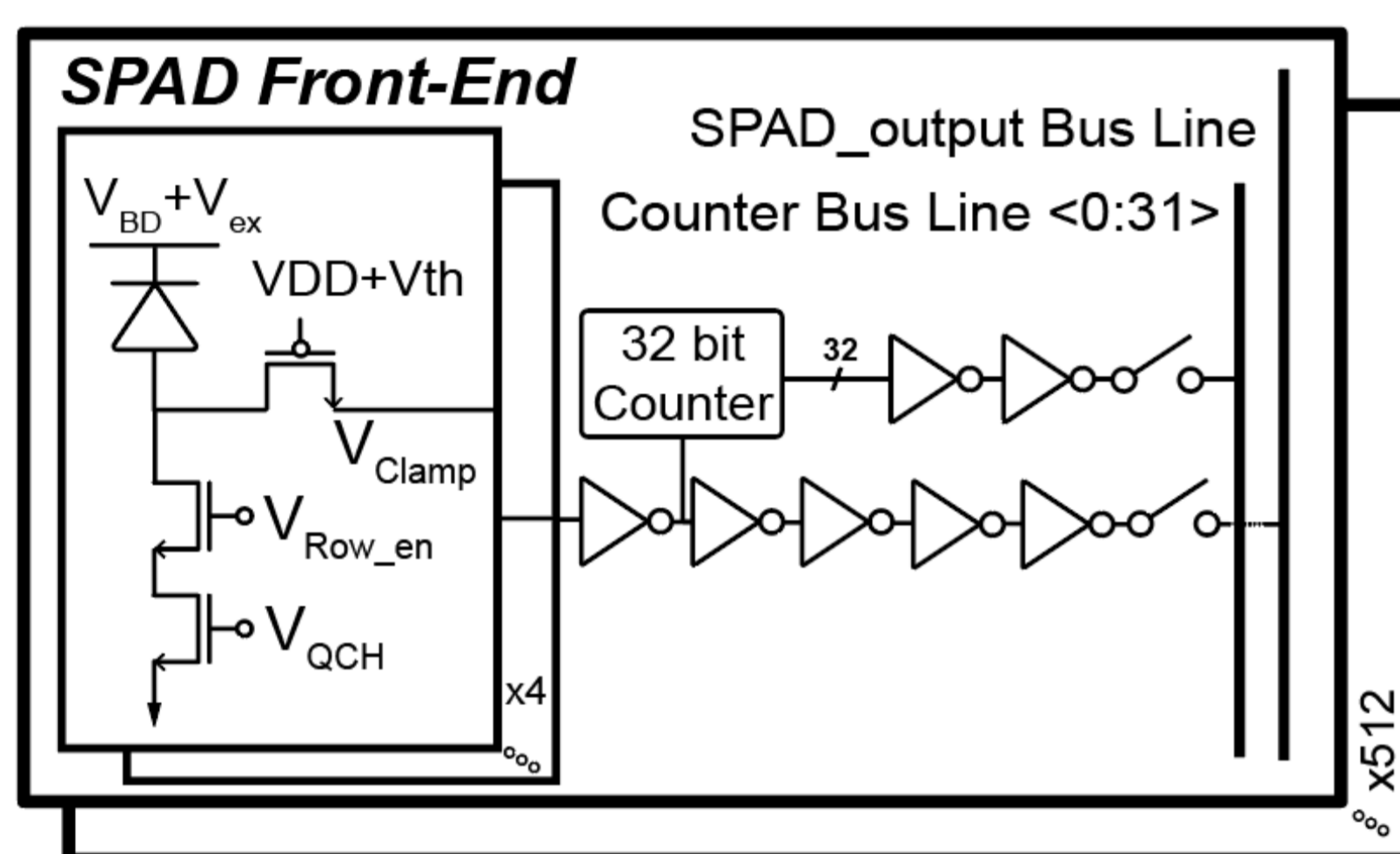
Outline of Test Bench

P-well/Deep N-well SPAD
Passive quenching + Counter
Data Storage
Data acquisition & Vex control

- SPAD Farm Measurement: Each different 2048 number of SPADs
- Significant time-effective measurement
- Automatic adjustment of excess voltage

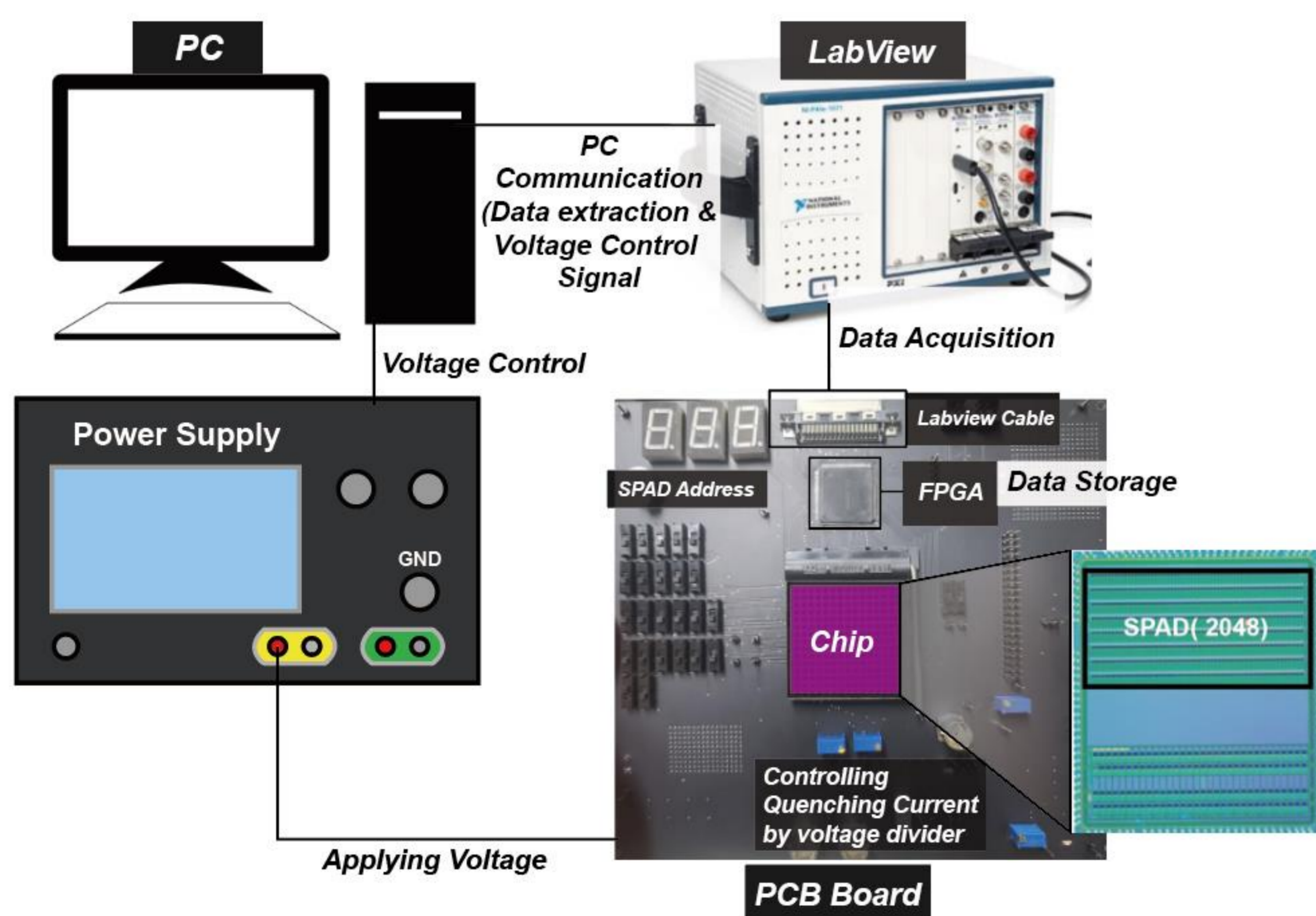
Main Idea

Chip Architecture



- V_{clamp} : Preventing the circuits from damage by high peak current.
- V_{QCH}
 - ❖ Passive quenching by current mirror
 - ❖ Lowering resistance for a maximum count rate

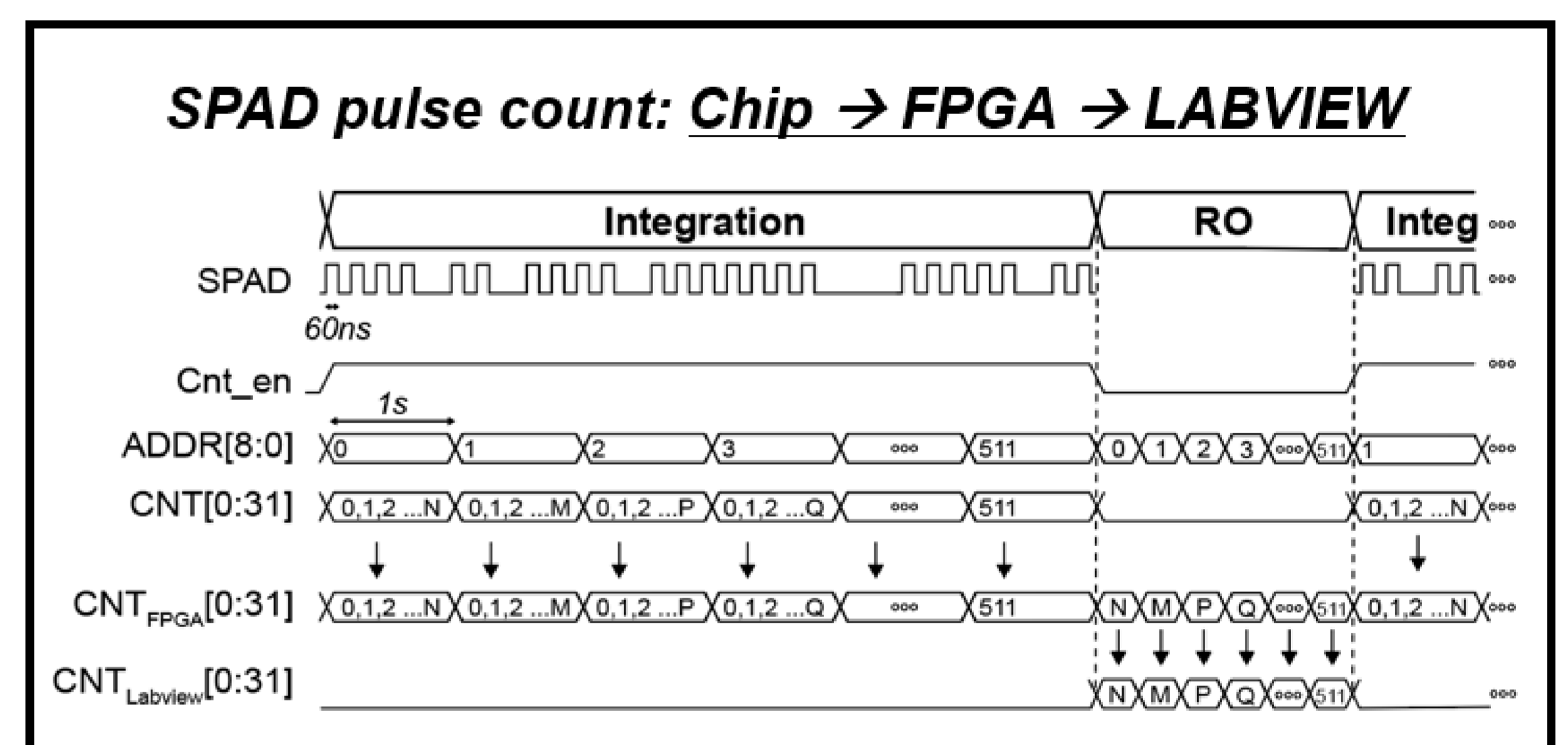
Measurement Set-up



- FPGA: Control the SPADs and associated circuits while storing the SPAD pulse count in a counter.
- LabView: Data extraction, excess voltage control

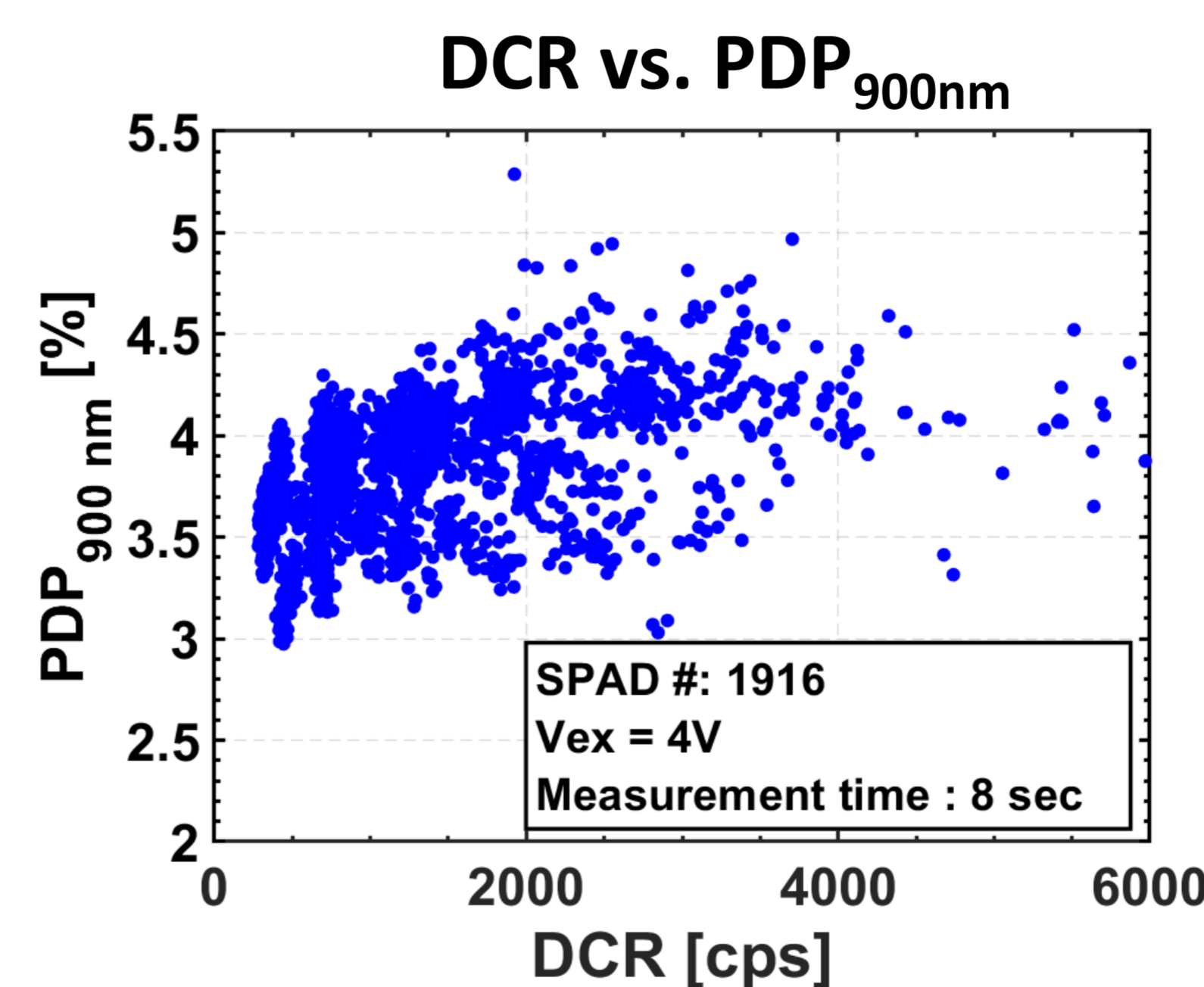
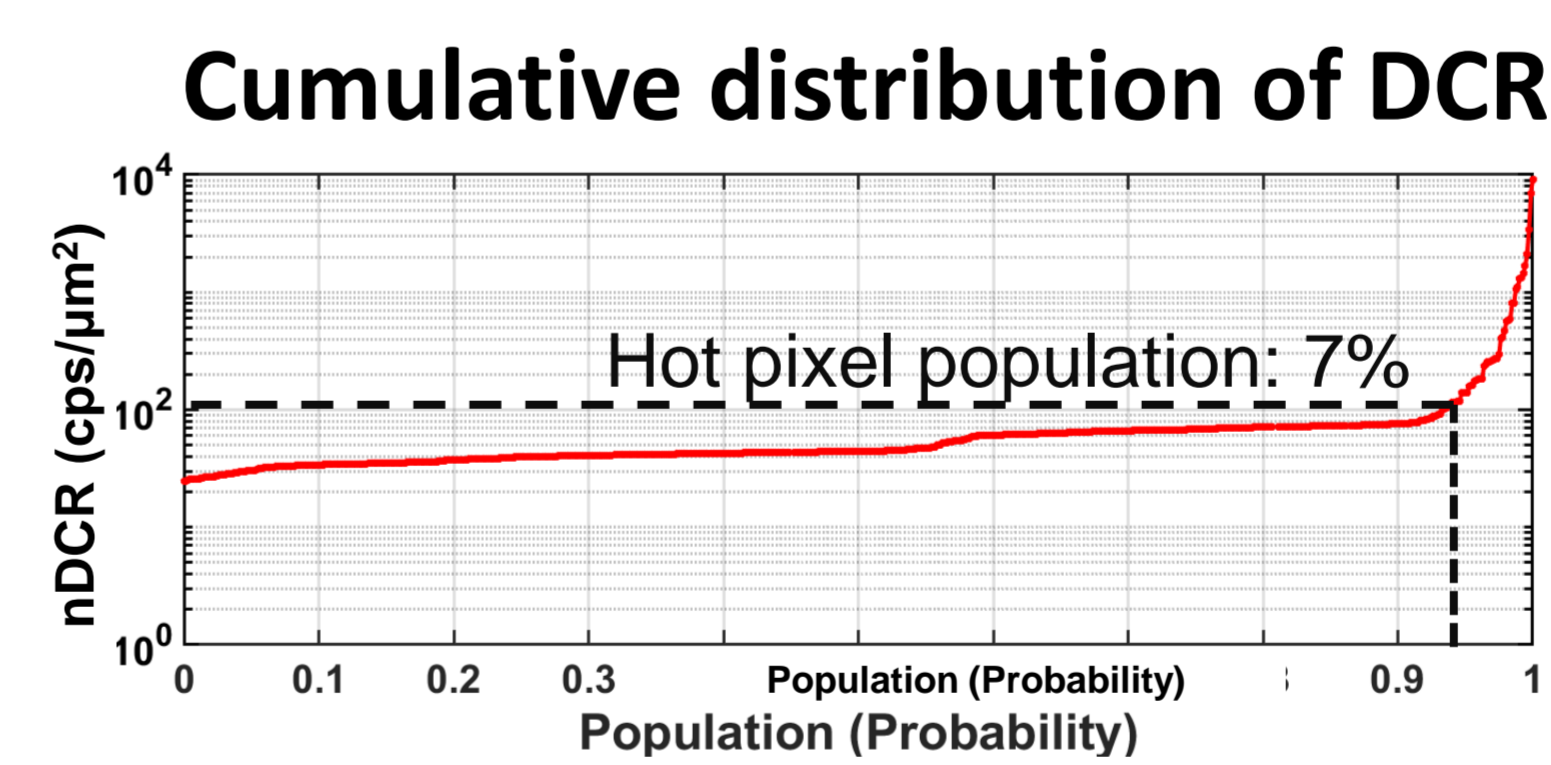
Measurement Process & Results

Timing Diagram



- FPGA : Making addressing signal, count enable signal and readout signal (strobe).
- LabView: Acquisition of counter value to PC using csv file

Measurement Results



Device Under Test			
N-well width	0.7	0.85	1
GR width	1	1.5	2
AA Radius	2.5	3.75	5
P+ Radius	AA	AA -0.5	AA-1
AA shape	R.S	circle	Square
P-well/ deep N-well (VG)			

- Analysis Procedure
 1. Cumulative distribution plot
 - Sorting the hot pixel population
 2. DCR vs. PDP measurement plot w/o hot pixels
 - Upper-left side points: high performances
- Reduction processing time compared to a SPAD w/o integrated circuitry

Conclusion

1. The time-effective characterizations of numerous SPADs in a very short time
2. Reducing the likelihood of inaccurate measurements due to SPADs' damage and temperature fluctuations