

Extended Dynamic Range SPAD Front-End Using Near-Threshold Inverter-Based Comparator

Maciej Wojtkiewicz¹, Bruce Rae², Robert K Henderson¹

¹The University of Edinburgh

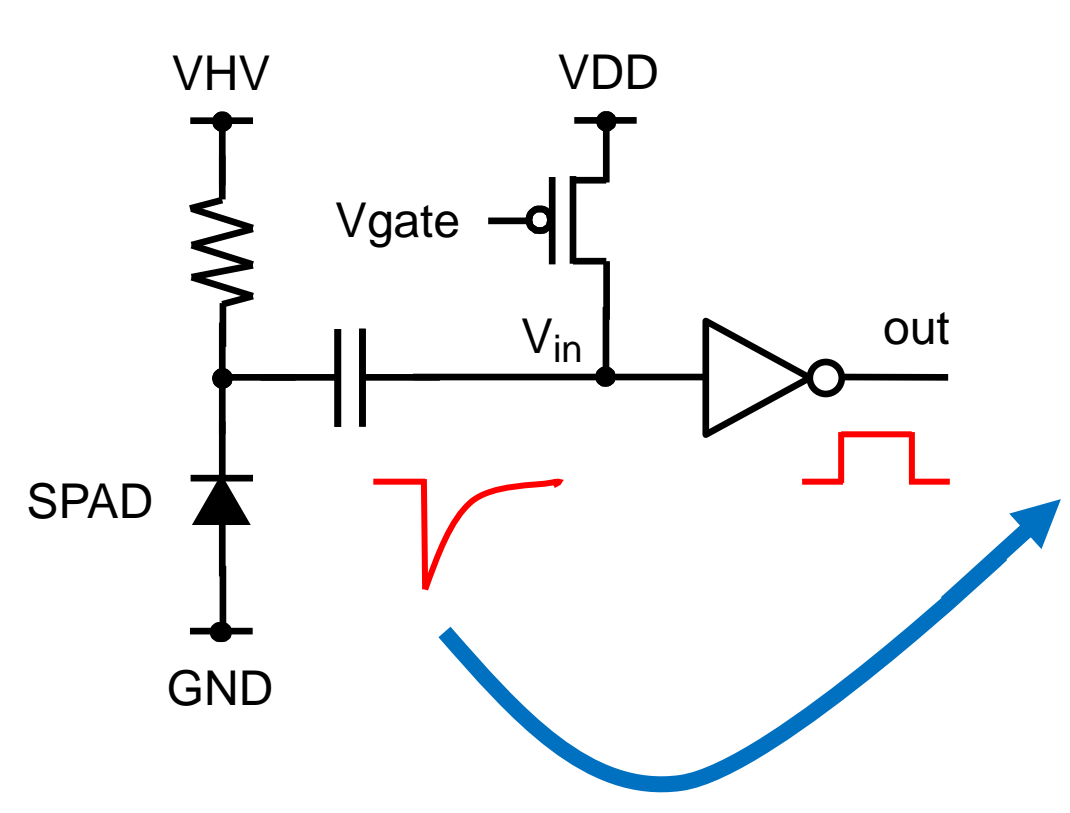
²STMicroelectronics, Imaging Division, Edinburgh

Motivation: Outdoor LIDAR

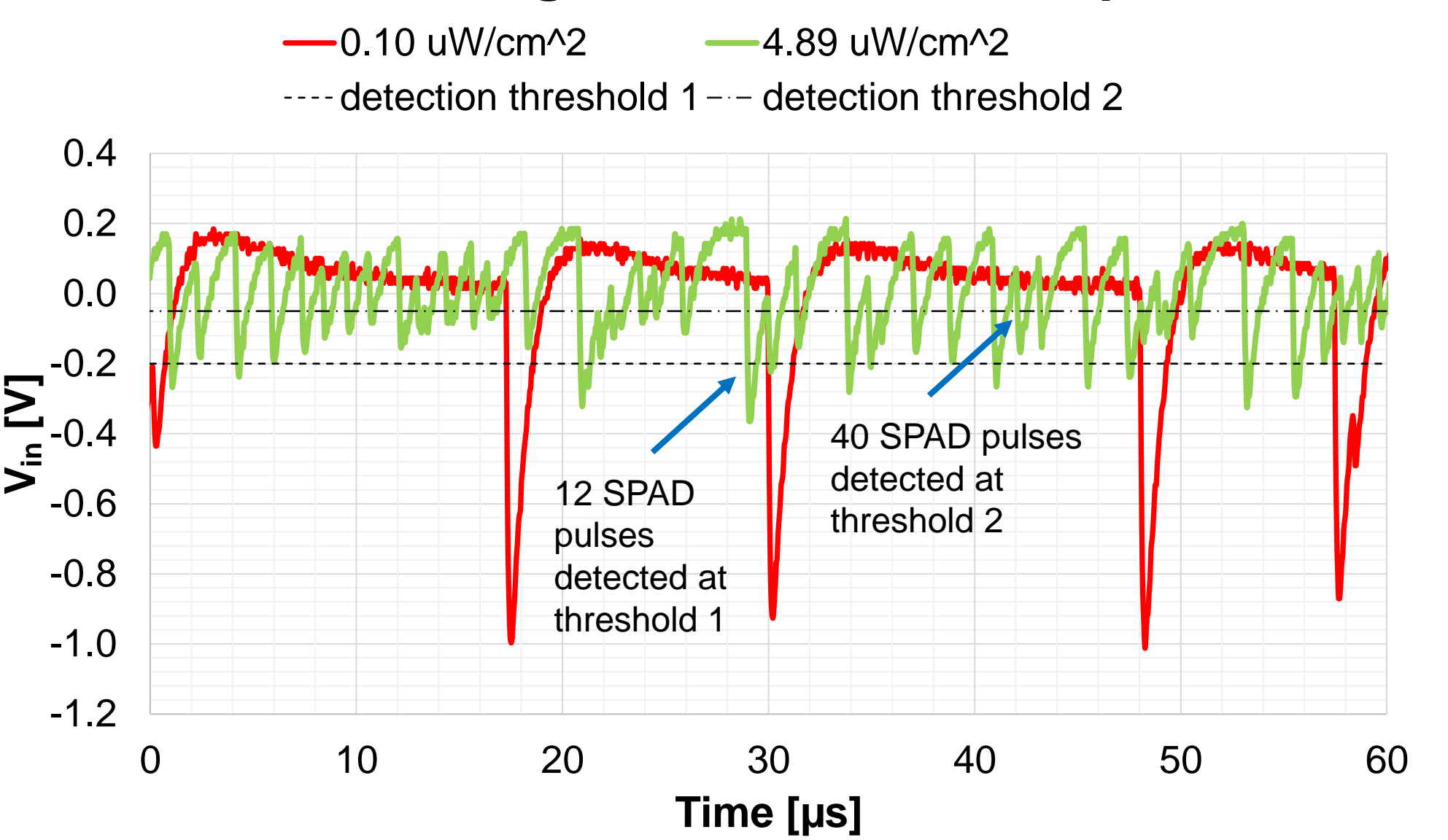
- SPAD-based pixels can time single photons with picosecond precision, which is appealing for time-of-flight systems [1], [2].
- In automotive LIDAR tolerance of high solar background is critical.
- At high illumination levels SPAD pixels easily saturate, especially when the diode is used in the RC-coupled arrangement.
- Near device paralysis there is still an output from the SPAD, but the pulse amplitude is too small to trigger the inverter.
- Comparators have been proposed to pick up low swing SPAD events to improve jitter [3], however here we recognise that they are also able to extend dynamic range by detecting smaller amplitude pulses occurring near saturation. However, normally they are area and power-hungry blocks difficult to integrate in pixel arrays.

Problem: SPAD Paralysis

Generic RC-Coupled SPAD Front-End

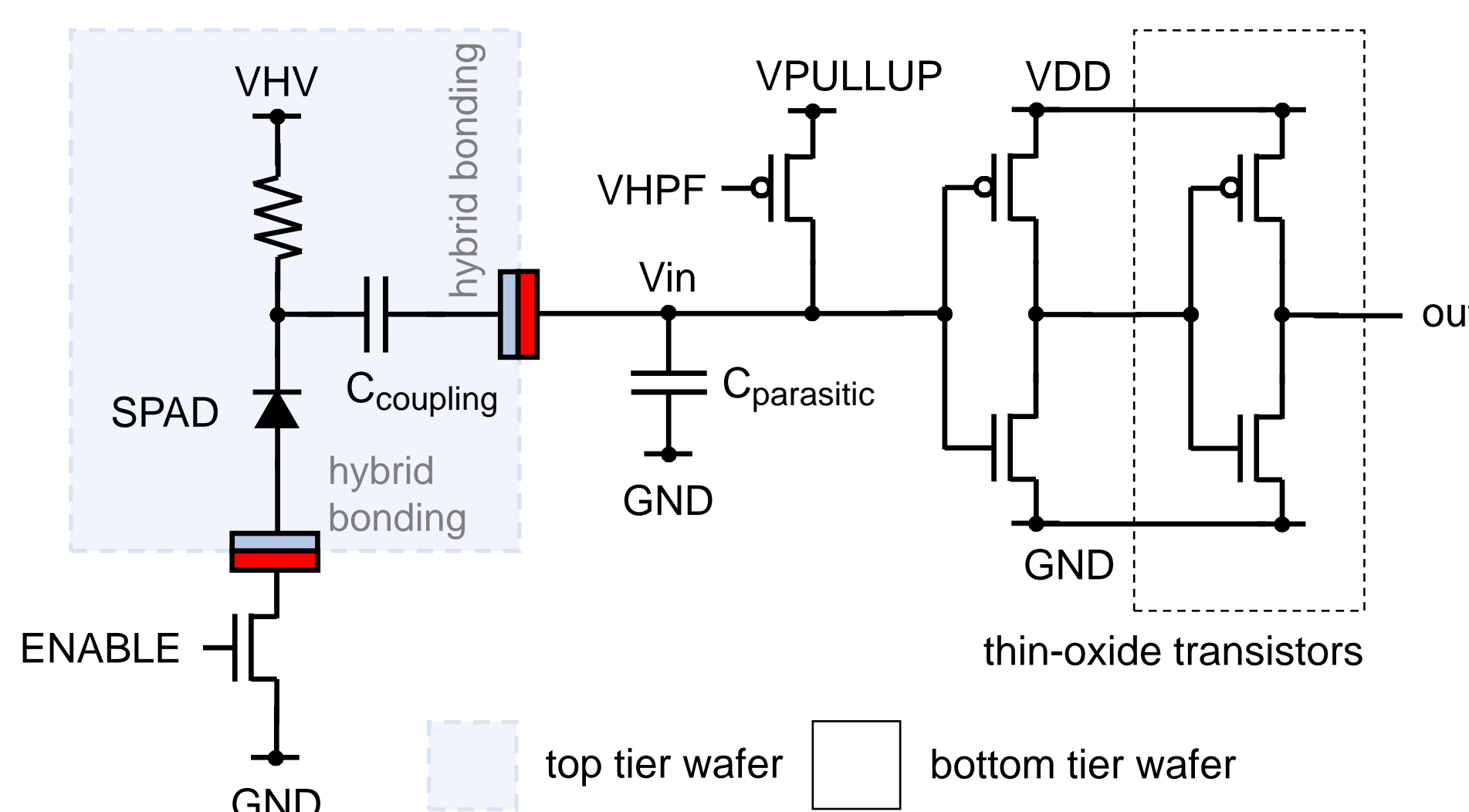


Transient Signal at the Inverter Input

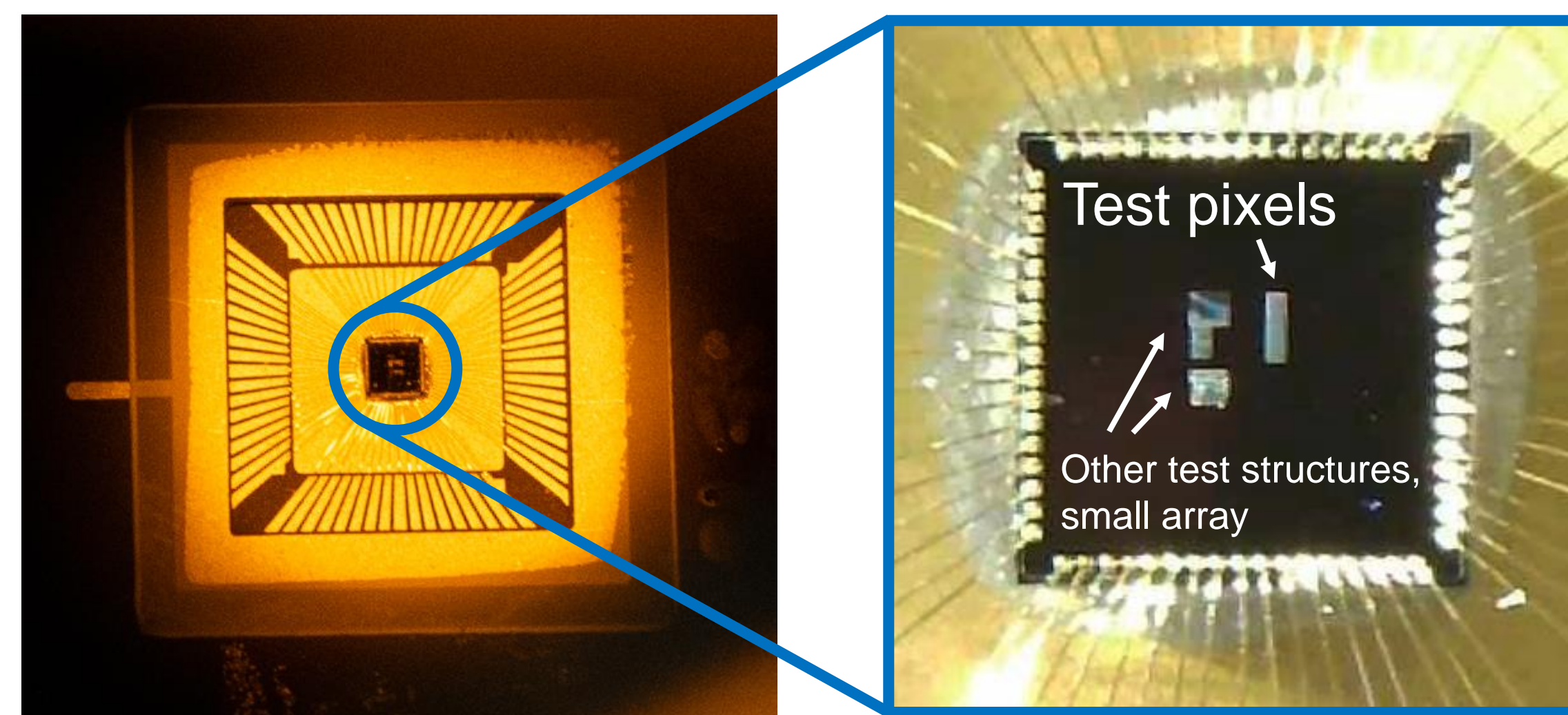


Solution: HDR SPAD Front-End

- Instead of biasing the inverter input to VDD, VPULLUP is chosen at different levels to tune the sensitivity of the input inverter to the small voltage excursions, optimize the DC current, and prevent any noise at Vin to trigger 'false' photon counts.

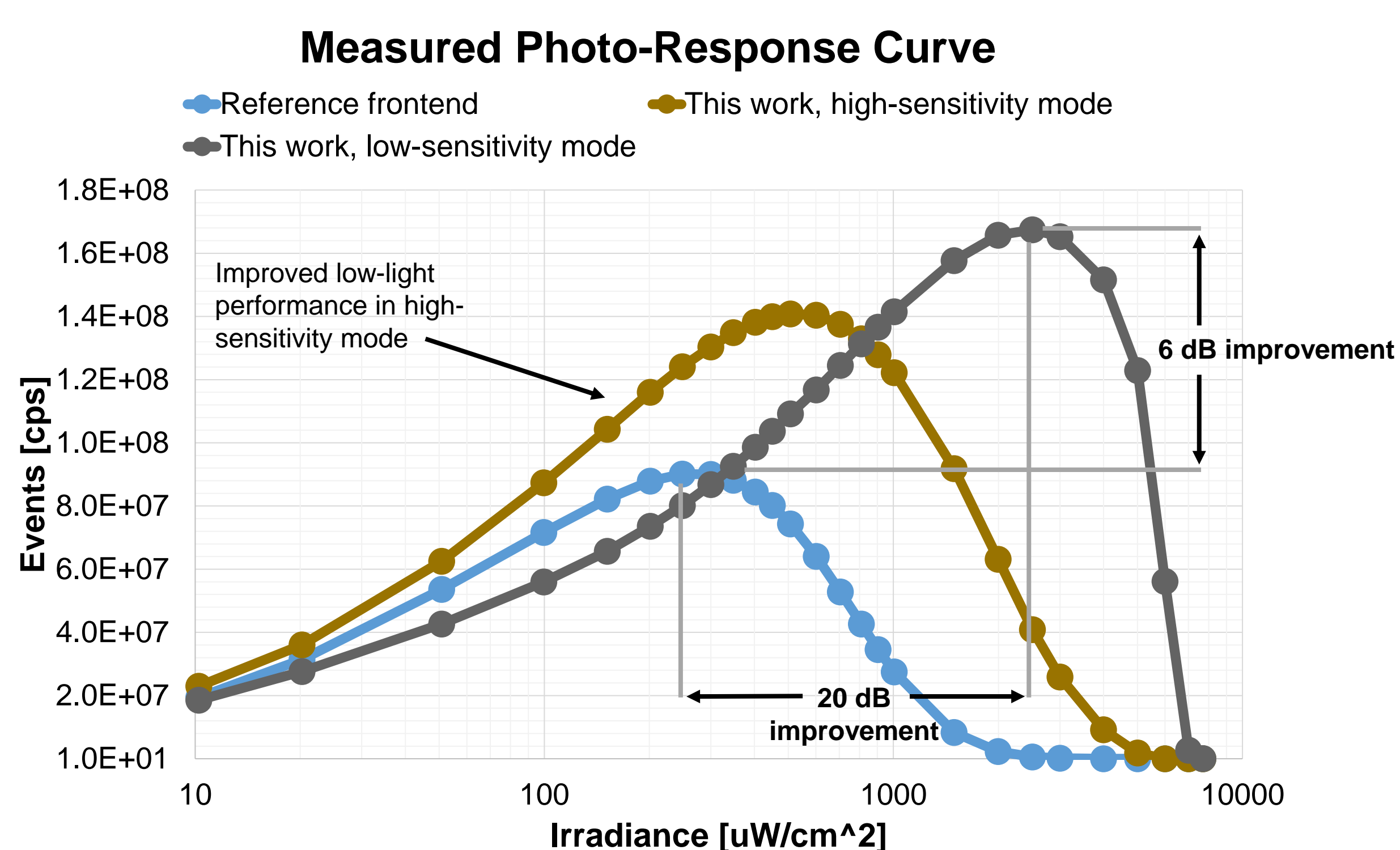


Execution: Test Chip



- Tapeout in ST's 3D40 SPAD stacked process.
- Contains many standalone SPAD pixels, small array and other test circuits.

Characterization Results



- Different sensitivity modes achievable with one front-end via VPULLUP and VHV adjustments.

State-of-the-Art

Parameter	This work	B. Mamdy [4]	K. Ito [5]	S. Shimada [6]	G. Roehrer [7], P. Taloud [8]
Technology (top/bottom tier)	90nm BSI/40nm	90nm BSI/40nm	90nm BSI/40nm	90nm BSI/22nm	45 nm BSI/22nm
Pixel pitch [μm]	10.17/4.1*	10.17	10.00	6.00	10.00
Fill factor [%]	~100	~100	~100	~100	N/A
Dynamic range [dB]	87	100	144	130	157
Max. count rate [Mcps]	167/141**	85	50	60	53
Peak PDE [%]	51.5 (@570 nm)	40.8 (@635 nm)	53.5 (@650 nm)	66.7 (@650 nm)	N/A
PDE@940nm [%]	14.4	18.5	14.2	20.2	11
DCR [cps/pix]	7934 (@27°C)	810 (@60°C)	3 (@25°C)	19 (@25°C)	0.7 (@25°C)
Timing jitter FWHM [ps]	419 (@773 nm)	119	173	137	120 (@940 nm)

* Pitch of the pixel fronted circuit on the bottom tier wafer.
** Low-sensitivity mode/high-sensitivity mode.

References and Acknowledgements

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- [2] P. Padmanabhan et al., "A 256 × 128 3D-Stacked (45nm) SPAD FLASH LiDAR with 7-Level Coincidence Detection and Progressive Gating for 100m Range and 10klux Background Light," IEEE ISSCC 2021.
- [3] A. Gulinatti et al., "35 ps time resolution at room temperature with large area single photon avalanche diodes," IET Electronic Letters, vol. 41, no. 5, pp. 272–274, Mar. 2005.
- [4] B. Mamdy et al., "A high PDE and high maximum count rate and low power consumption 3D-stacked SPAD device for Lidar applications," IISW 2023.
- [5] K. Ito et al., "A Back Illuminated 10μm SPAD Pixel Array Comprising Full Trench," IEEE IEDM 2020.
- [6] S. Shimada et al., "A Back Illuminated 6 μm SPAD Pixel Array with High PDE and Timing Jitter Performance," IEEE IEDM 2021.
- [7] G. Roehrer et al., "A Back Side Illuminated 3D-Stacked SPAD in 45nm Technology," ISSW 2022
- [8] P. Taloud et al., "A 1.2K dots dToF 3D Imaging System in 45/22nm 3D-stacked BSI SPAD CMOS," ISSW 2022.

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