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INTERNATIONAL IMAGE SENSOR SOCIETY

ISSW 2024 THE INTERNATIONAL SPAD SENSOR WORKSHOP

A 1.8-μm pitch, 47-ps jitter SPAD Array in 130nm SiGe BiCMOS process

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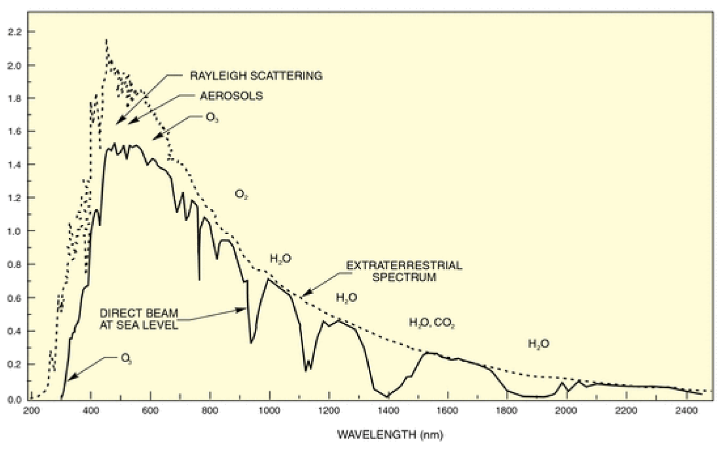
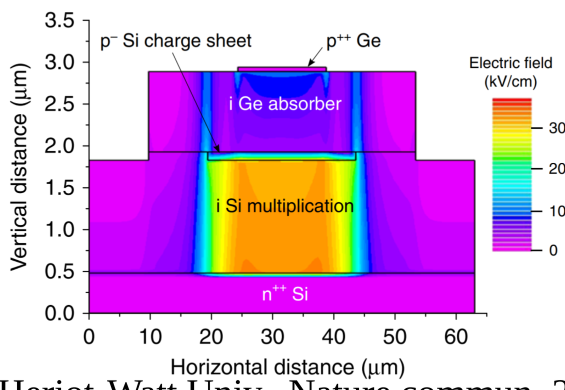
EPFL

宇称电子 MICROPARITY Sensor and Science

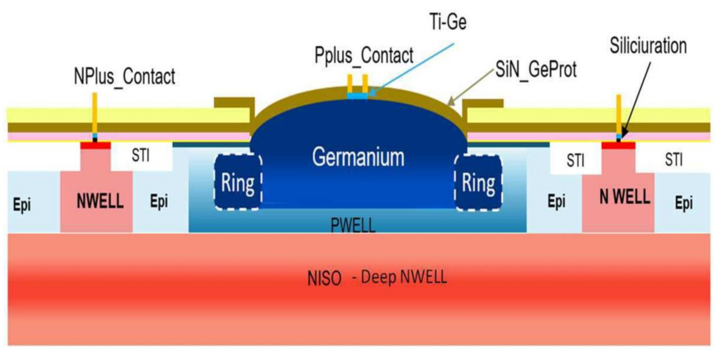
Introduction

- SiGe SPAD (SWIR)
  - Decreased solar background
  - Higher eye-safety threshold
  - Decrease in scattering from particles
  - More expensive, higher dark counter rate…
- Device Miniaturization and Large Format Camera
- SiGe SPAD Approach





Heriot-Watt Univ., Nature commun. 2019

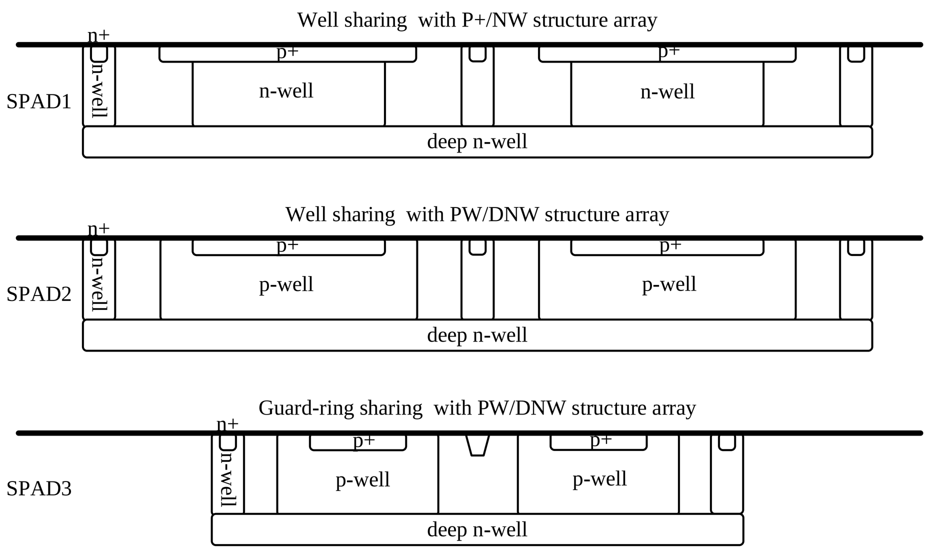


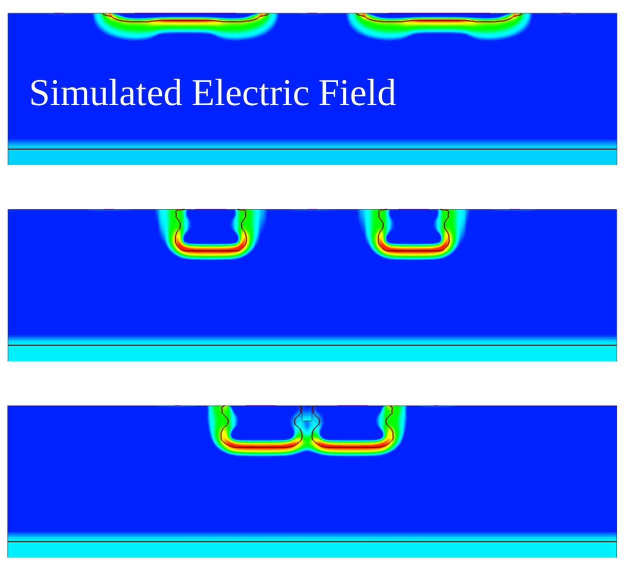
STMicroelectronics, IISW2023

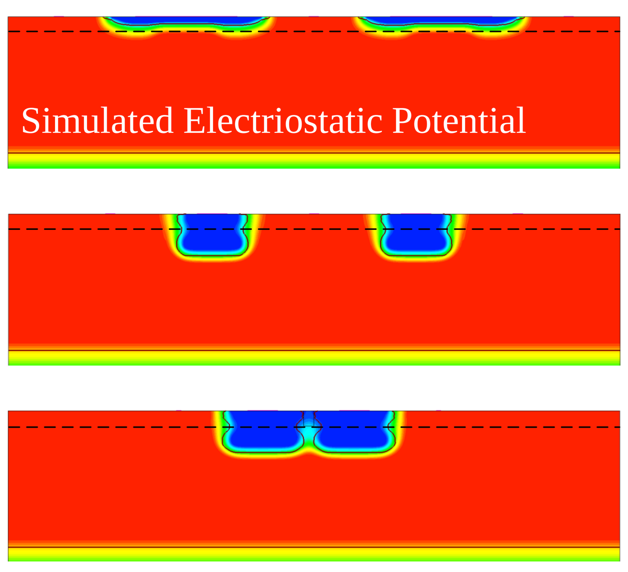
SPAD and Circuit Design

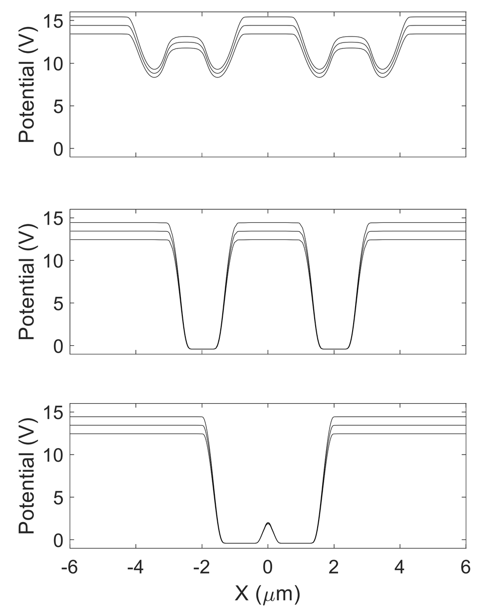
- Silicon SPAD device
  - First attempt to design SPAD in BiCMOS process
  - A series of SPAD structures and sharing techniques were implemented

	SPAD1	SPAD2	SPAD3
Structure	p+/nw	pw/dnw	pw/dnw
Array sharing	nw	nw	guard ring
Pitch (μm)	11.3	8.3	1.8
Draw active diameter (μm)	5.0	5.2	1.0
Fill factor (%)	15.3	30.9	24.2

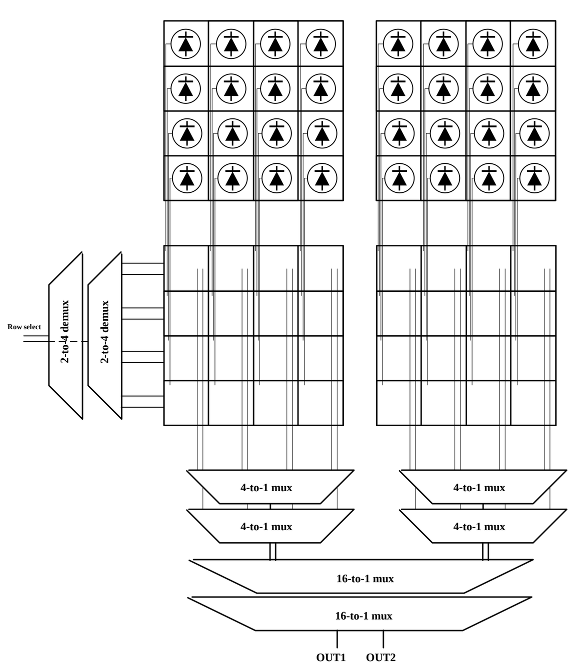




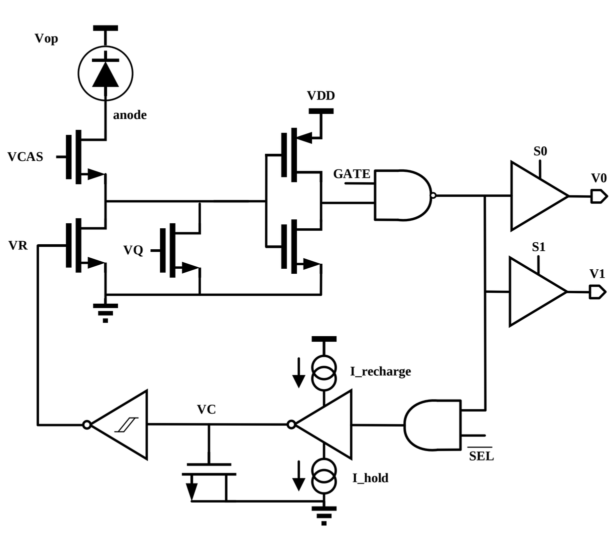




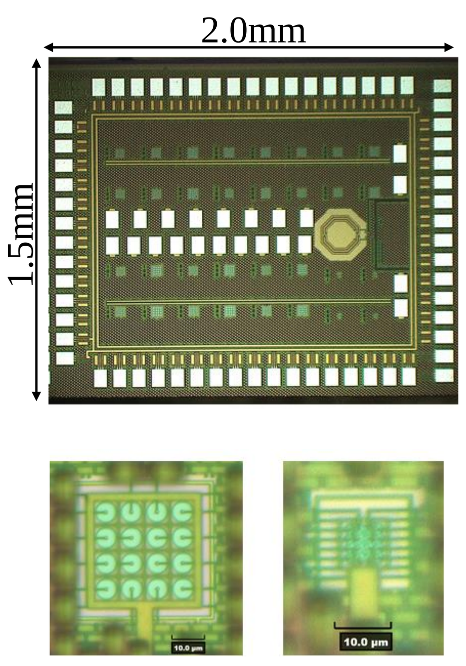
- Circuit Design



4×4 array circuit



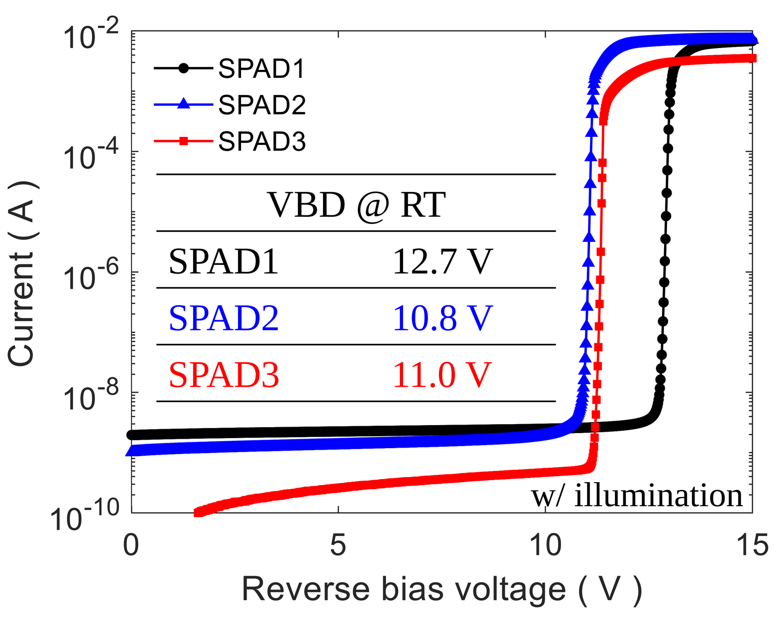
pixel circuit

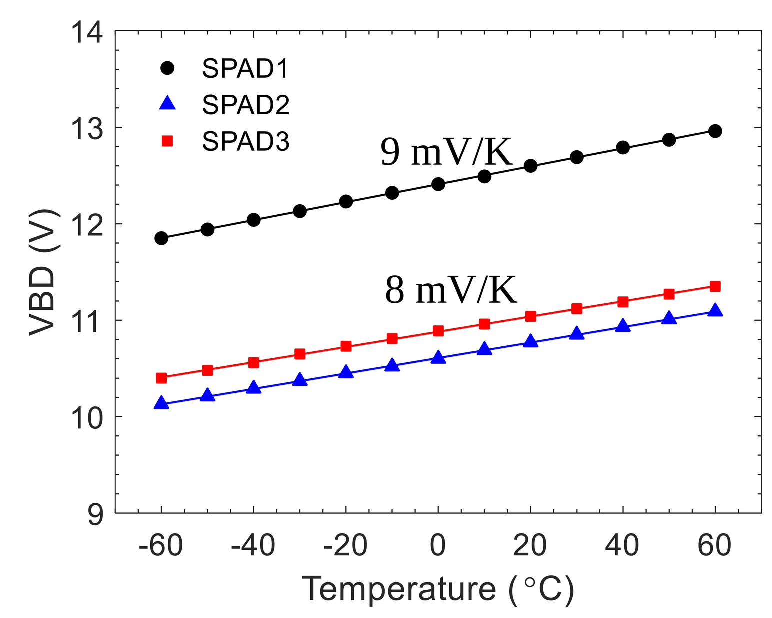


micrograph

Measurement Results(A)

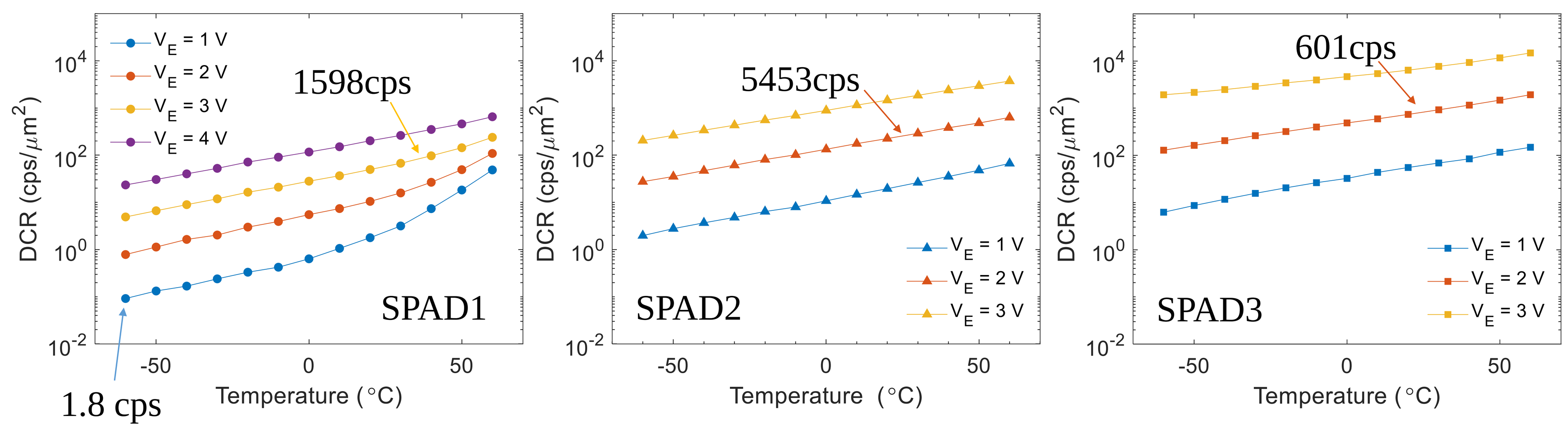
- Breakdown voltage & temperature dependence



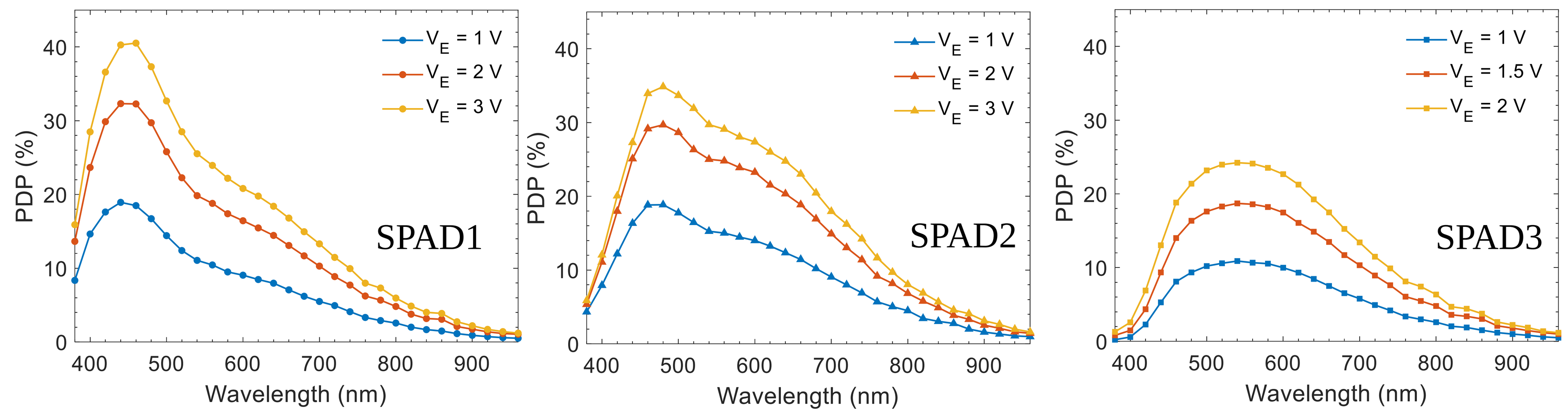


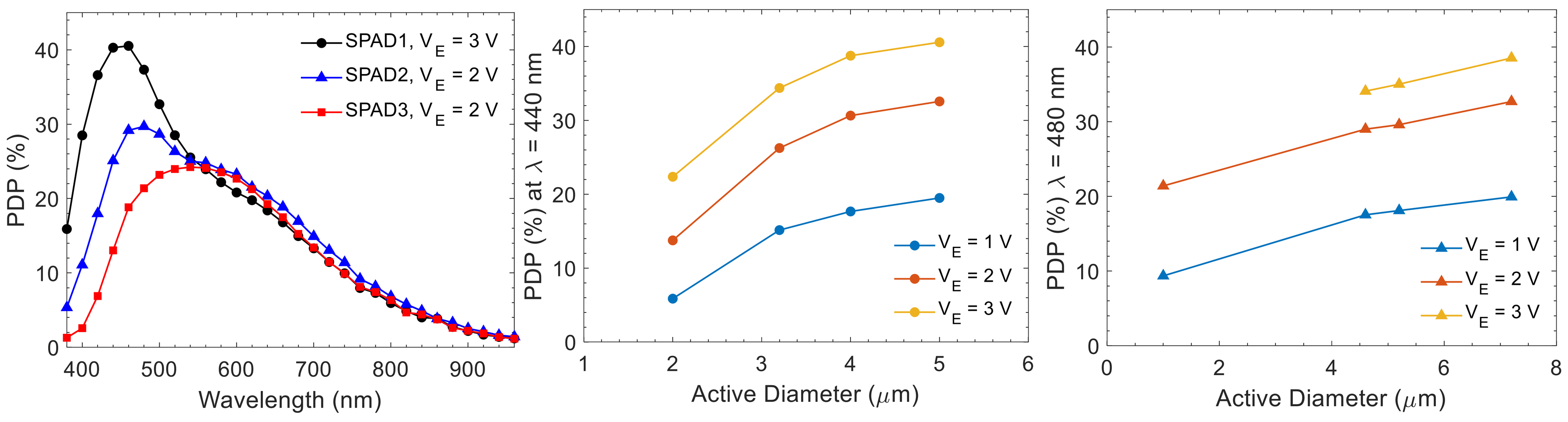
Measurement Results(B)

- Dark Count Rate(DCR)



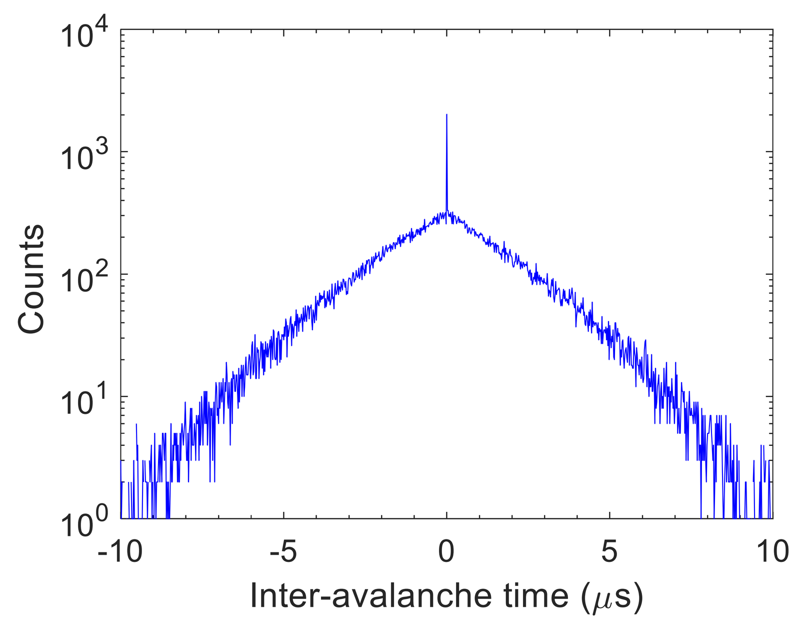
- Photon Detection Probability (PDP)

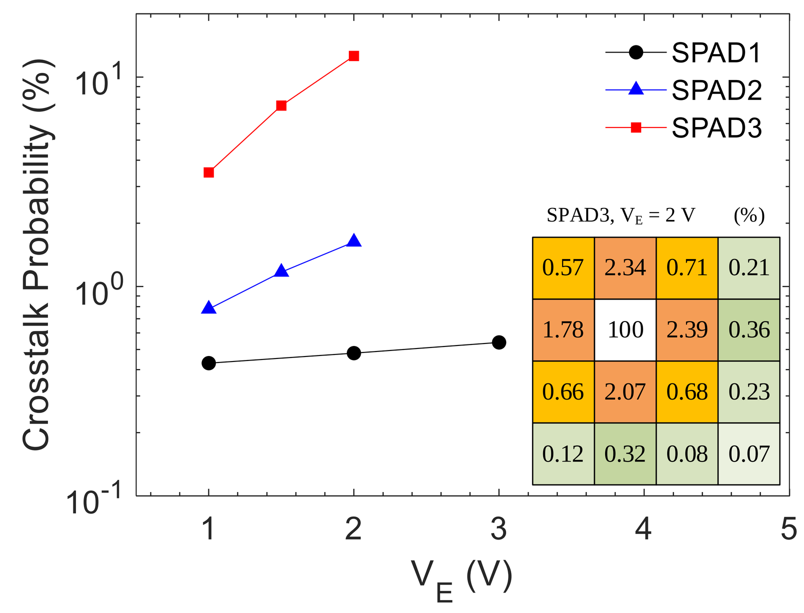




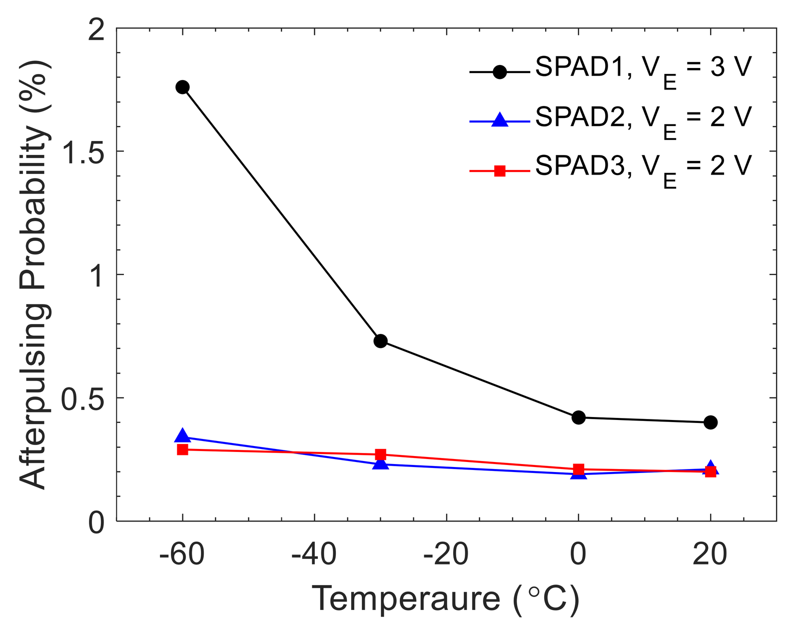
*measured PDP is corrected after removing afterpulsing and crosstalk probability.

- Crosstalk Probability (Xtalk)

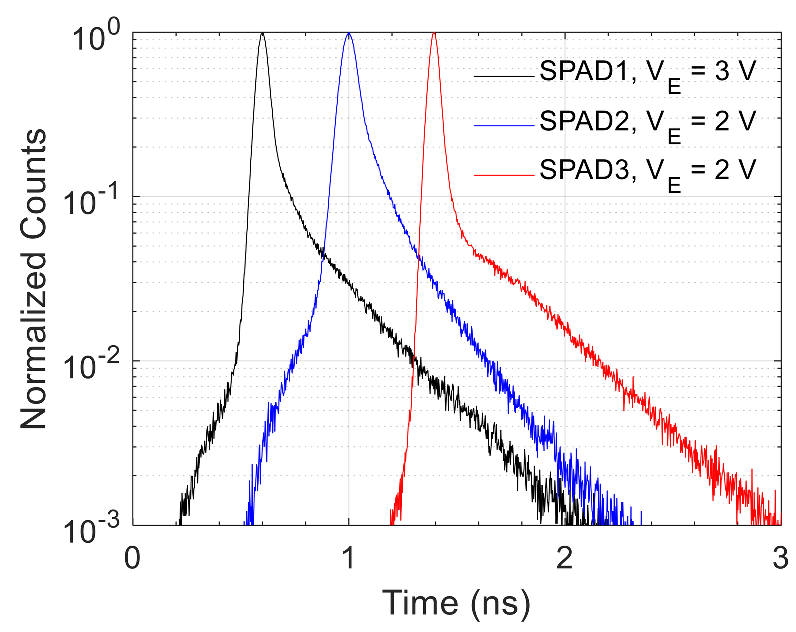




- Afterpulsing Probability



- Timing Jitter @850nm



Comparison and Conclusion

- First fully characterized silicon SPAD in SiGe BiCMOS process.
- Smallest SPAD array (1.8-μm) using guard ring sharing technique.
- Better timing jitter (< 50 ps) at low excess bias voltage.
- For possible future research on SiGe SPAD: Cryogenic characterization for quantum application, Ge layer implemented on Si SPAD with process optimization, etc.

	2010[1]	2017[2]	2020[3]	2022[4]	2023[5]	This work			
Technology (nm)	FSI 90nm	FSI 130nm	FSI 180nm	BSI-3D 90nm	BSI-3D 90nm	SiGe FSI 130nm			
Pitch (μm)	5	3	2.2	2.5	3.06	11.3	8.3	1.8	1.8
Array size	3×3	4×4	4×4	N/D	160×264	4×4	4×4	4×4	4×4
Fill Factor (%)	12.5	14	19.5	N/D	N/D	15.3	30.9	24.2	24.2
VBD (V)	10.3	15.8	32.35	18	20.9	12.7	10.8	11.0	11.0
VE (V)	0.6	3.2	4	3	3	3	2	1	2
Median DCR (cps)	250	150[a]	751	173	15.8	1598	5453	36.9	601
Peak PDP (%)	36	15	10.3	N/D	N/D	40.6	29.5	9.4	21.4
Peak PDE (%)	4.5	2.1	2.0	76.1	57	6.2	9.1	2.3	5.2
Crosstalk (%)	<0.1	<0.2[a]	2.97	1.0	<0.4	0.5	1.6	3.5	12.6
Afterpulsing probability (%)	N/D	0.18[a]	<0.2	<0.1	N/D	0.4	0.21	<0.2	0.2
Dead time (ns)	N/D	10	10	6.0	N/D	5.0	5.0	5.0	5.0
Timing Jitter (ps)	107	176	72	214	N/D	55	84	49	47

[a] The data was measured at 1V excess bias voltage.

[1] Robert K. Henderson, IEDM 2010

[2] You Ziyang, IISW 2017

[3] Kazuhiro Morimoto, Optics Express 2020

[4] Shohei Shimada, IEDM 2022

[5] Jun Ogi, IISW 2023