P1.12

Histogram-less SPAD/SiPM-based dTOF imaging with parallel ML processing

Tommaso Milanese*, Jiuxuan Zhao*, Brent Hearn†, Edoardo Charbon*

*AQUA laboratory, École Polytechnique Fédérale de Lausanne, Neuchâtel
†Imaging division, STMicroelectronics, Edinburgh, U.K.

Multi-pixel event-based histogram-less processing

- Parallel timestamp processing with ML for 10 SPAD pixels.
- We extend our previous work [1] from **single pixel** to **10 pixels.**

	Standard TCSPC	Our approach
Speed	**Low**	**High**
Memory	**High**	**Low**

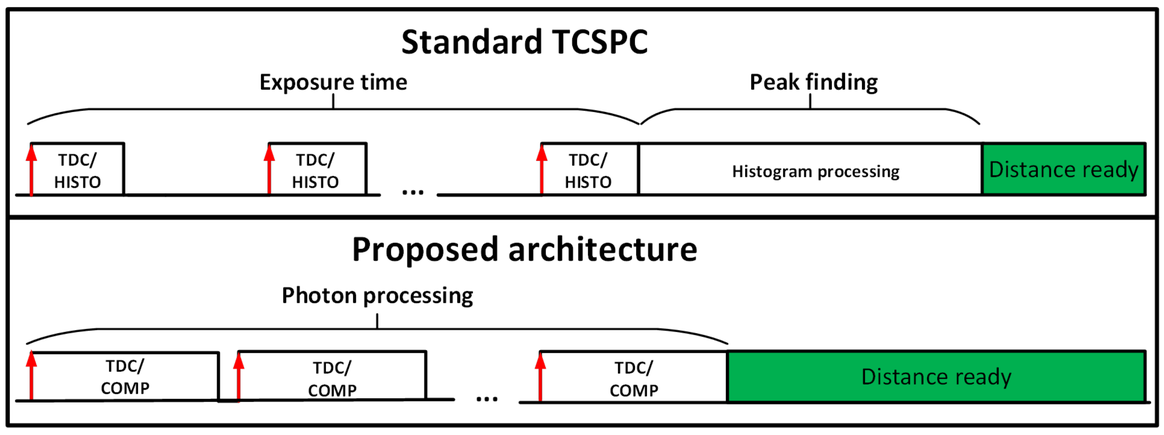


Figure 1: Timing diagram of the proposed histogram-less timestamps processing technique.

IC & FPGA architecture

- Integrated SPAD gating.
- Gradient-gating.

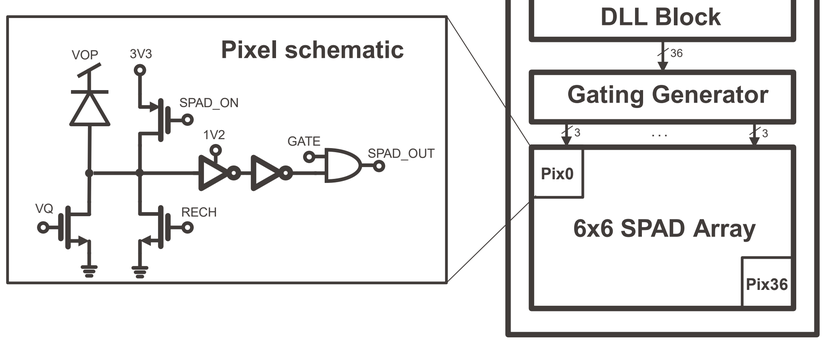


Figure 2: Chip architecture [2].

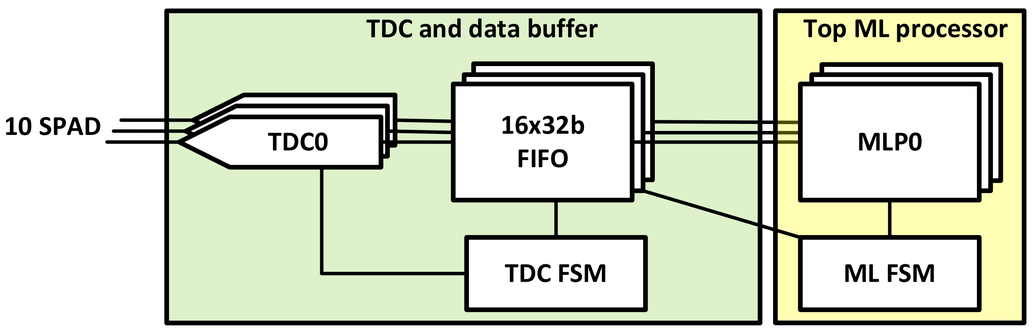


Figure 3: System architecture. 10 parallel TDC channels and 10 ML processors. The single ML processor is shown in Fig.4.

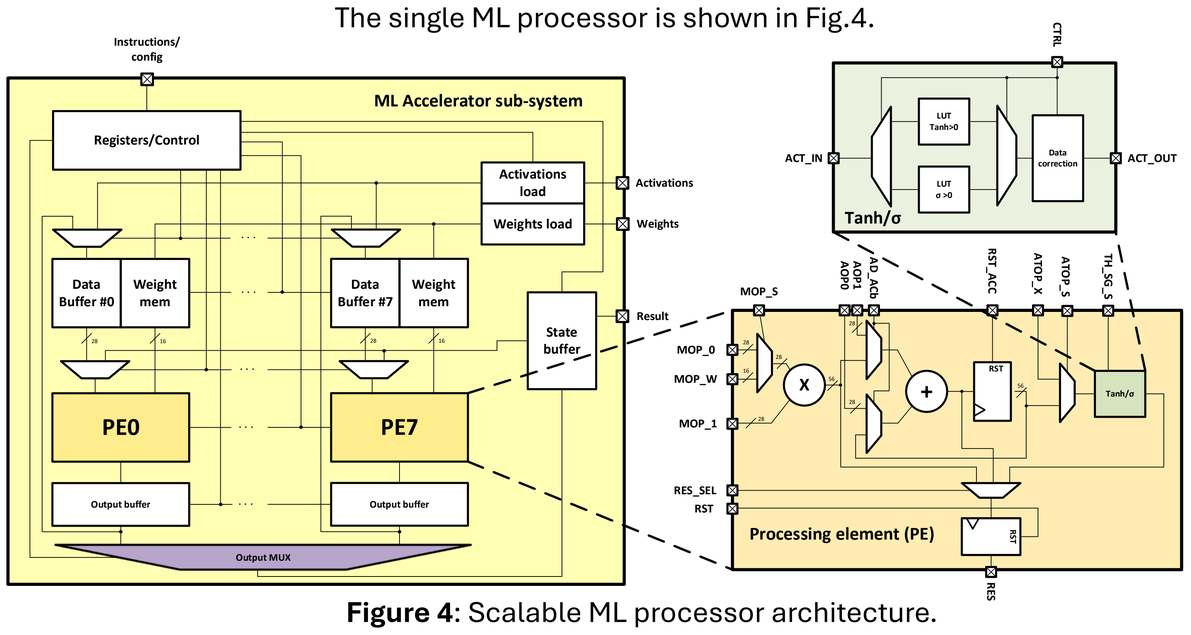
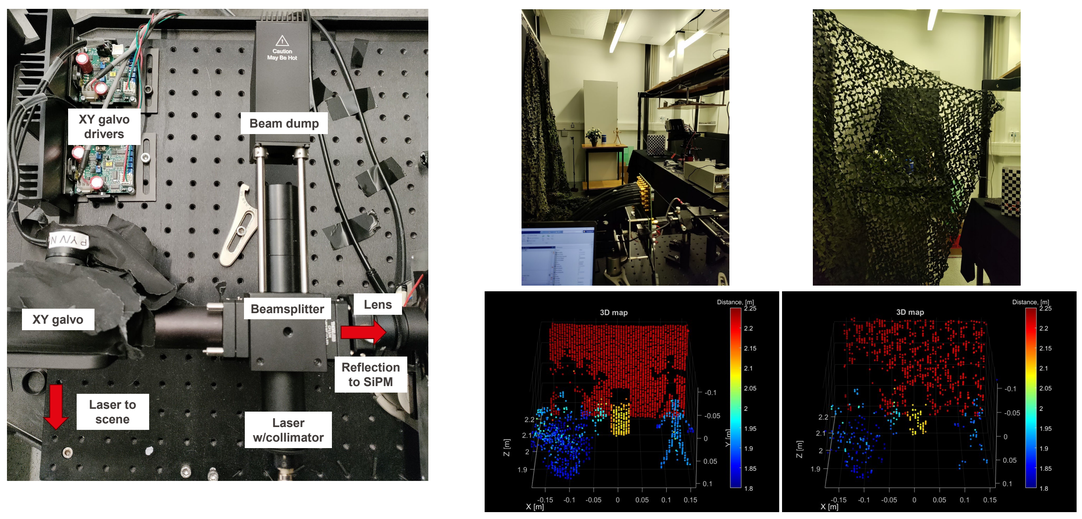


Figure 4: Scalable ML processor architecture.

Line-of-sight and non-line-of-sight results



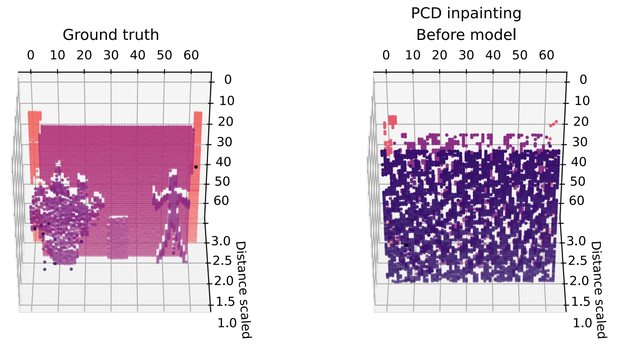


Figure 5: Experimental setup used in standard DToF [3] and results before/after CNN reconstruction .

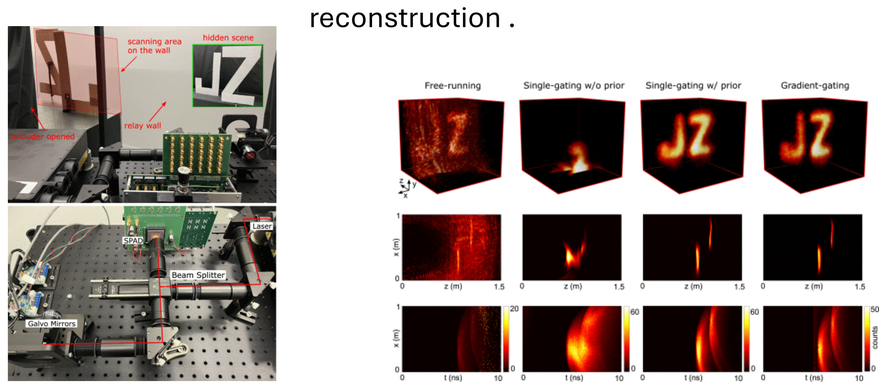


Figure 6: Non-line-of-sight setup and reconstruction result [2].

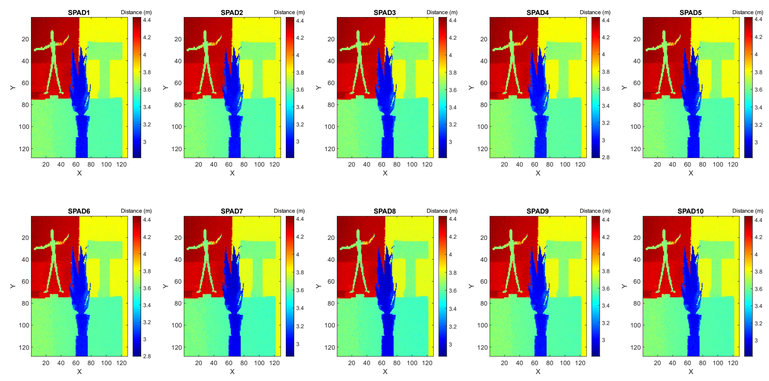


Figure 7: FPGA emulation of line-of-sight histogram-less reconstruction with 10 parallel channels. The setup used is shown in Fig.5.

Conclusions & Future work

- The scalability of our histogram-less approach has been shown.
- Table 1 shows a comparison with state-of-the-art DToF systems.

	This work	[4]	[5]	[6]
Memory per TDC [bytes]	**127**	22000	4125	48
Channels	**10**	16	1	4800
Histogram technique	**N.A.**	Full	Full	Partial

Table 1: Comparison between standard TCSPC works and our timestamp processing approach.

- Envisioned future work is scaling the approach to kpixels and Mpixels SPAD arrays.

References

[1] Milanese, Tommaso, et al. "Histogram-less direct time-of-flight imaging based on a machine learning processor on FPGA.“, *Int. Image Sensor Workshop*. 2023.
[2] Zhao, Jiuxuan, et al. "A Gradient-Gated SPAD Array for Non-Line-of-Sight Imaging." *IEEE Journal of Selected Topics in Quantum Electronics* (2023)..
[3] Zhao, Jiuxuan, et al. "On analog silicon photomultipliers in standard 55-nm BCD technology for LiDAR applications." *IEEE Journal of Selected Topics in Quantum Electronics* 28.5: Lidars and Photonic Radars (2022): 1-10.
[4] Niclass, Cristiano, et al. "A 100-m Range 10-Frame/s 340X96-Pixel Time-of-Flight Depth Sensor in 0.18-um CMOS." *IEEE Journal of Solid-State Circuits* 48.2 (2012): 559-572.
[5] Al Abbas, Tarek, et al. "A CMOS SPAD sensor with a multi-event folded flash time-to-digital converter for ultra-fast optical transient capture." *IEEE Sensors Journal* 18.8 (2018): 3163-3173.
[6] Stoppa, David, et al. "A reconfigurable QVGA/Q3VGA Direct time-of-flight 3D imaging system with on-chip depth-map computation in 45/40 nm 3D-stacked BSI SPAD CMOS." *Proc. Int. Image Sensor Workshop*. 2021.