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Front-side photon detection improvement of SPAD integrated in FD-SOI CMOS Technology thanks to STI patterning

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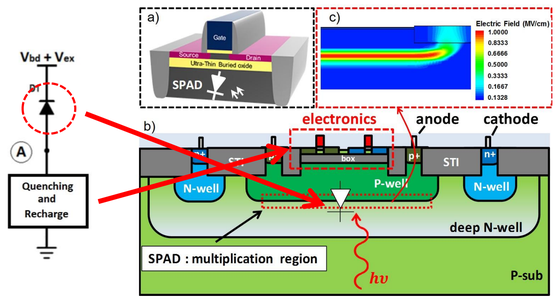
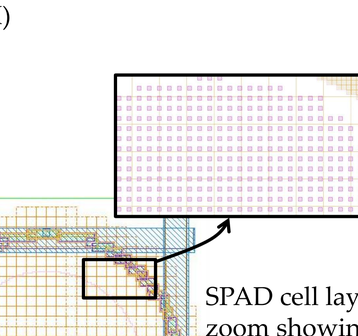
Context

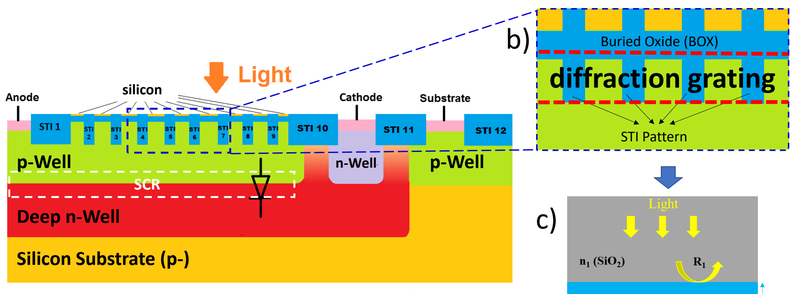
- SPAD integrated in CMOS FDSOI 28nm
- PDP improvement → Nanostructuration of STI
- Test chip designed and fabricated



Implementation of SPAD in CMOS FD-SOI technology below the thin silicon film and the buried oxide (BOX)



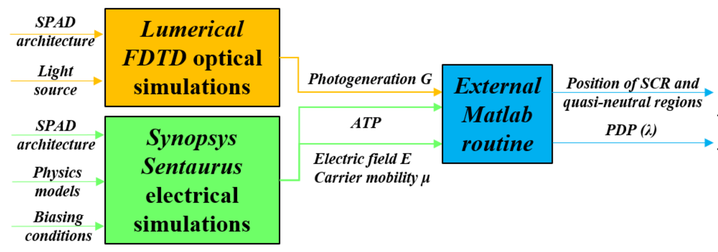
Test chip layout view



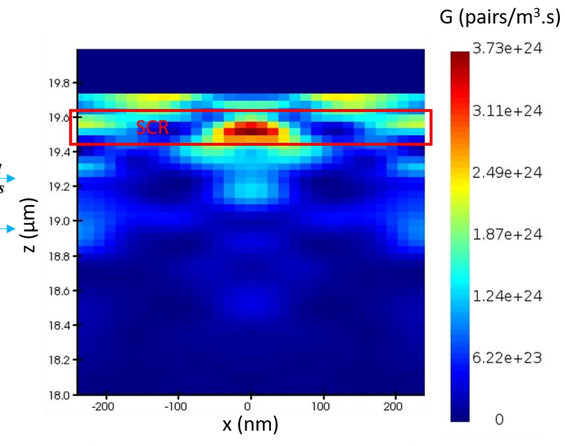
a) Schematic cross section of a SPAD FD-SOI (half-cell), b) zoom on the diffraction grating, c) simplified 1-D model for optical modelling and optimization.

SPAD cell layout zoom showing STI patterning above the photosensitive area

STI patterning simulation



Block diagram describing the methodology for estimating the photon detection probability



Cartography of photogeneration rate on periodic pattern for FF = 15% and period = 0.48µm

- Electro-optical simulation with Matlab post-processing
- Optimization of squared STI pattern
  - Fill Factor (FF) → Anti reflection
  - Period → Constructive interferences in space charge region
  - ➔ FF = 25% and 15%, period = 480nm

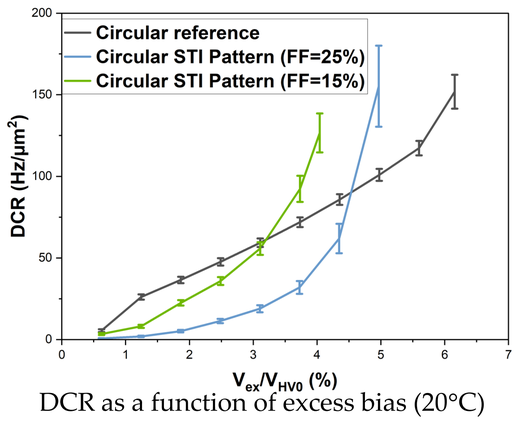
Experimental results

DCR measurements of patterned and reference SPAD

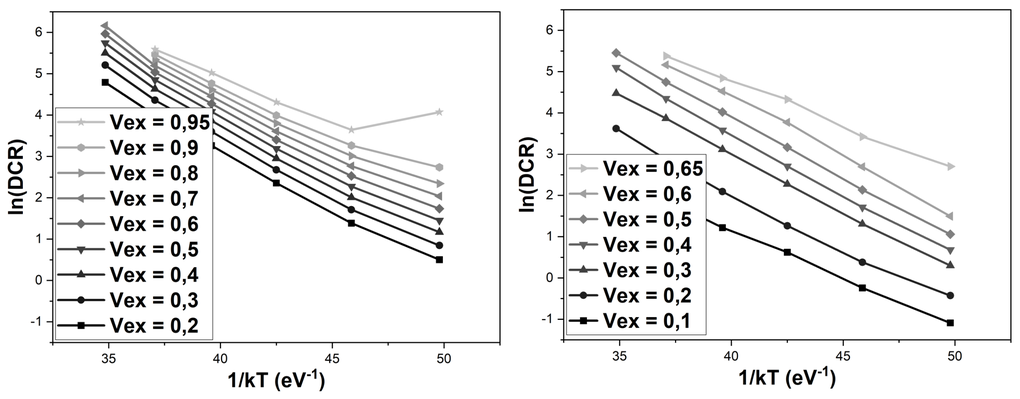
- V_{bd} = f(T) : Same V_{bd} and slope (≈20mV/K) for reference and patterned SPAD
- DCR = f(T) :

  $DCR_{FF=25\%} < DCR_{FF=15\%} < DCR_{ref}$ for $V_{ex} < 4\%$
- E_a ≈ 0.3 eV for both reference and patterned SPAD

  → presence of both SRH and B2B-TAT mechanisms



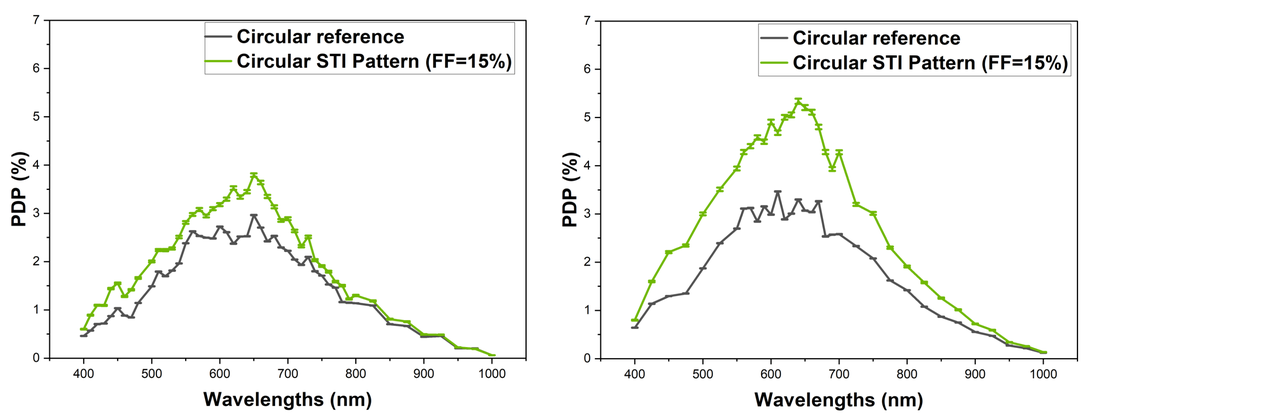
DCR as a function of excess bias (20°C)



(a) Reference SPAD (b) Patterned SPAD with FF=15%

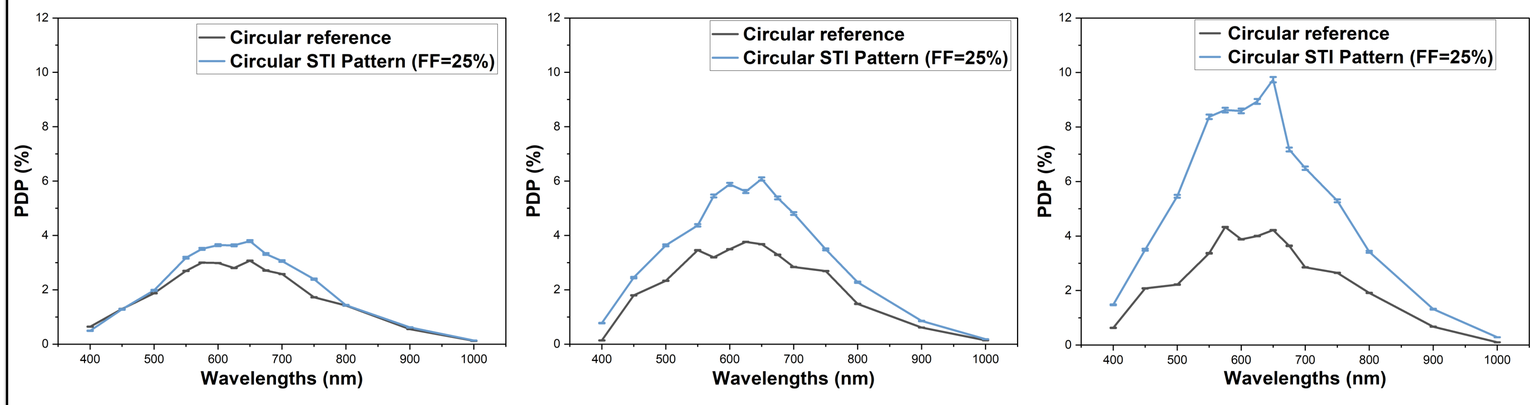
Arrhenius plot of measured DCR

PDP measurements of patterned SPAD with FF = 15%



(a) V_{ex} = 0.4V (b) V_{ex} = 0.5V

PDP measurements of patterned SPAD with FF = 25%



(a) V_{ex} = 0.5V (b) V_{ex} = 0.6V (c) V_{ex} = 0.7V

Summary of measured relative PDP gains

Fill Factor	Relative PDP gain at peak sensitivity (λ ~ 645nm)	Average relative PDP gain in the range [400nm - 1000nm]
FF =15%	28% @ V_{ex}= 0.4V	33% @ V_{ex}= 0.4V
	62% @ V_{ex}= 0.5V	55% @ V_{ex} = 0.5V
FF = 25%	23% @ V_{ex}= 0.5V	12% @ V_{ex} = 0.5V
	65% @ V_{ex}= 0.6V	53% @ V_{ex} = 0.6V
	131% @ V_{ex}= 0.7V	116% @ V_{ex} = 0.7V

- PDP improvement thanks to STI patterning
- Up to 116% average PDP improvement with similar DCR level

References

[1] T. Chaves de Albuquerque et al. “Integration of SPAD in 28nm FDSOI CMOS technology,” ESSDERC 2018 (http://dx.doi.org/10.1109/ESSDERC.2018.8486852).
[2] M. Dolatpoor Lakeh et al. “Integration of an Ultra-Fast Active Quenching Circuit with a Monolithic 3D SPAD Pixel in a 28 nm FD-SOI CMOS Technology” Sensors and Actuators: A. Physical, Volume 363, 1 December 2023, 114744 (https://doi.org/10.1016/j.sna.2023.114744).
[3] D. Issartel et al. “Architecture optimization of SPAD integrated in 28 nm FD-SOI CMOS technology to reduce the DCR,” Solid-State Electronics, Elsevier, Volume 191, April 2022, p. 108297 (https://doi.org/10.1016/j.sse.2022.108297).
[4] S. Gao et al. “Correlations between DCR and PDP of SPAD integrated in a 28 nm FD-SOI CMOS Technology” IISW 2023, available online: https://imagesensors.org/.
[5] S. Gao et al. “3D Electro-optical Simulations for Improving the Photon Detection Probability of SPAD Implemented in FD-SOI CMOS Technology” SISPAD conference, 27-29 Sept. 2021: (https://doi.org/10.1109/SISPAD54002.2021.9592555)

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