PHOTON-TO-DIGITAL CONVERTER DEVELOPMENT: 3D INTEGRATION PROGRESS AND CHARACTERIZATION PLATFORM

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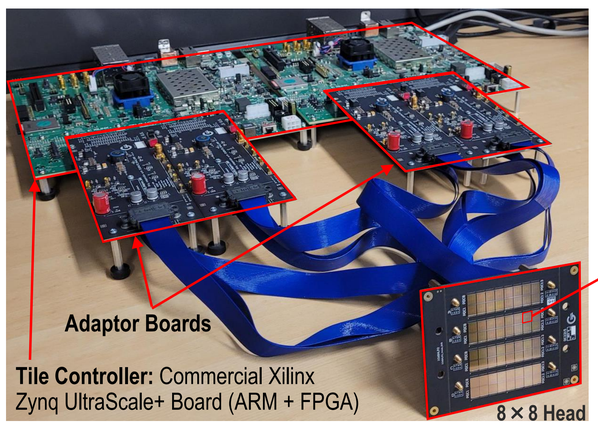
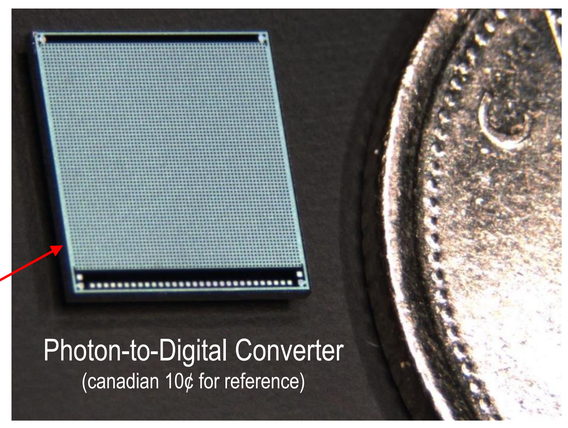
INTRODUCTION

University of Sherbrooke in partnership with Teledyne DALSA Semiconductor, is developing a Photon-to-Digital Converter (PDC) based on a TSV-less, frontside illuminated (FSI) single-photon avalanche diode (SPAD) array [1].

In the PDC, each SPAD is thinned down and vertically integrated on a quenching-readout circuit, benefiting from the digital signal processing capabilities of CMOS electronics without compromising the photosensitive area of the detector [2].

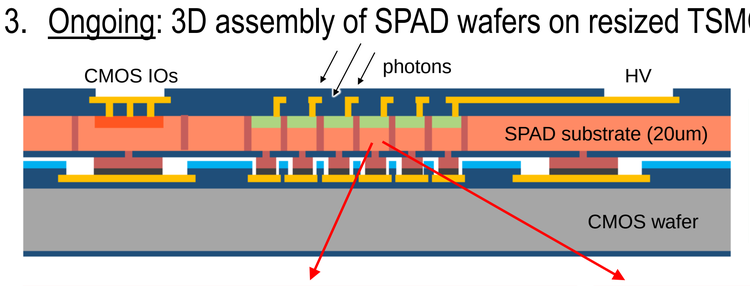
In the context of large-scale photosensitive panels, we have built an 8x8 PDC tile prototype. A tile controller ASIC is currently in development to replace the FPGA boards.



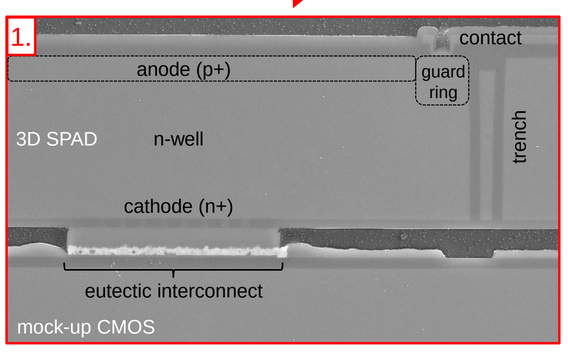


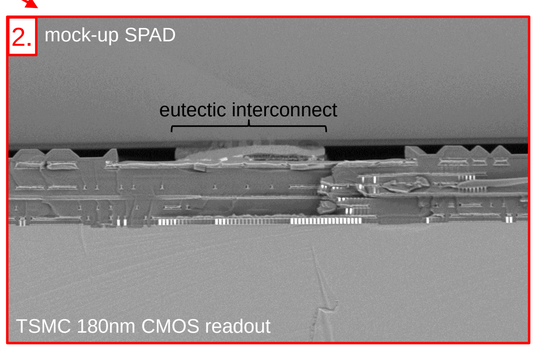
FABRICATION OF THE PDC IN MULTIPLE PHASES

1. Demonstration of the SPAD technology and 3D assembly on a mock-up CMOS wafer.
2. Demonstration of the 3D assembly of a mock-up SPAD wafer on a resized TSMC CMOS readout wafer.
3. Ongoing: 3D assembly of SPAD wafers on resized TSMC CMOS readout wafers.



Full-thickness opto-electrical isolation trenches surround each SPAD and enable the TSV-less architecture.

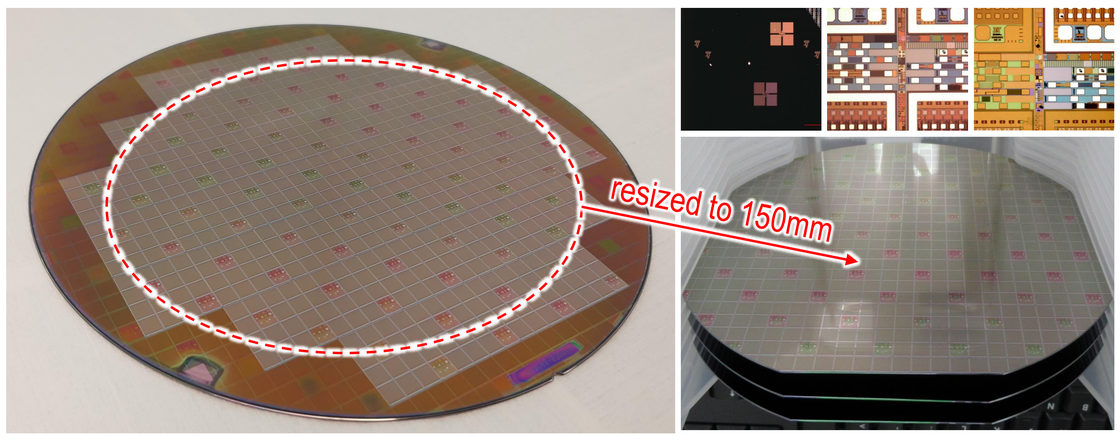




Wafer-level CMOS design and wafer resizing

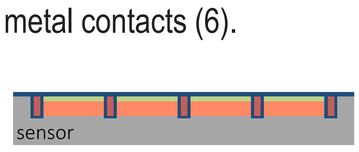
The CMOS readout circuit is fabricated in TSMC 180 nm BCD on 200 mm wafers [3]. A compounded 16-die pattern is repeated on the wafer. It is composed of 14 CMOS readouts and 2 process control & monitoring dies (PCM).

The SPAD wafer layout was adjusted to match perfectly the CMOS wafer layout and the test structures added by the foundry during tape-out. Additionally, the CMOS wafers were resized to 150 mm, allowing 3D assembly with the 150 mm SPAD wafers.

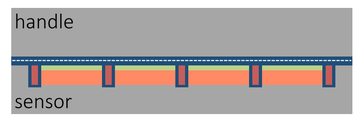


3D SPAD process overview

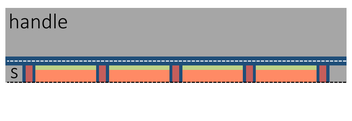
The SPAD junction profile and trenches are done first (1). The SPAD's frontside is bonded to a handle wafer (2), acting as a mechanical support during the SPAD's backside thinning (3). The thinned down SPAD and handle are 3D-bonded to the CMOS wafer using a eutectic bonding (4). The handle wafer is removed (5) to reveal the SPAD and to make the metal contacts (6).



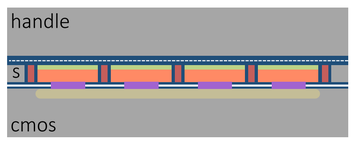
1. SPAD frontend (pn junction & trenches)



2. Handle wafer direct bonding



3. SPAD backside thinning

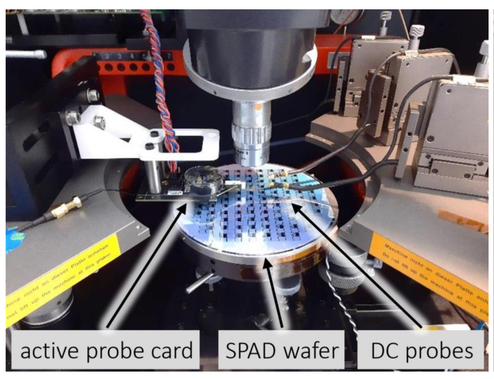


4. Al-Ge wafer-to-wafer 3D bonding

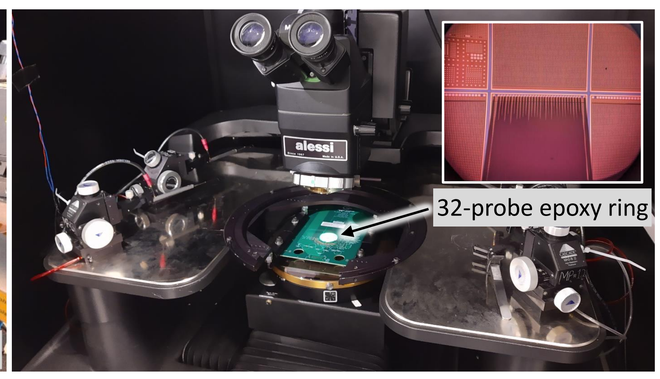
5. Handle wafer removal

6. SPAD backend (metal contacts)

CHARACTERIZATION METHODS AT WAFER-LEVEL



Single-probe quenching circuit for SPAD testing in Geiger-mode [4,5]

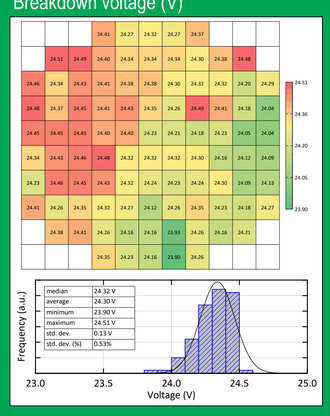


Passive (I-V charac.) or active (with tile controller) probe card for PDC characterization

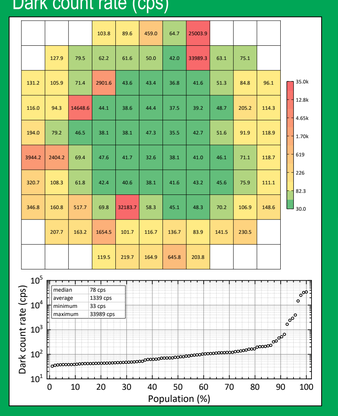
RESULTS

Single pixel in PCM over 3D SPAD 150 mm wafer

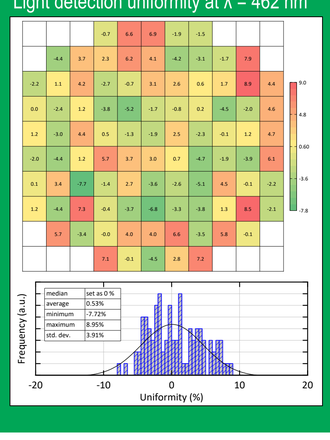
Breakdown voltage (V)



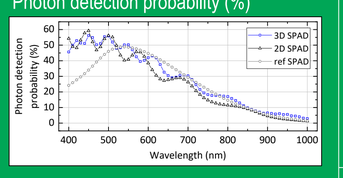
Dark count rate (cps)



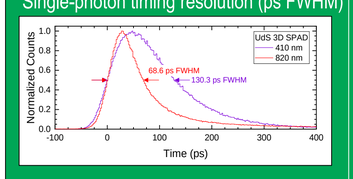
Light detection uniformity at λ = 462 nm



Photon detection probability (%)

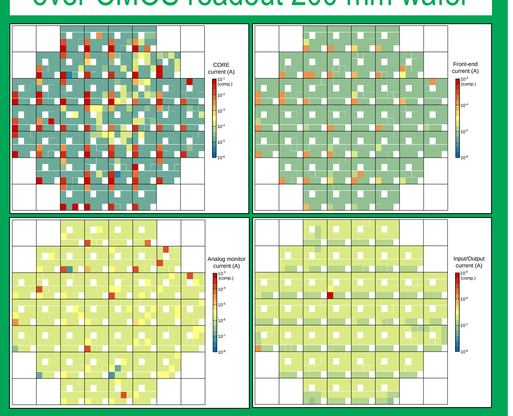


Single-photon timing resolution (ps FWHM)



*all measurements done at T = 20˚C, V_{OV} = 25% of V_{BD}

Maximum current of power domains over CMOS readout 200 mm wafer



CMOS readout

- I-V characteristics of the PDC's 4 power domains:
  - *Core* (1V8) → QC recharge/holdoff logic and digital logic
  - *Analog monitor* (5V0) → SPAD analog output equivalent
  - *Front-end* (5V0) → QC inverter, recharge/holdoff transistors
  - *Input/Output* (1V8) → digital signal output (e.g SPAD digital sum)
- Mapping revealed the bottom left PDC of each 4x4 shot to consume more power. Hypothesis suggests a layout close to the design rule limits.

3D SPAD

- The breakdown voltage is uniform throughout the wafer with a slight decrease towards the lower right-hand side (σ = 0.13 V).
- Concentric distribution of the dark noise is caused by metal contacts misalignment during in-process issues (known solution underway).
- The relative sensitivity of SPADs at λ = 462 nm is uniformally distributed and doesn't depend on the noise distribution.
- Photon detection probability peaks at 56% at 450 nm and is similar to the 2D SPAD equivalent. Diffusion of the pn junction due to added thermal steps in the 3D SPAD process explains the shift towards longer wavelengths.

CONCLUSION & OUTLOOK

- The TSV-less frontside illuminated 3D SPAD architecture is demonstrated.
- A wafer-level characterization platform allows passive and active testing of PDC wafers.
- The 3D assembly of SPAD wafers and resized TSMC CMOS readout wafers have been demonstrated, each with their mock-up wafers counterpart. 3D assembly of both functional SPAD wafers and resized TSMC CMOS readout wafers is underway.

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1. Parent, Samuel. "Design of a vertically integrated single-photon avalanche diodes, manufactured at wafer level, for a photon-to-digital converter technology." Ph.D. dissertation, University of Sherbrooke, 2022.
2. Pratte, Jean-François, et al. "3D Photon-To-Digital Converter for Radiation Instrumentation: Motivation and Future Works." Sensors 21.2 (2021): 598.
3. Rossignol, Tommy, et al. "A 3D Photon-to-Digital Converter Readout for Low-Power and Large-Area Applications." Preprint on TechRxiv, (2024).
4. Vachon, Frédéric, et al. "Measuring count rates free from correlated noise in digital silicon photomultipliers." Measurement Science and Technology 32.2 (2020): 025105.
5. Parent, Samuel, et al. "Wafer-level Characterization and Monitoring Platform for Single-Photon Avalanche Diodes.", IEEE Journal of the Electron Devices Society 12 (2024): 127-137.