Red-Enhanced SPAD Sensor with 150-ps Gating for FLIM

A. Carimatto, H. Homulle , C. Saudan, P. Keshavarzian, I. Michel Antolovic

augusto.carimatto@piimaging.com

B. Pi Imaging Technology

INTRODUCTION

Fluorescence Lifetime Imaging Microscopy (FLIM) provides a unique view on cellular dynamics and molecular interactions in living organisms [1]. FLIM can give functional information about the cells and their environment apart from the structural information that would be visualized with traditional methods. This is achieved by measuring the time it takes for fluorophores to return to their relaxed state after excitation by pulsed light. The efficacy of FLIM heavily relies on the ability to measure fluorescence lifetimes, which is the fluorophore's intrinsic property of emitting light during a unique period upon excitation. The technique relies on the precision of the sensor to measure the fluorescence lifetime and its capability to detect light, especially at the wavelength of interest. Therefore, SPAD sensors for FLIM [2] require a high Photon Detection Efficiency (PDE) with a high-precision time resolution. In this work, we present a red-enhanced SPAD sensor with gating capabilities [3], 48% PDE@640-nm/5V_{ex}, 90 cps median DCR (Dark Count Rate) and 123-ps jitter with a flexible read-out system that makes the integration of a cheap microscopy module with low complexity possible.

SYSTEM

The chip has been fully integrated with and an FPGA in a plug&play (Fig. 1) system that can be operated using a software which includes a TCP-IP interface for further integration with proprietary software. The system is equipped with 4 inputs to synchronize the chip with the scanning signals of a microscope; such as frame, line and pixel synch signals. For timing capabilities, the system has a Time-to-Digital converter (TDC) per SPAD to time stamp the photon arrival times down to 20-ps resolution. System example after integration shown in Fig. 2.

Fig. 1: Turn-key system with software for simple integration.

Fig. 2: System with the chip integrated.

ARCHITECTURE

The sensor (Fig. 3) comprises a microlensed SPAD array in a square arrangement. There are back-end pixel electronics to detect and process the pulses in two flexible modes. Gating is performed by means of a balanced tree that reaches every pixel circuitry with negligible skew. Waveforms are shown in Fig. 4. Finally, a digital core with a serial peripheral interface (SPI) is used to configure the chip.

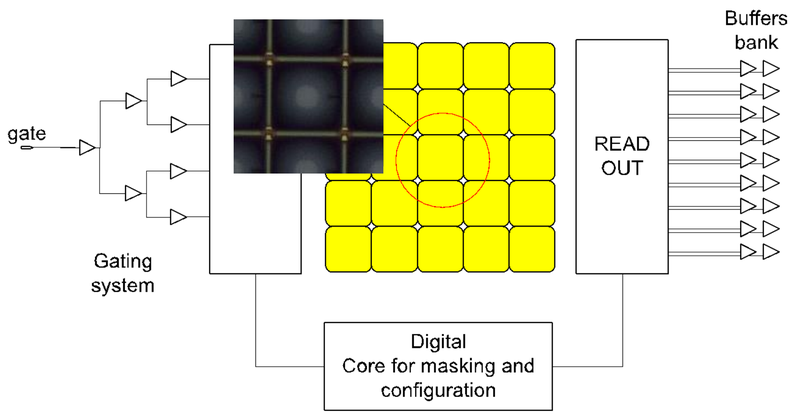

Fig. 3: Block diagram of the sensor with a micrograph picture of the microlensed pixels.

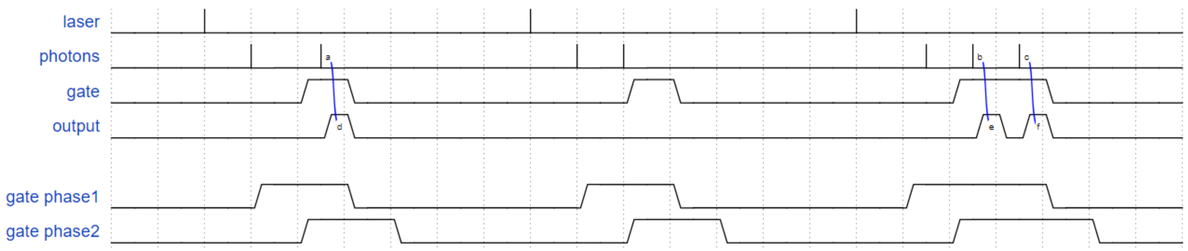

Fig. 4: Waveforms for gating operation mode.

PIXEL CIRCUITRY

Every SPAD is connected to an electronic circuit that detects the pulse and has the option to either elongate or shrink it. This feature is fully configurable with an analog voltage, allowing the user to couple the sensor to different external systems. The gating window is also applied at this stage if the sensor was programmed in this mode. Fig. 5 shows the complete scheme. A 1-bit memory can be configured from the digital core to mask the SPAD, i.e. its pulses will not be propagated to the outputs. This is useful in cases where a SPAD happens to be very noisy, and it would saturate the output if no action were taken.

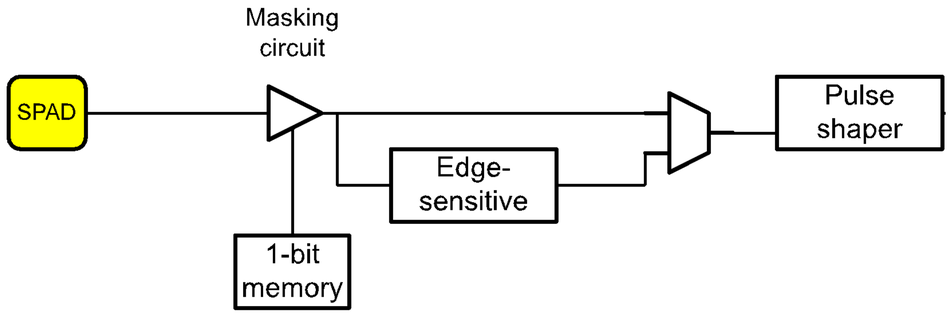

Fig. 5: Pixel circuit used to shape the signal to suit the external system.

RESULTS

The DCR has been measured at 27ºC and at an excess bias voltage of 4V. The median value is 90 cps. Gate rising and falling edges performance is shown in Fig. 6. Gate shape for all the SPADs is depicted in Fig.7 and the gate length histogram is shown in Fig. 8. Jitter has been measured by using a pulsed laser and time-to-digital converters (TDC), thoroughly explained in [4]. The complete system exhibits an average jitter of 123 ps @FWHM, shown in Fig. 9.

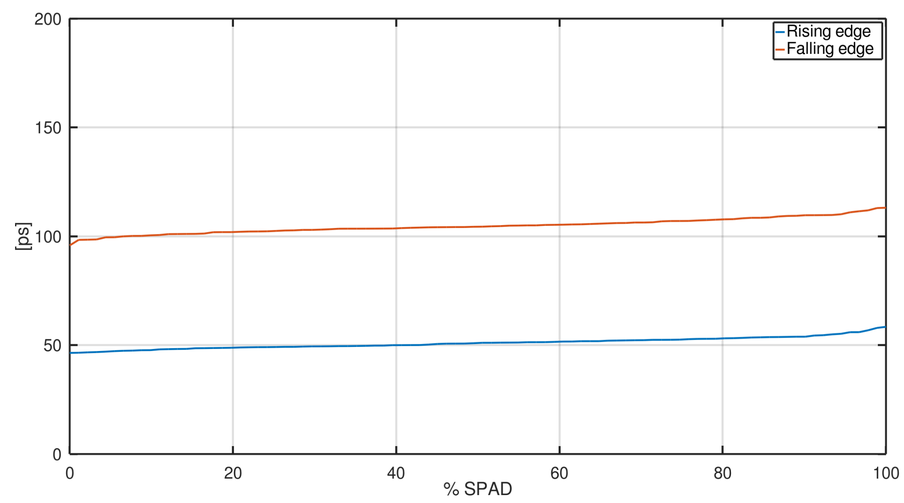

Fig. 6: Gate edge transition from 10% to 90% of the total value.

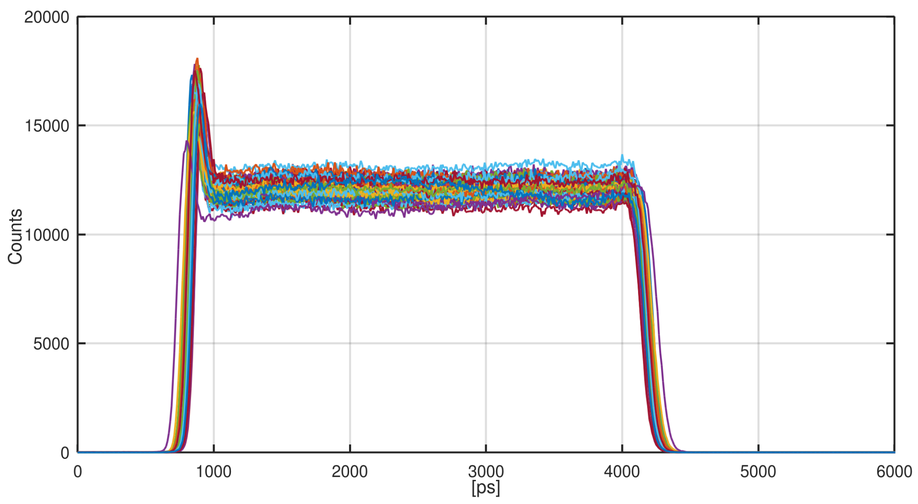

Fig. 7: Gate shape for all the SPADs

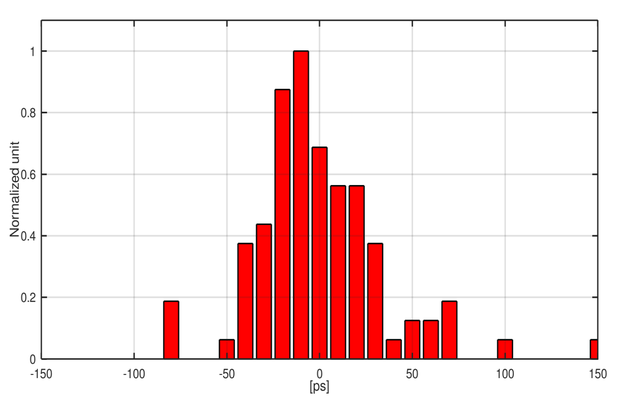

Fig. 8: gate length deviation histogram.

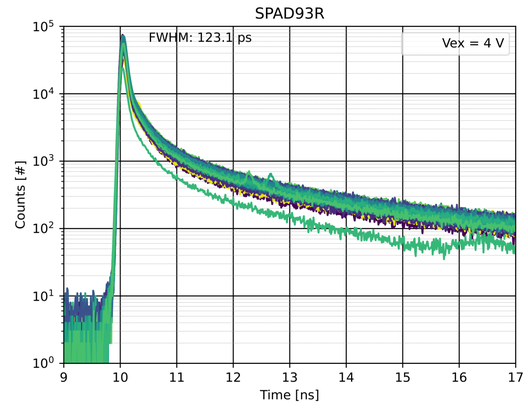

Fig. 8: gate length deviation histogram. Fig. 9: Jitter of the SPADs.

REFERENCES

1. Suhling, K., Hirvonen, L. M., Levitt, J. A., Chung, P.-H., Tregidgo, C. et al. Fluorescence lifetime imaging (FLIM): Basic concepts and some recent developments. Medical Photonics 2015, 27: 3–40
2. Henderson, R. K., Rae, B. R., Li, D.-U. Complementary metal-oxide-semiconductor (CMOS) sensors for fluorescence lifetime imaging (FLIM), chap. 11: 312–347 (Elsevier, 2014).
3. Maruyama, Y., Blacksberg, J., Charbon, E. A 1024×8, 700 ps time-gated SPAD line sensor for planetary surface exploration with laser Raman spectroscopy and LIBS. IEEE J. Solid-State Circuits 2014, 49: 179–189.
4. Mandai, S., Charbon, E. A 4×4×416 digital SiPM array with 192 TDCs for multiple high-resolution timestamp acquisition. J. Instrum. 2013, 8: P05024.

www.piimaging.com

info@piimaging.com

Pi Imaging Technology SA

EPFL Innovation Park, Bâtiment C

1015 Lausanne, Switzerland