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Recent advances in SPAD sensor technology: Pixel size shrinking and PDE enhancement

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Outline

1. Pixel size reduction in SPAD sensor development
2. Pixel size reduction to 2.5 μm
3. PDE enhancement for near infrared
4. High-resolution photon-counting image sensor
5. Challenge of reducing pixel size via new structure
6. Summary

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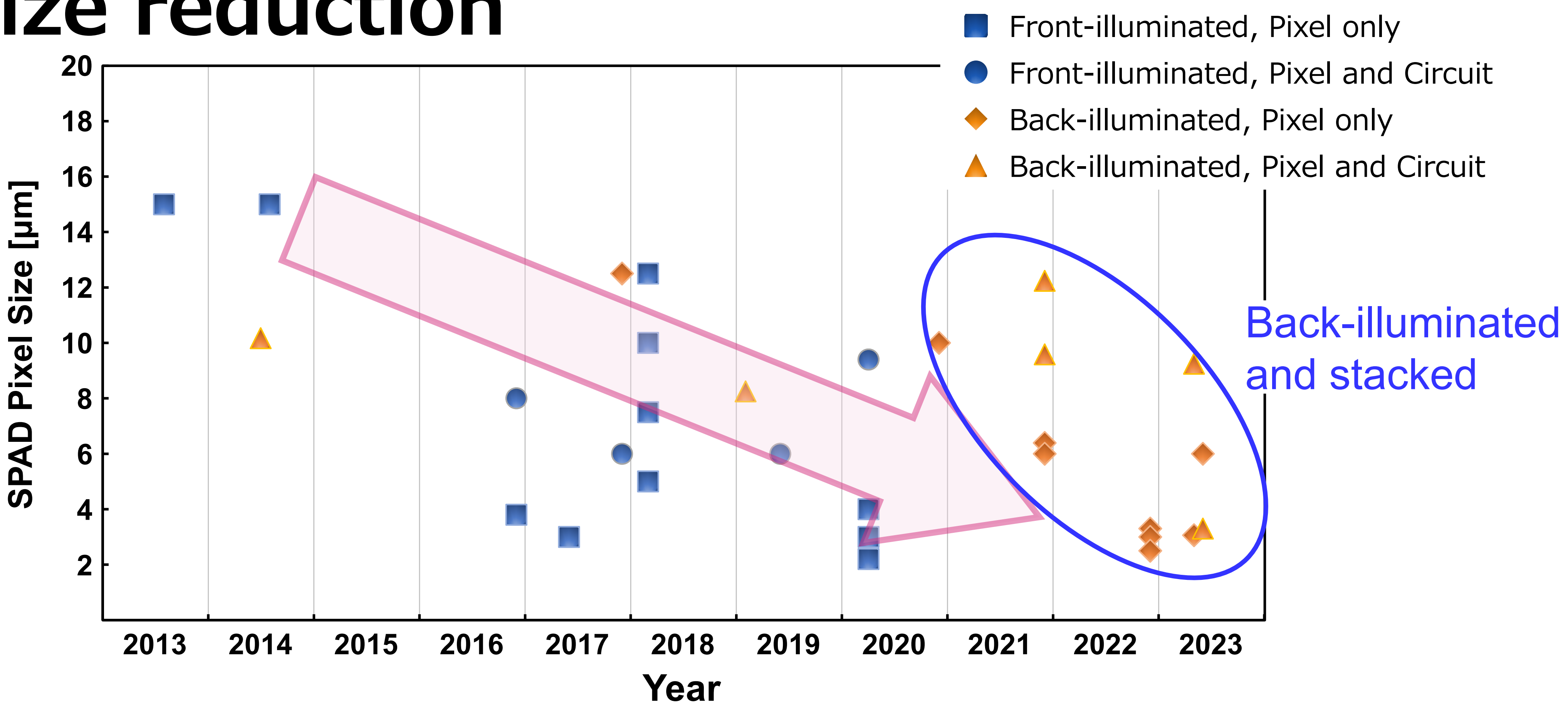
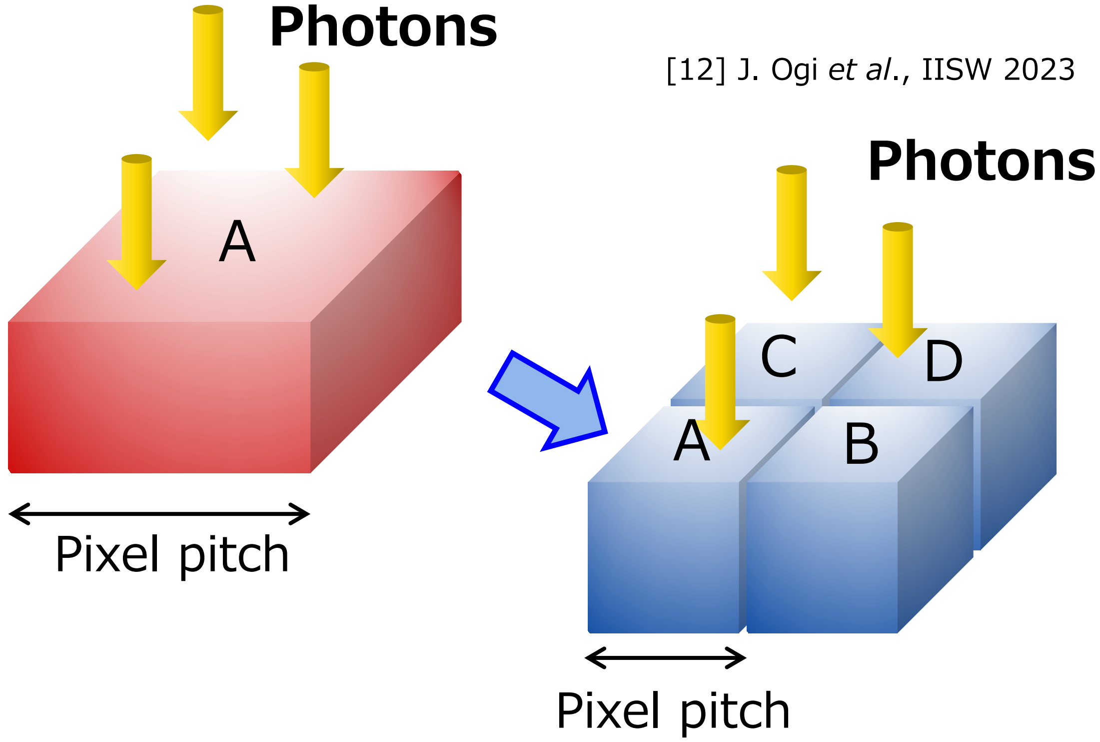
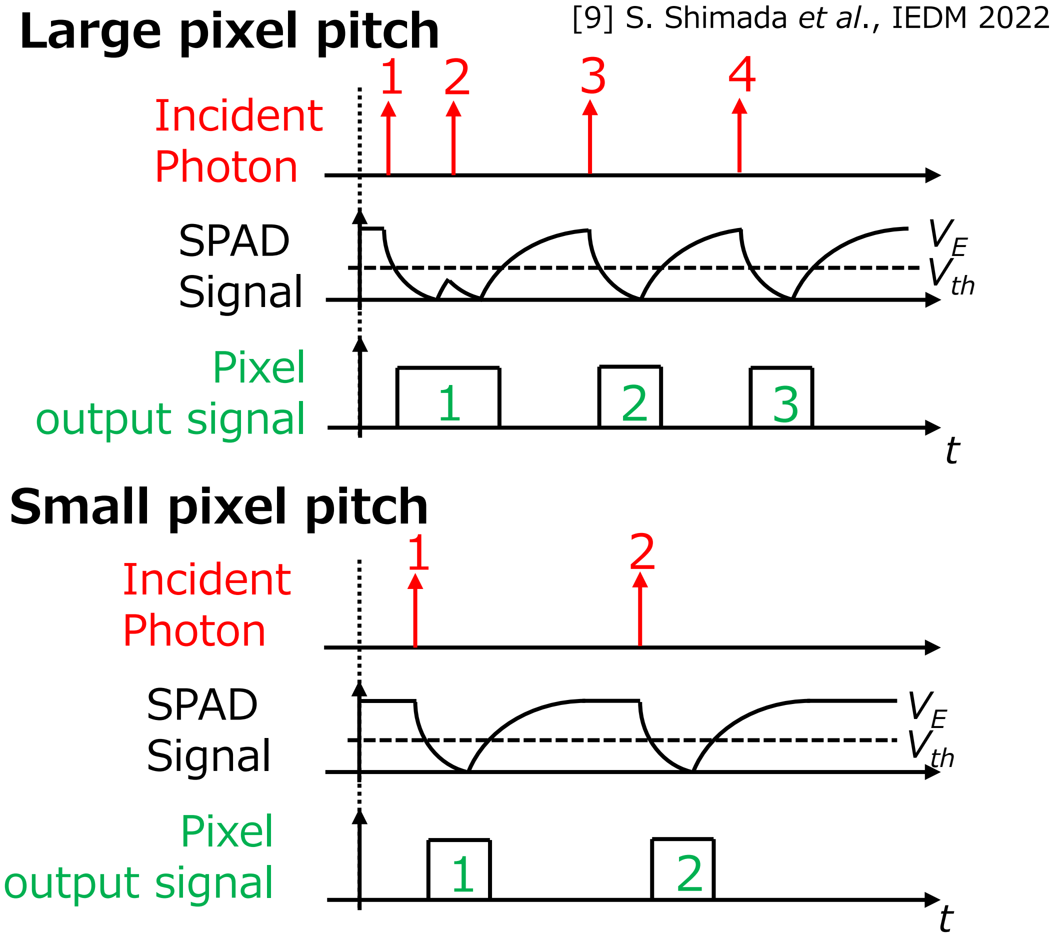
Pixel size reduction



- The SPAD pixel size has been reduced to improve the SPAD sensors performances.
- Back-illuminated and stacked technology is mainly applied in the last 3 years.

Impact of pixel size reduction

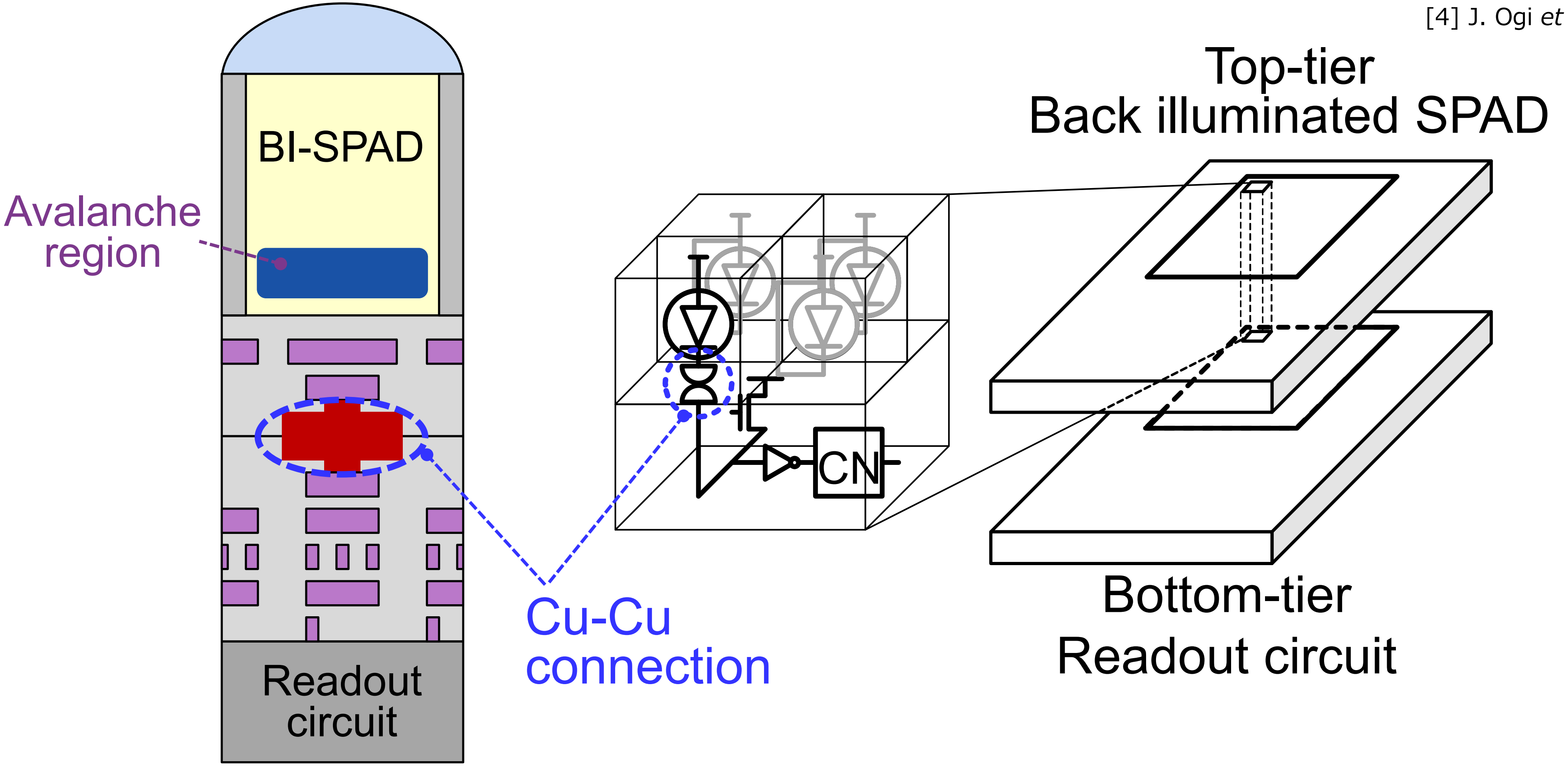




- A small pixel pitch is essential to increase the resolution
- The small pixel also contributes to detect high photon flux

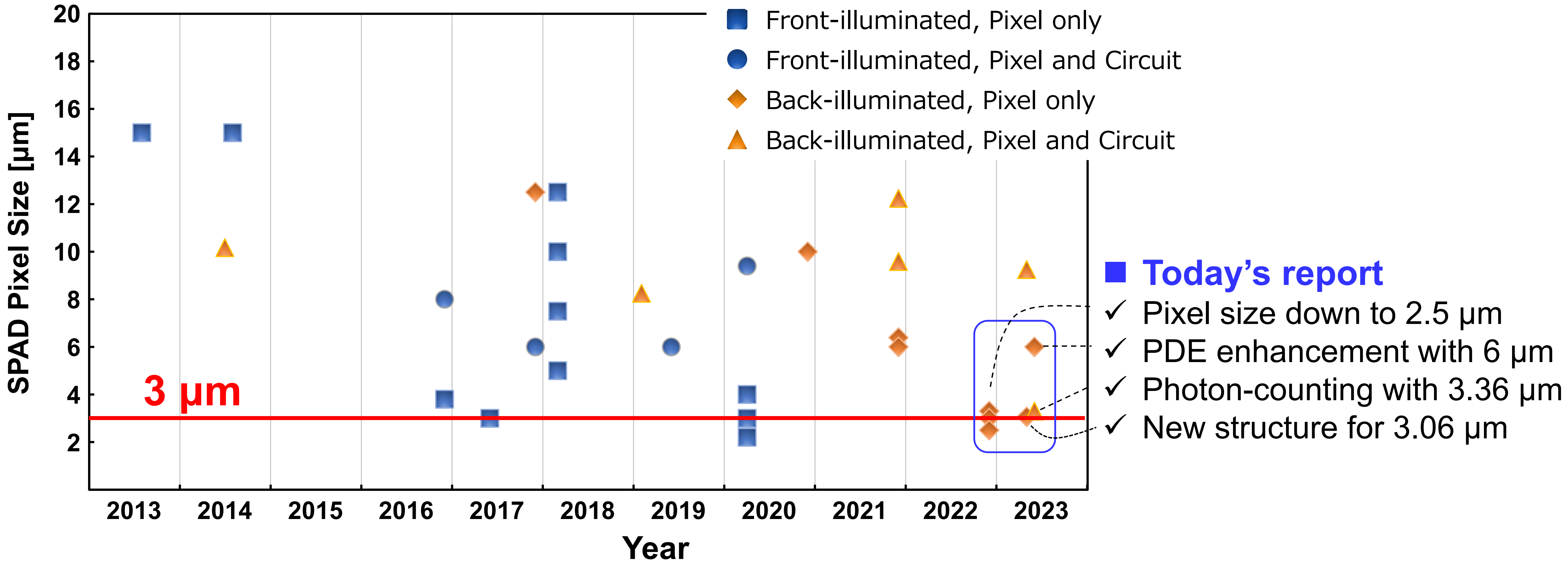
Back-illuminated SPAD stacked with pixel-front-end circuits

[4] J. Ogi *et al.*, ISSCC2021



- Back-illuminated SPAD pixel and 3D stacking of pixel-front-end circuit allows high-sensitivity and small pixel pitch.

Recent advances in the pixel size reduction



- The pixel size has been reduced less than 3 µm
- Near infrared PDE is improved with 6-µm-pitch pixel

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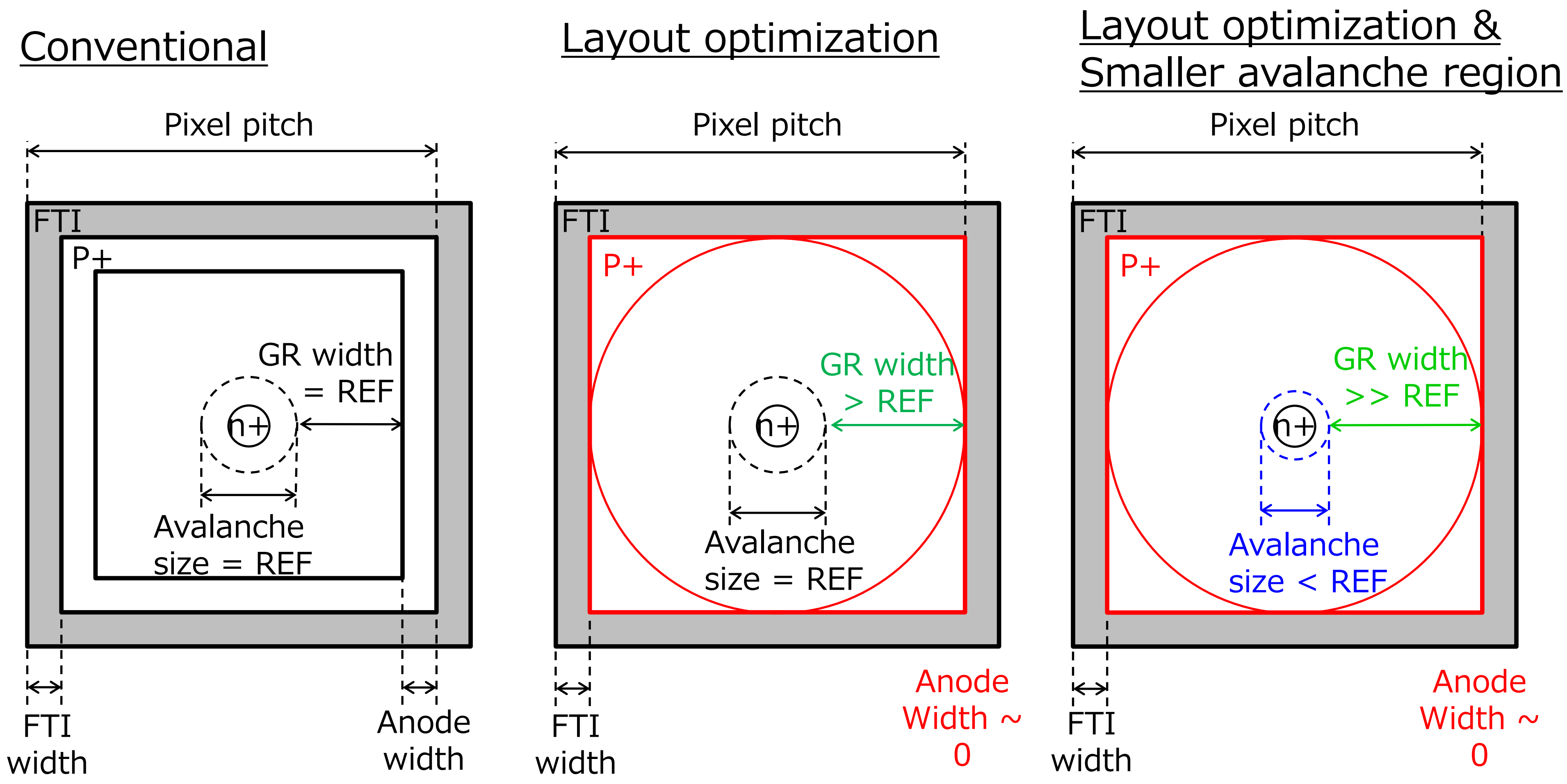
[9] S. Shimada *et al.*, IEDM 2022

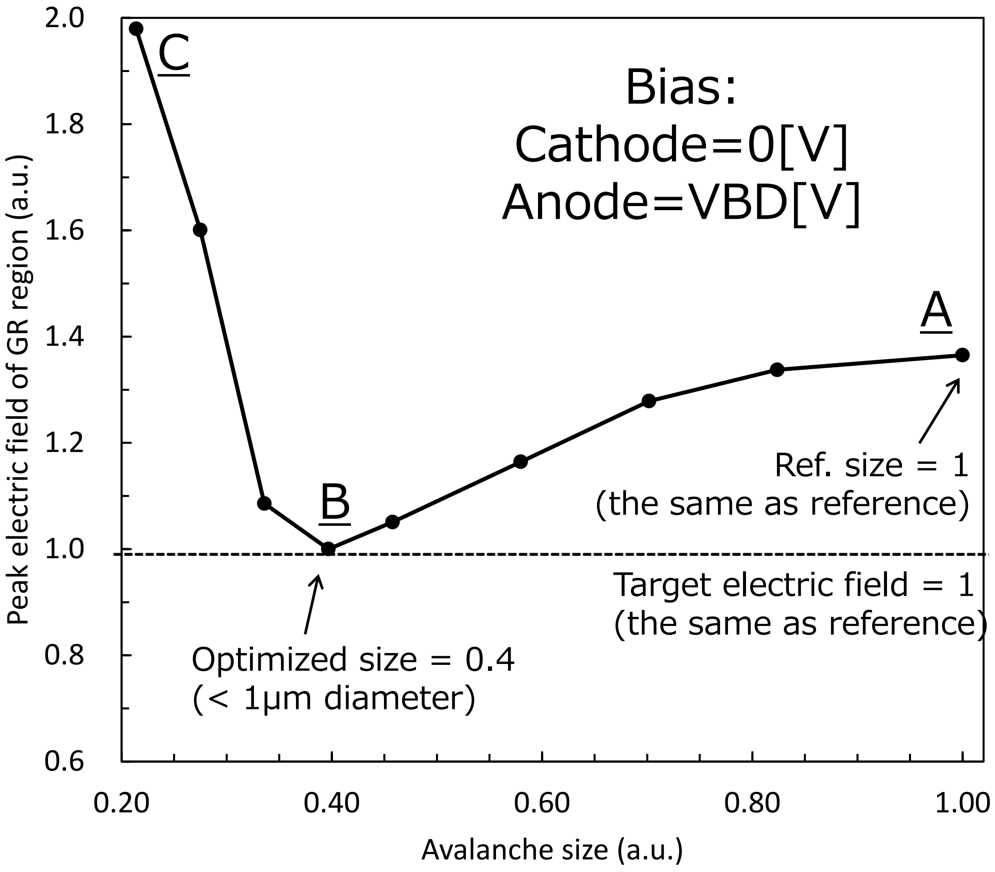
Layout optimization



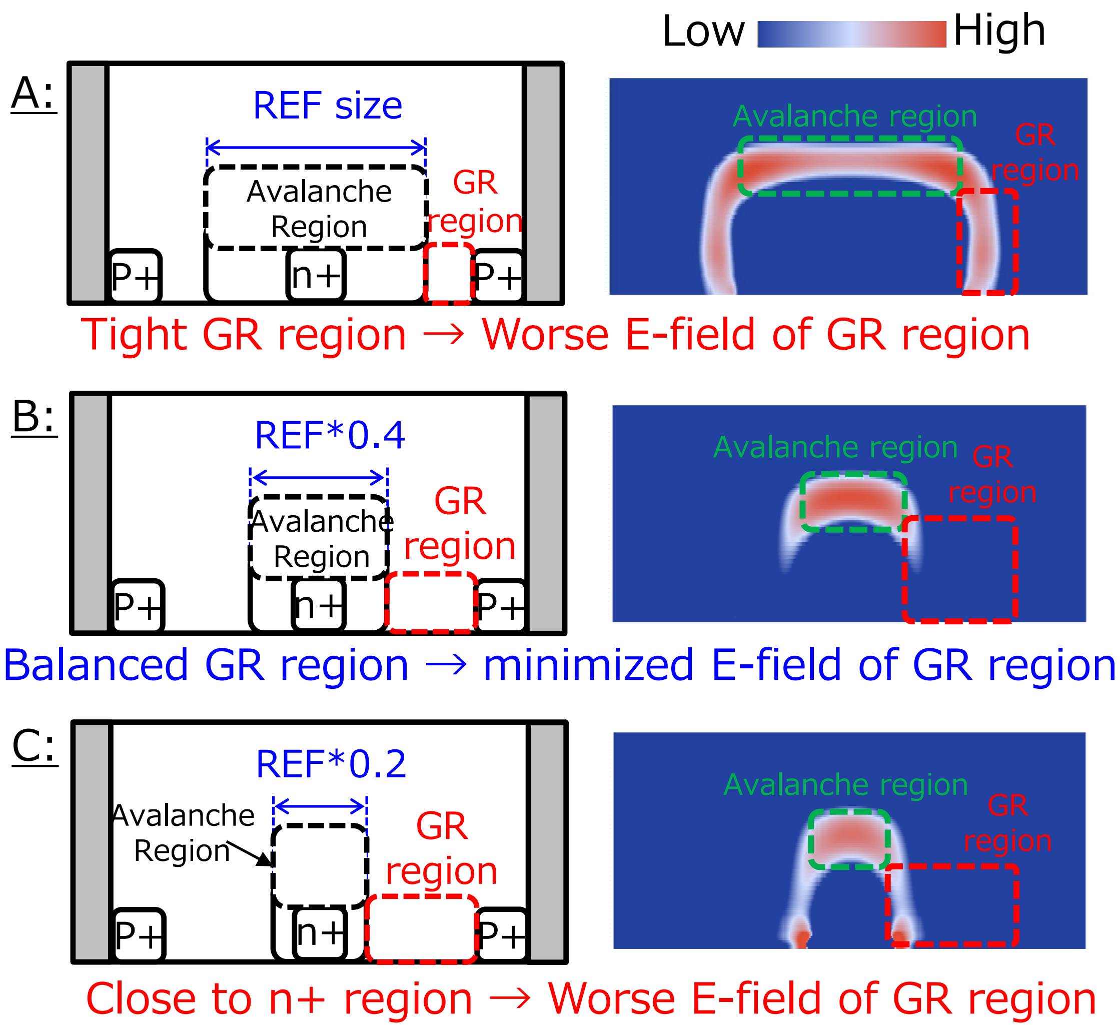
- To prevent premature edge breakdown, we combined layout design optimization and smaller avalanche region to increase the GR width.

The multiplication design

3μm pixel TCAD simulation results

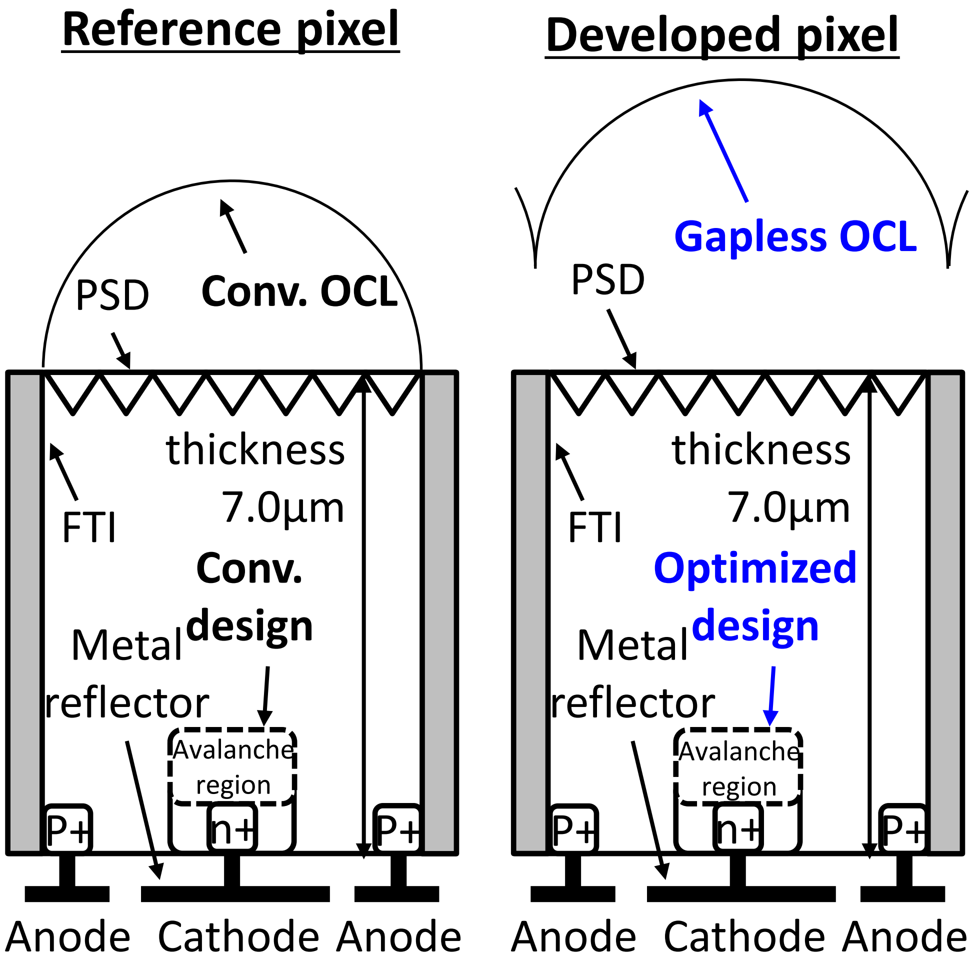


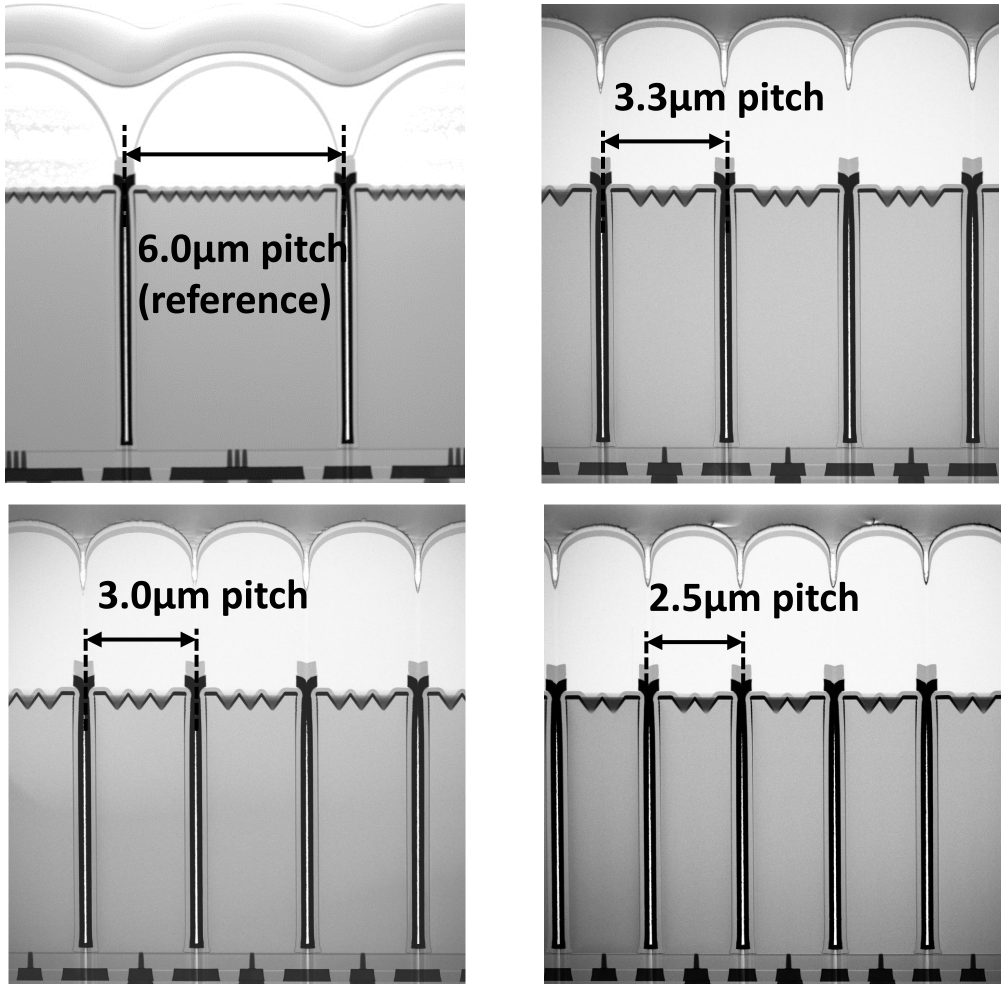
Cross section Image   Electric field (simulation)



- The optimal point B was applied to avoid premature edge breakdown

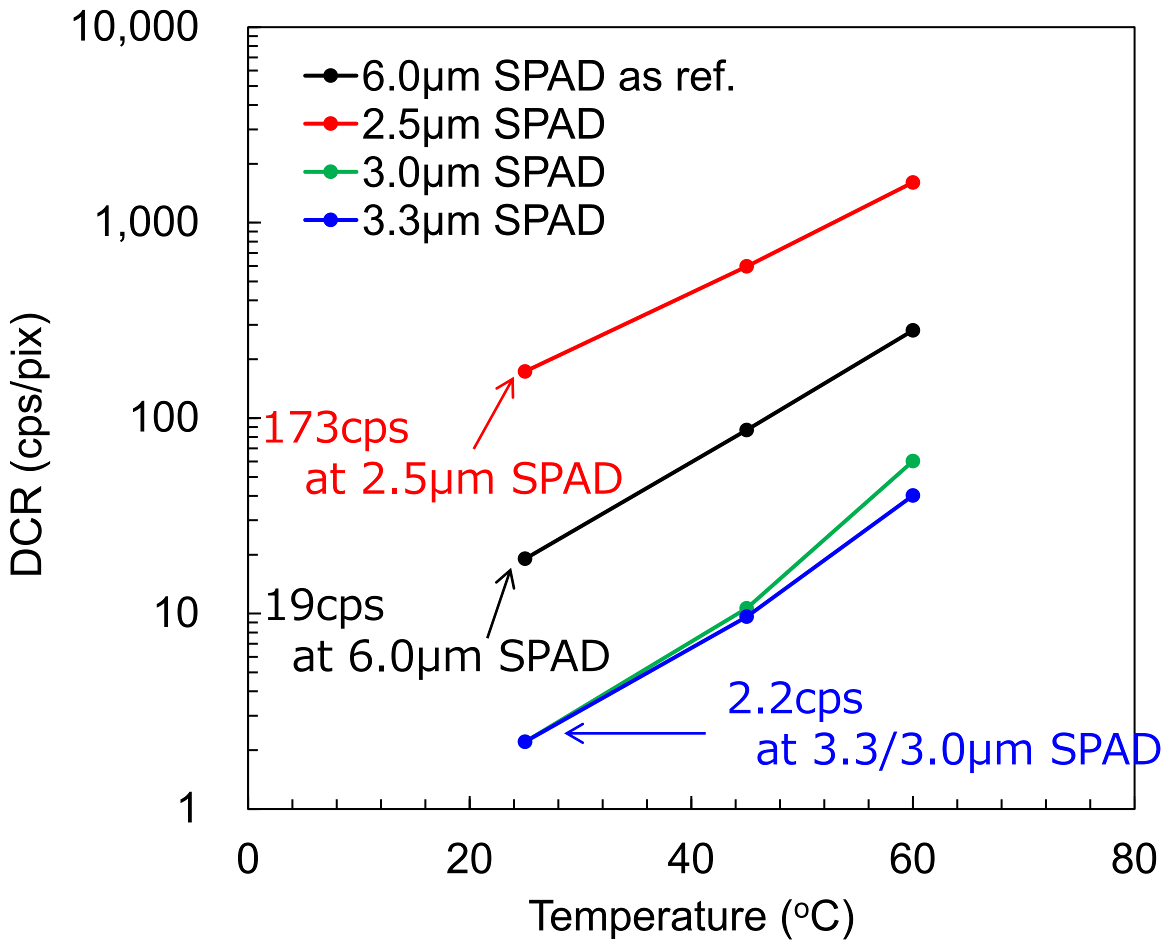
SPAD pixel structures





- Cross-section of the scaled down pixels with optimized avalanche region, and Gapless OCL for PDE enhancement.

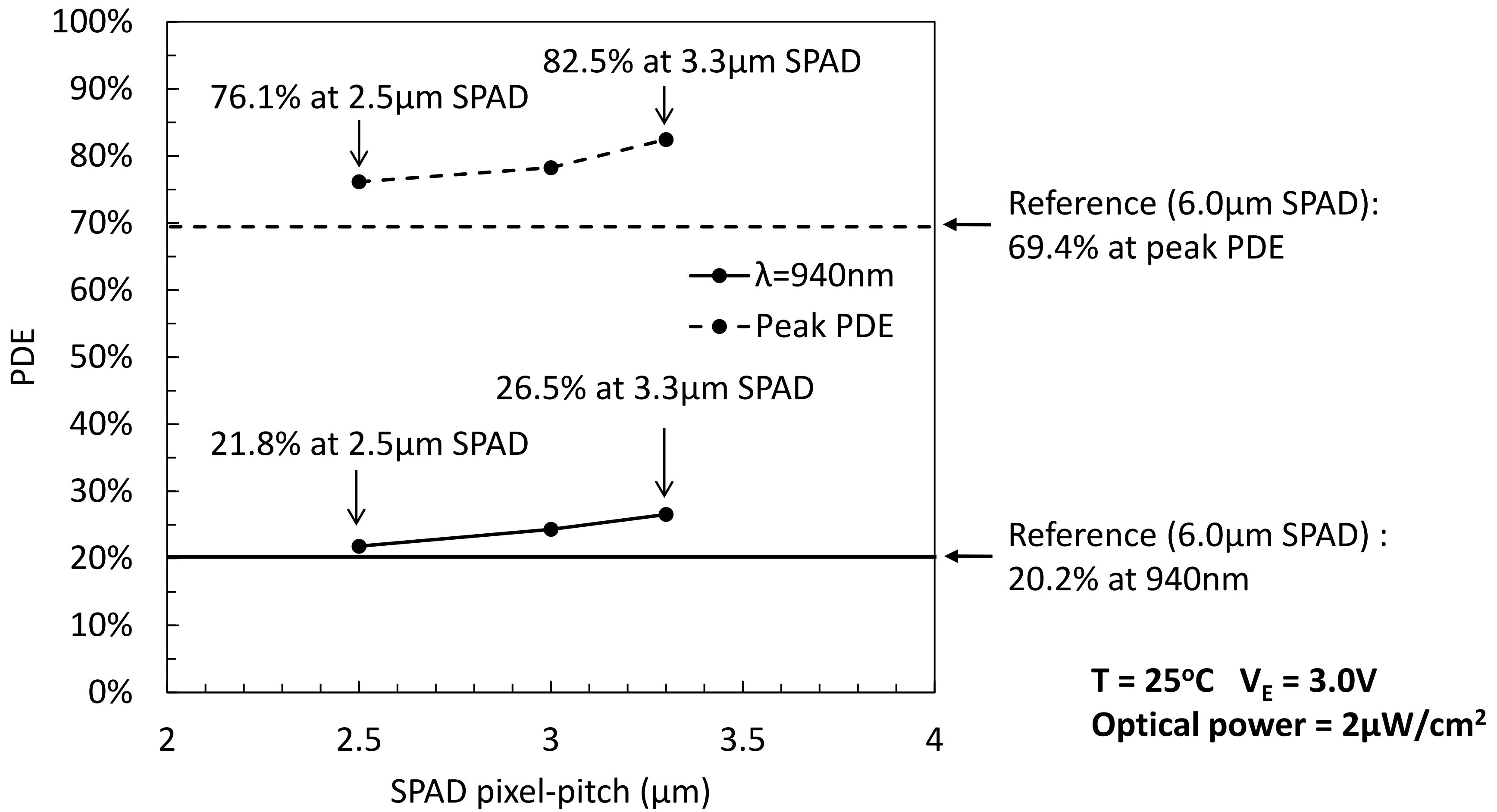
Dark count rate



V_E = 3.0V
Median DCR within die

- 3.3, 3.0μm pixels DCR improvement over the 6μm pixel is attributed to the avalanche region design optimization.

PDE as function of pixel pitch



- The scaled down pixels achieve higher PDE than the 6µm reference in terms of both, NIR and Peak PDE in the visible region.

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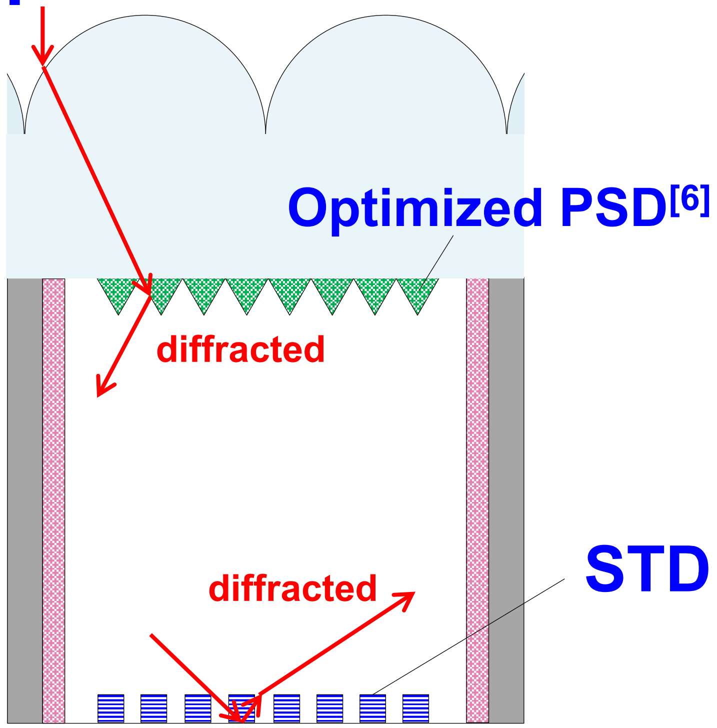
PDE enhancement with dual diffraction structure

1. **pyramid surface for diffraction (PSD) on incident surface**
2. **shallow trench for diffraction (STD) on opposite surface**

PSD + STD } **Dual Diffraction Structure**

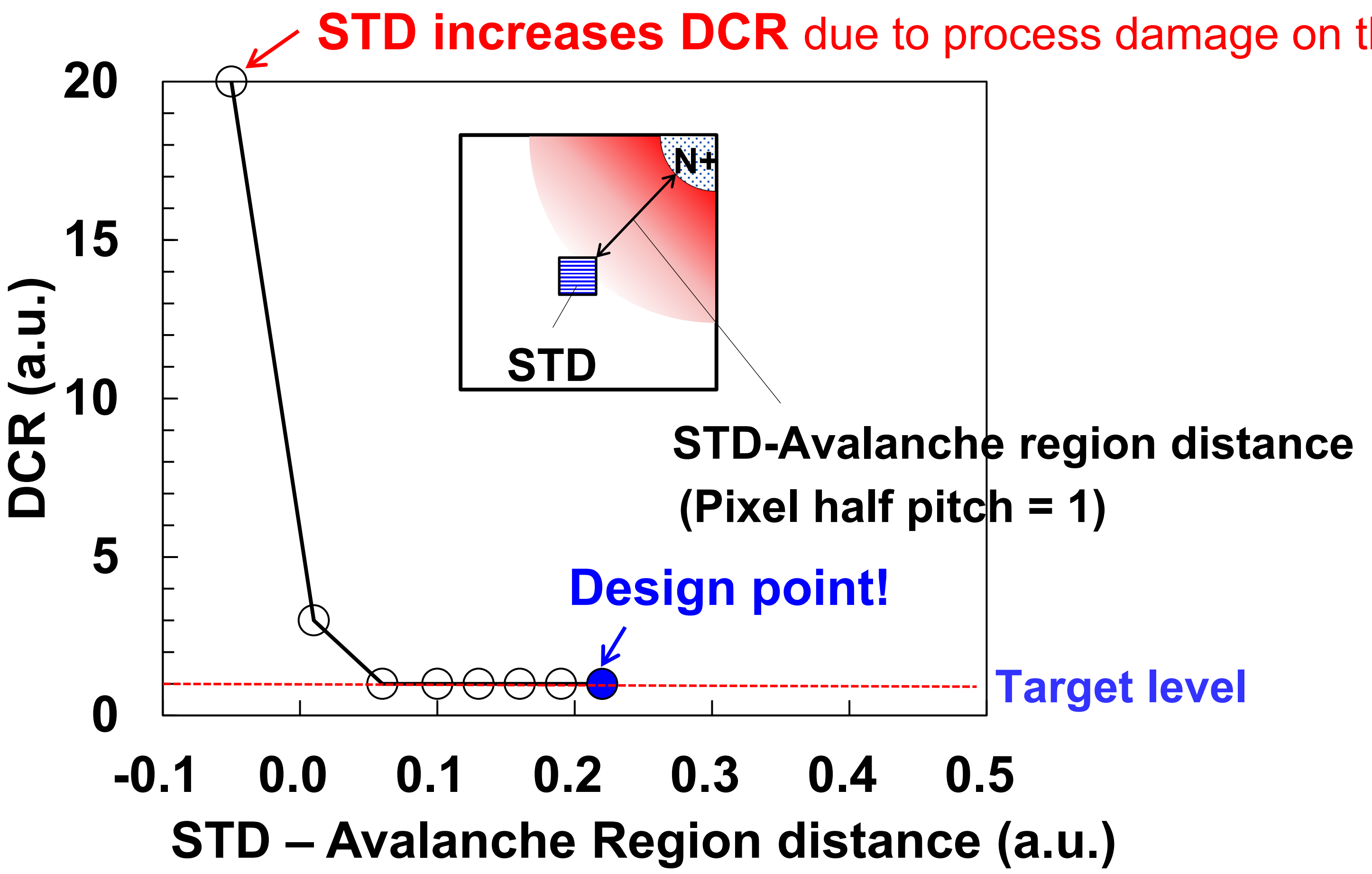
⬇

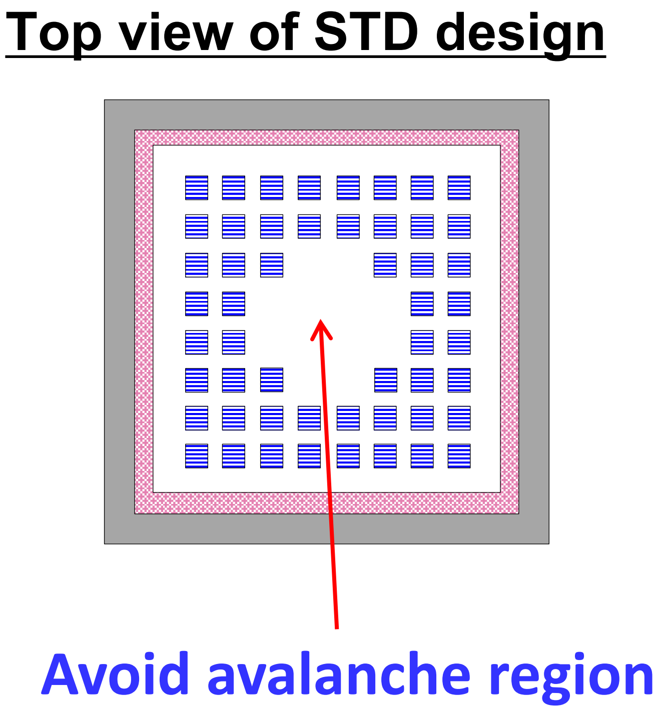
Optical path is longer than PSD only!



- Dual diffraction structure increase optical path in the pixel.

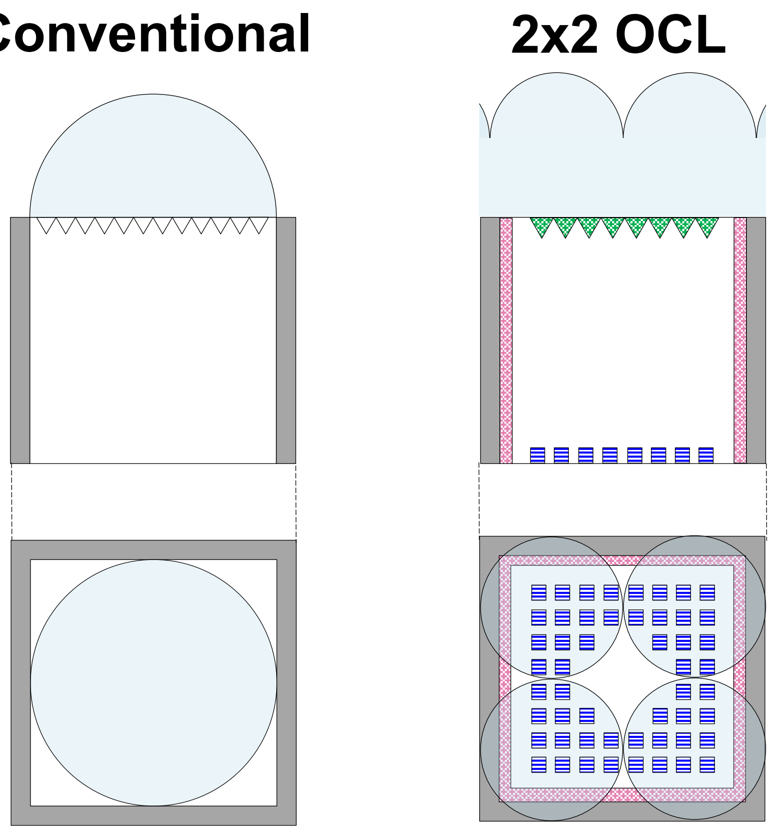
Shallow Trench for Diffraction (STD)

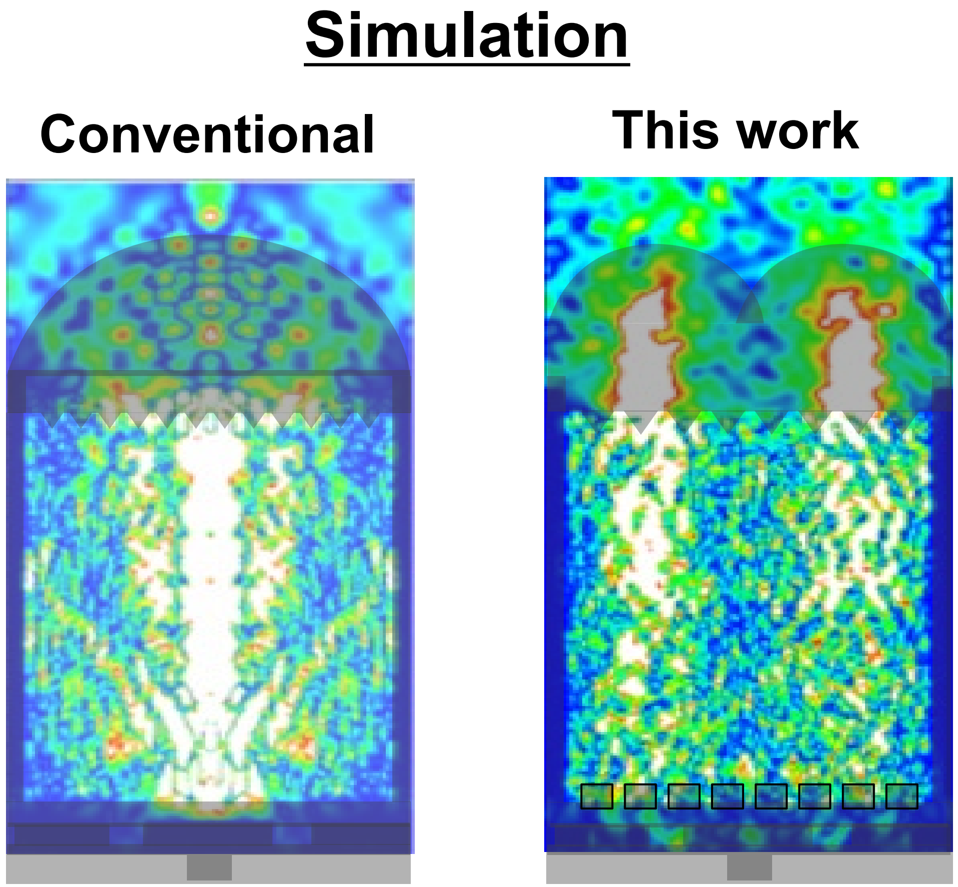




- Shallow trench diffraction is used for the diffraction structure on the front-side of the pixel and the design is optimized to reduce DCR.

2×2 On-Chip Lens

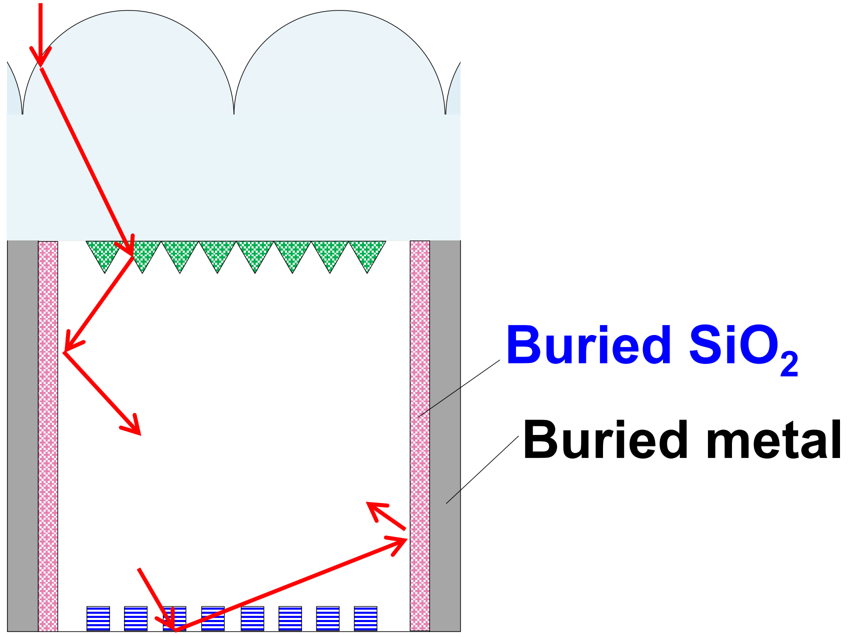


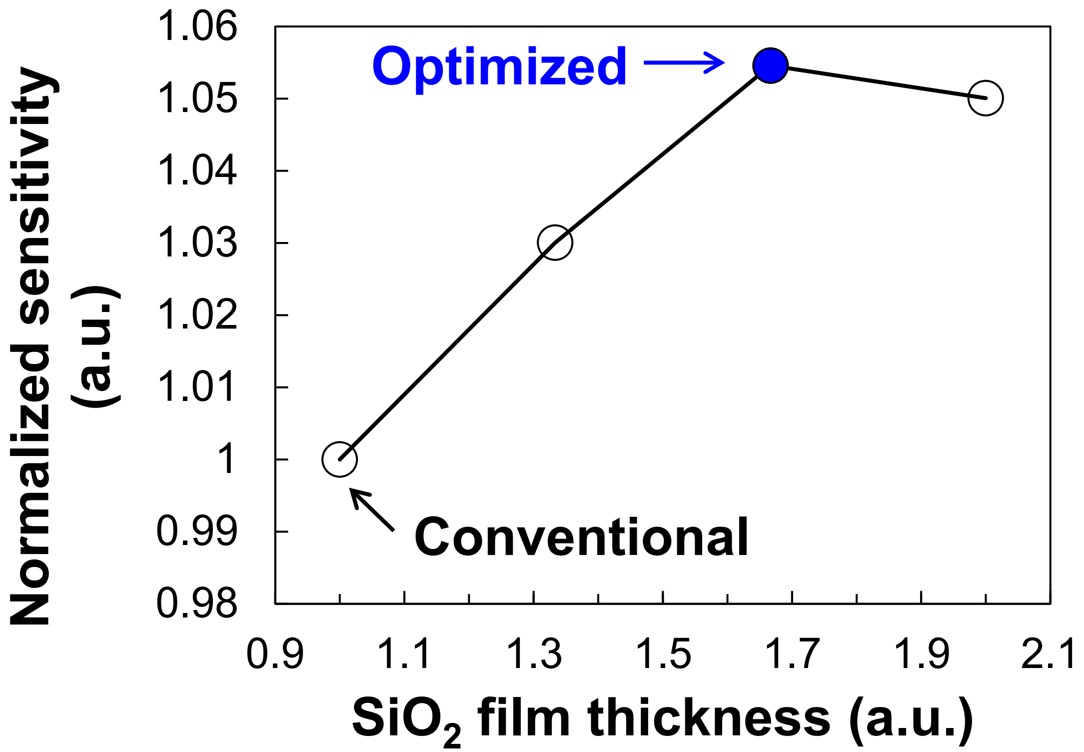


Scattering sufficiently!

- Single OCL cannot focus on the STD.
- 2x2 OCL per pixel is used to increase the scattering effect.

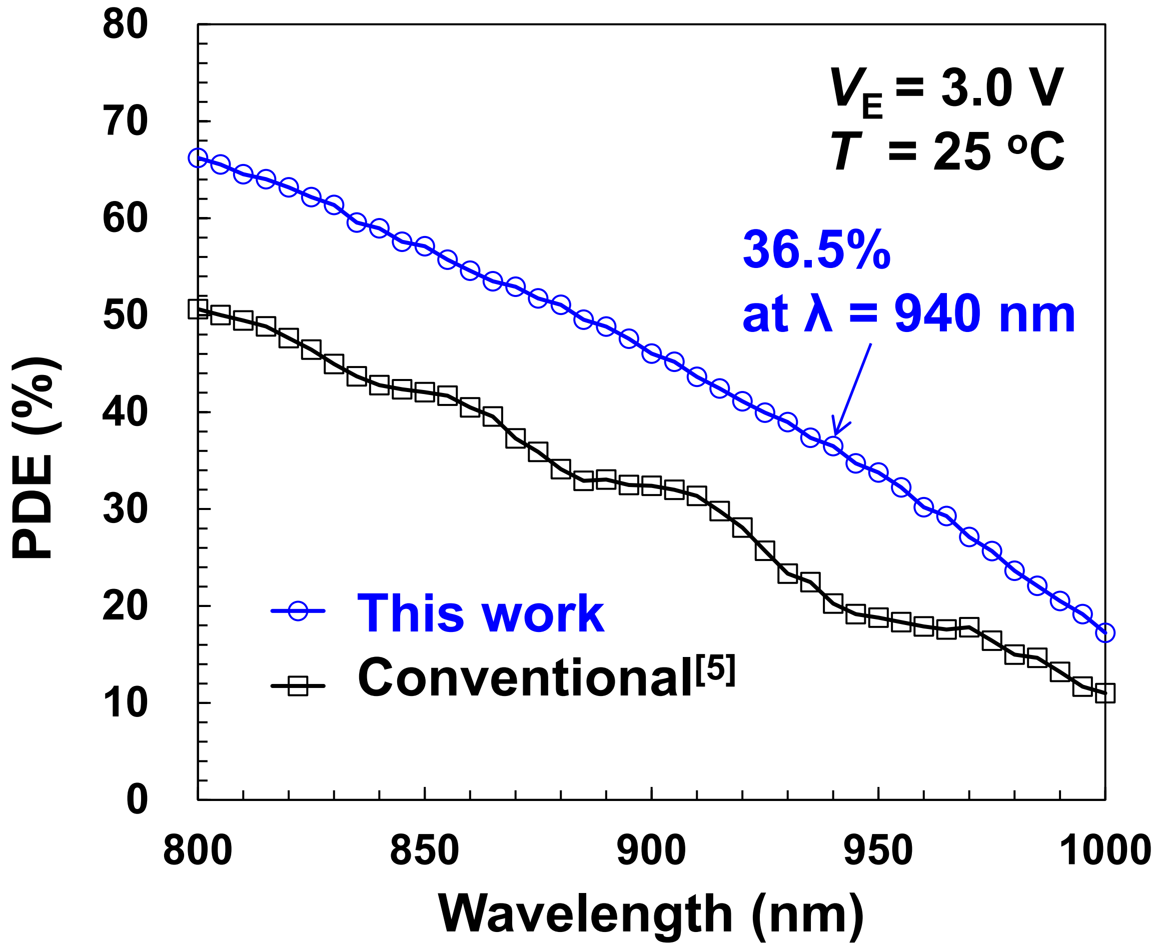
Full Trench Isolation (FTI) optimization





- Metal buried FTI, which blocks cross-talk, degrades PDE due to light absorption on the metal.
- The buried SiO2 thickness is optimized to reduce the absorption.

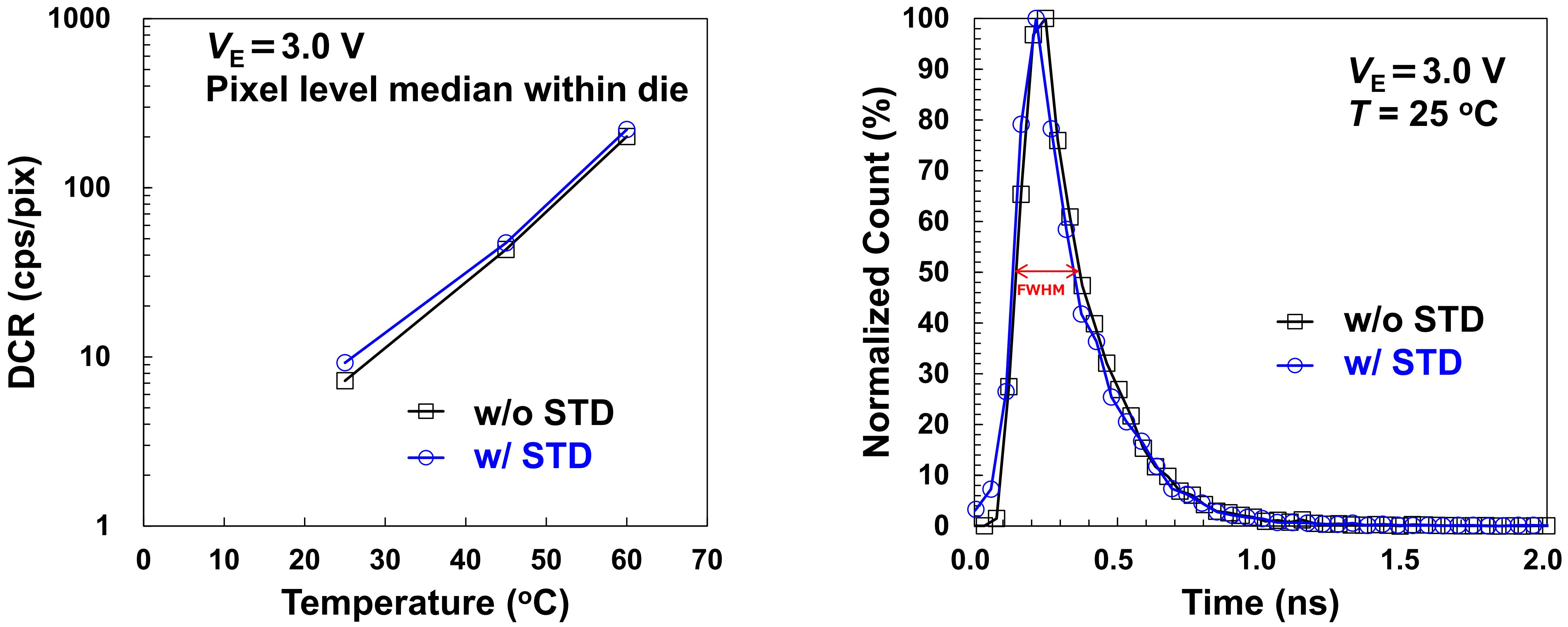
PDE for near infrared



>16 point increase
at λ = 940 nm

- PDE of 36.5 % at 940nm wavelength is achieved.

DCR & Timing jitter



- DCR & timing jitter are maintained with STD.

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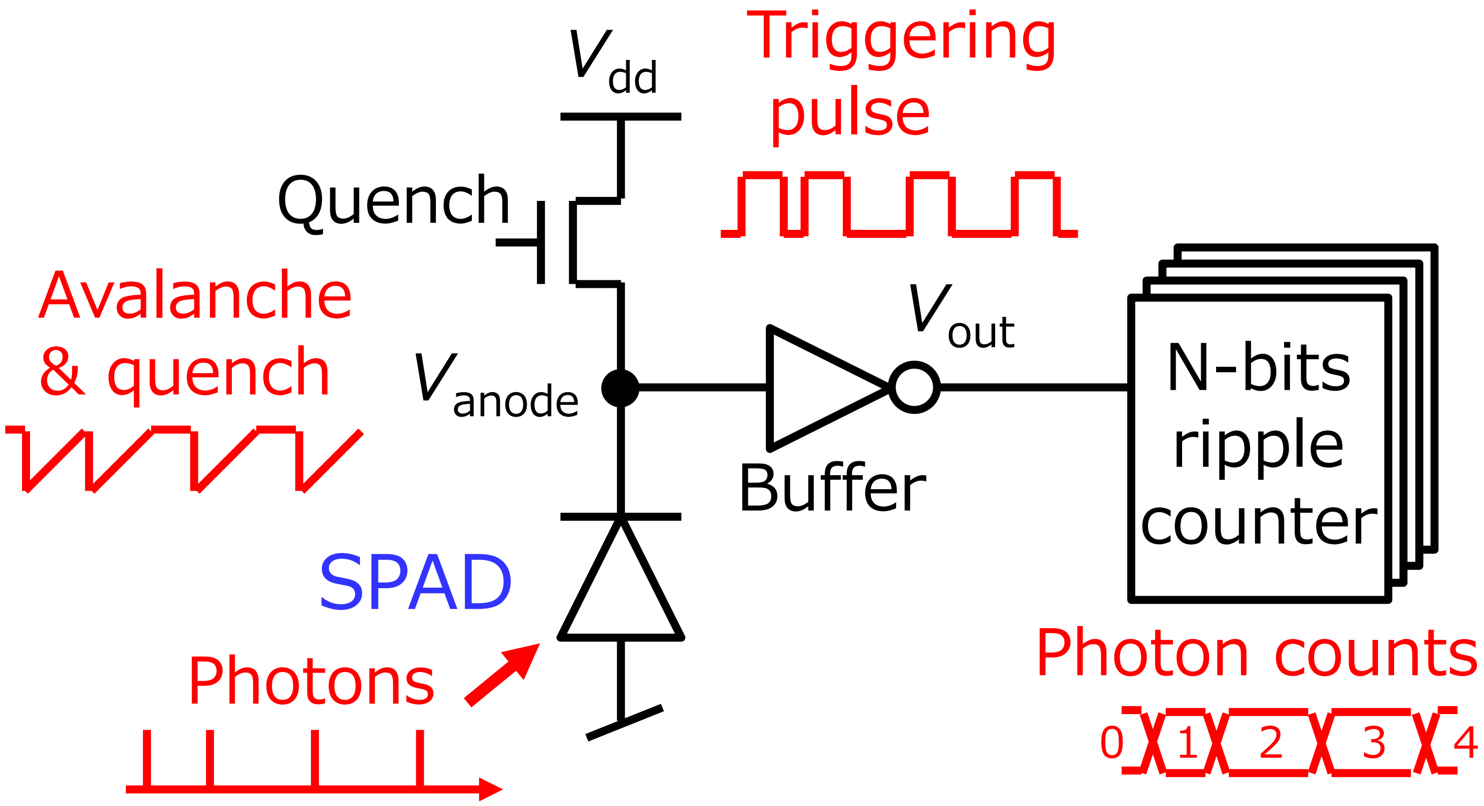
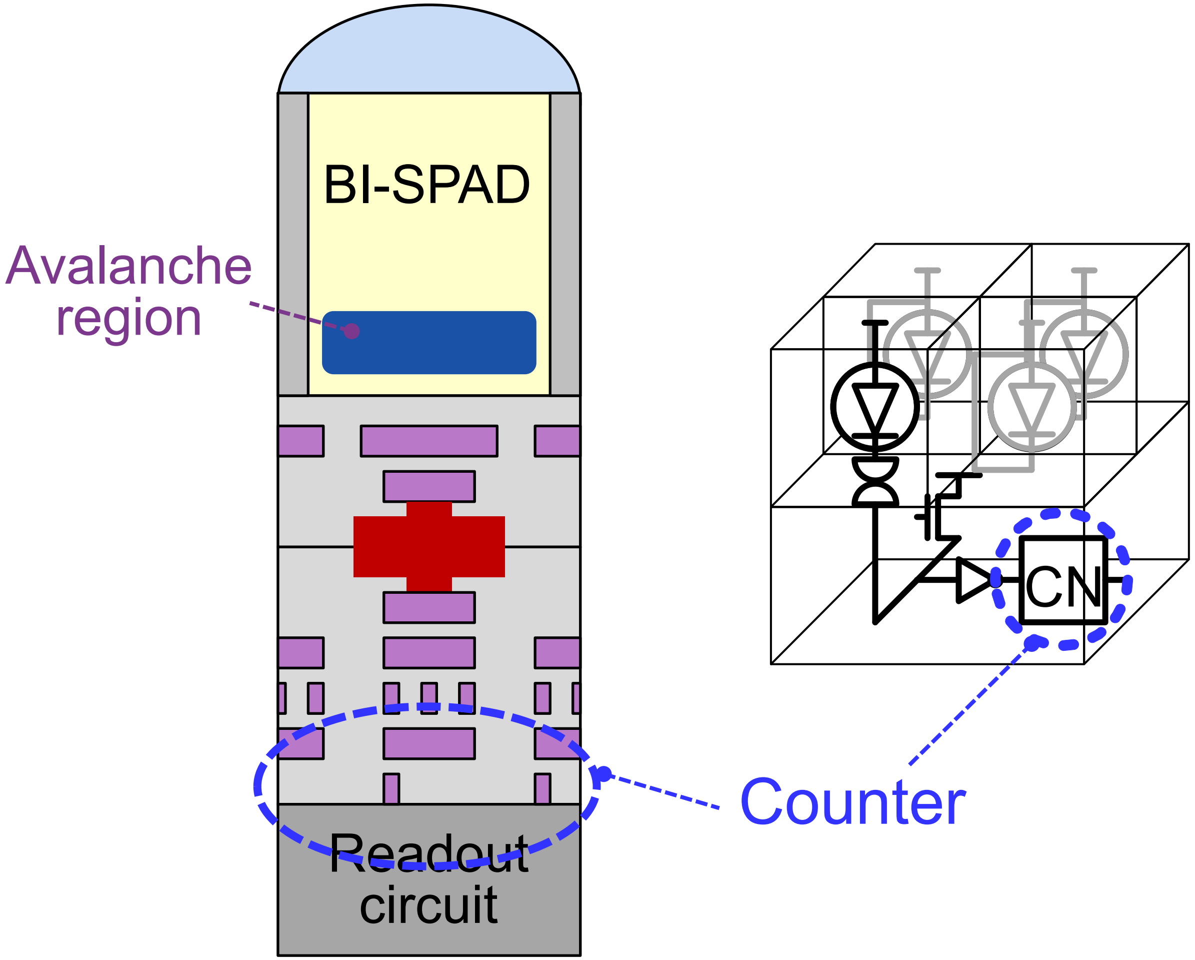
[4] J. Ogi *et al.*, ISSCC2021

Photon counting with SPAD



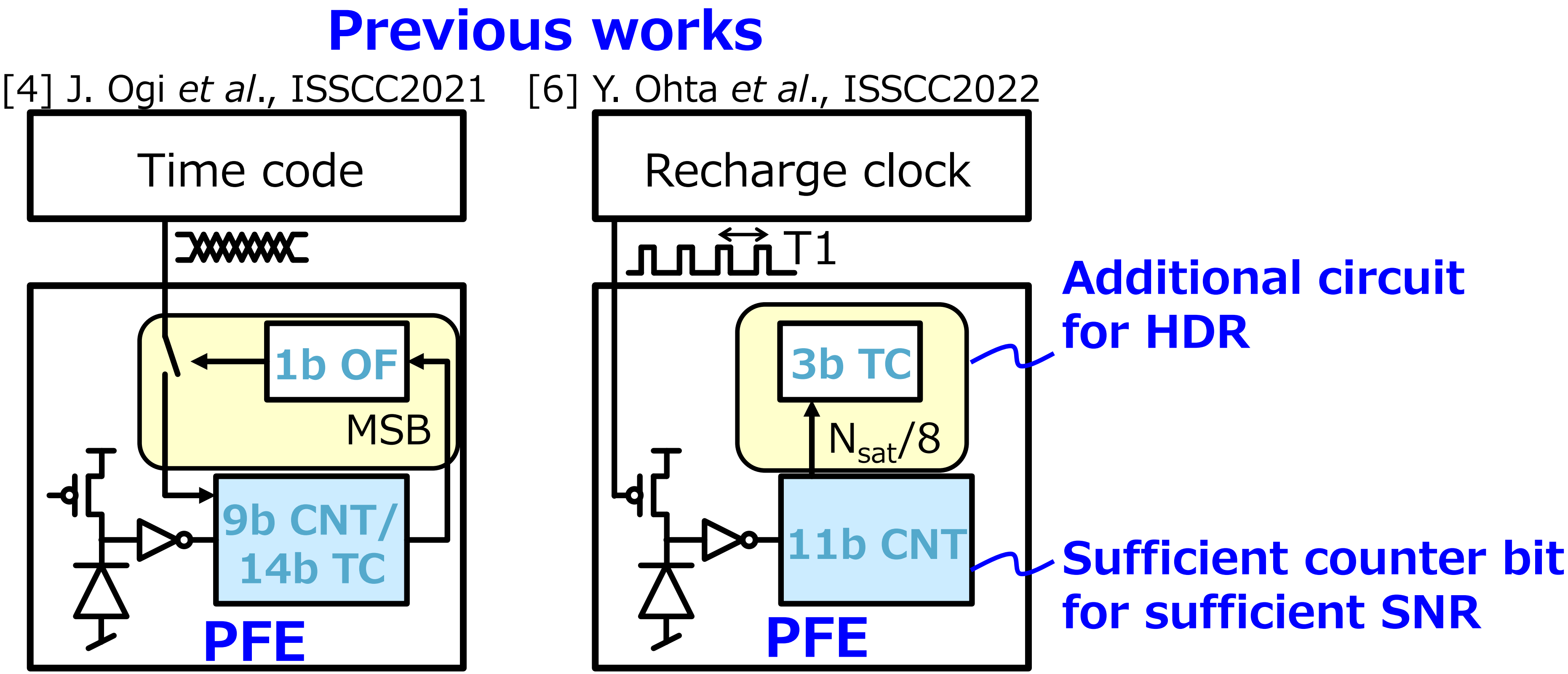
- The photons can be counted using the triggering pulse which is induced by incident photons in the SPAD.

Readout circuit size reduction



- The counter size must be reduced for the pixel pitch shrinking

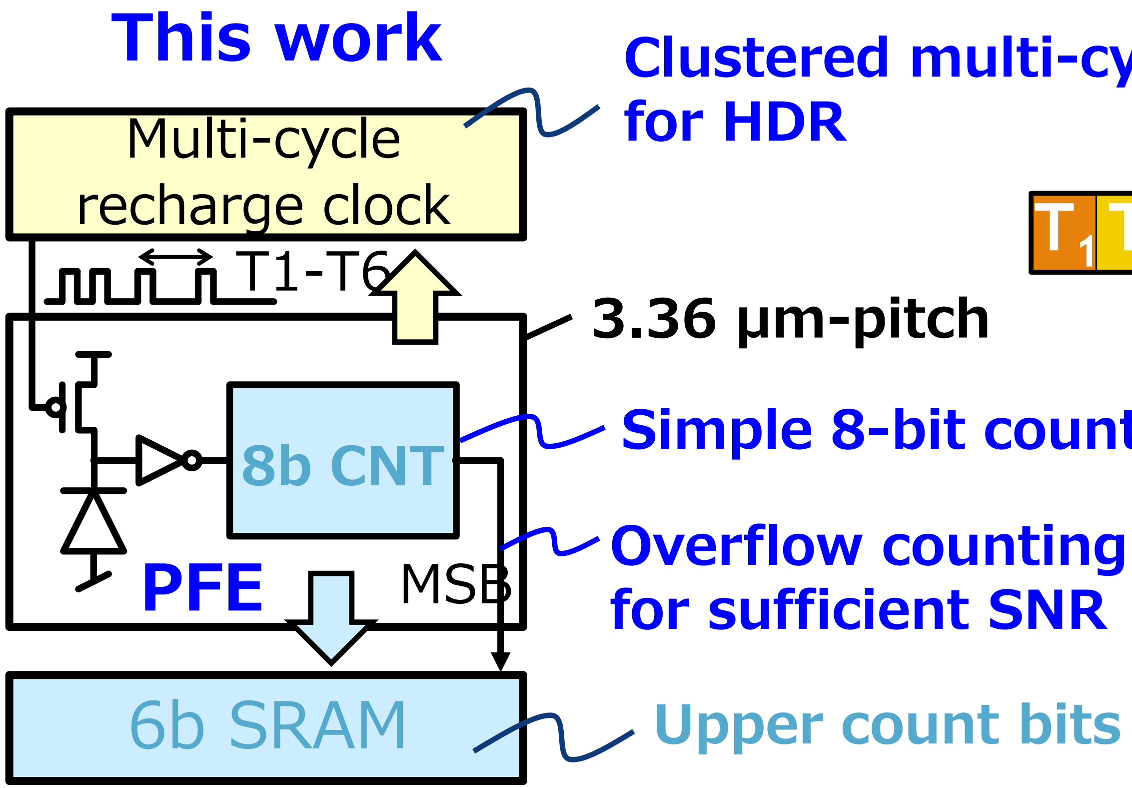
Challenges in reducing pixel size



- Additional circuits for HDR and sufficient counter bits for sufficient SNR are needed in pixel front-end (PFE) circuit.

[11] T. Takatsuka *et al.*, VLSI 2023

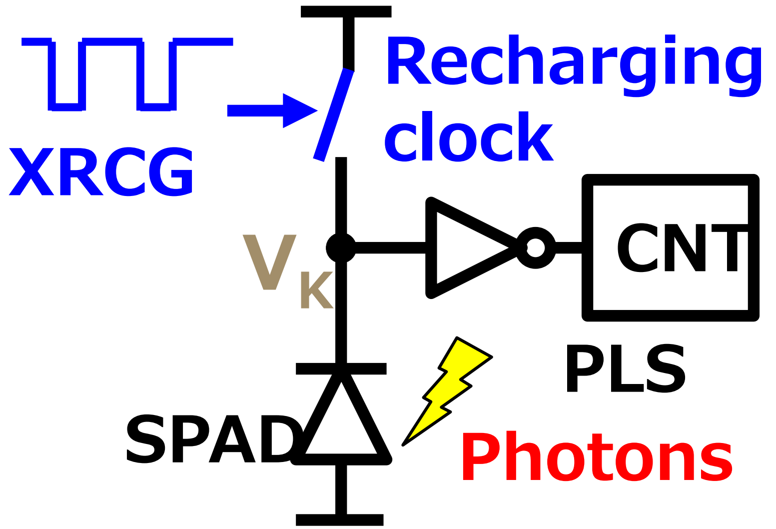
Approach to 3.36 μm-pitch pixel circuit



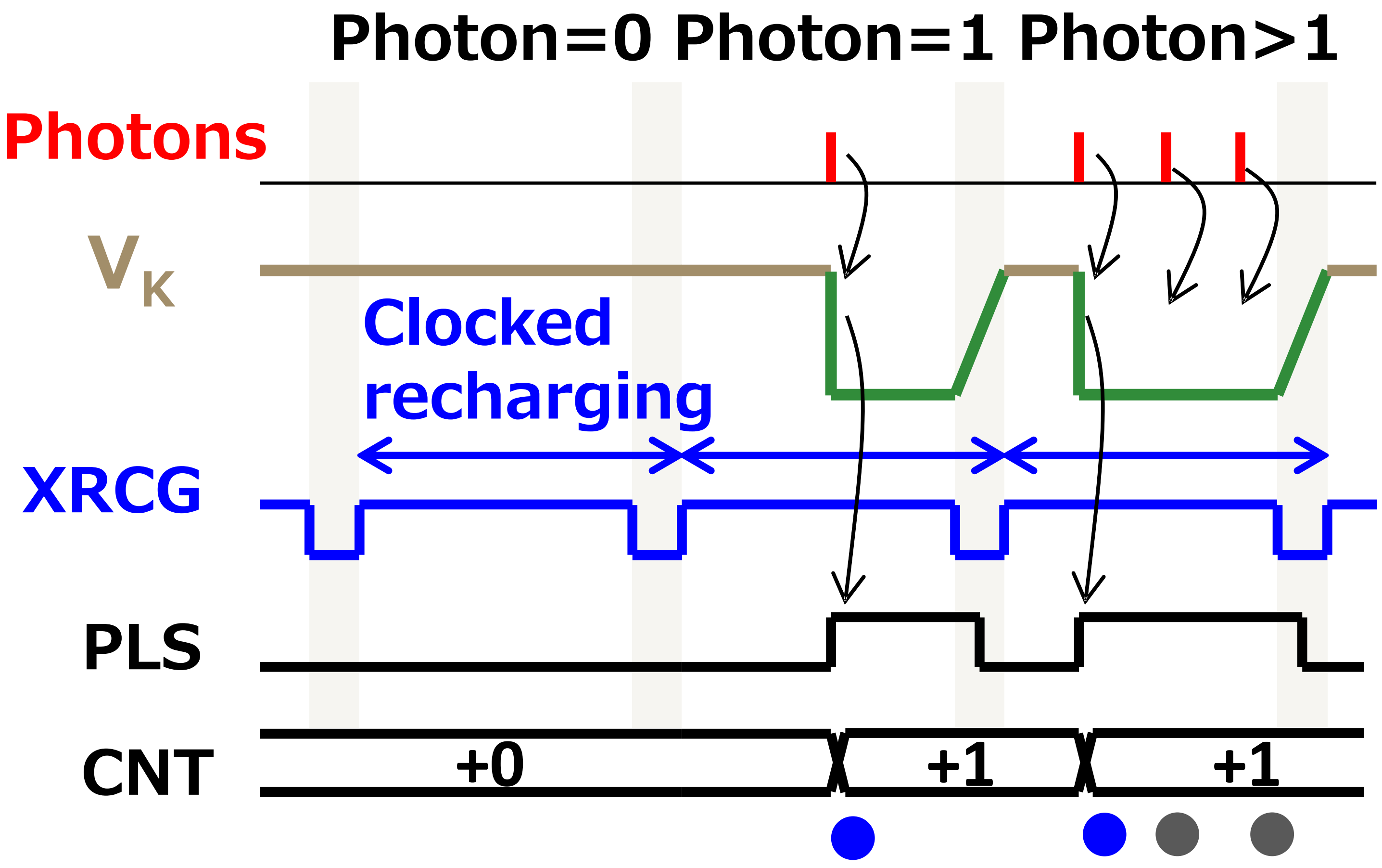
- 3.36 μm-pitch pixel circuits is realized by moving the HDR circuit and upper count bits to outside of the PFE.

[11] T. Takatsuka *et al.*, VLSI 2023

Photon-counting with clocked recharging

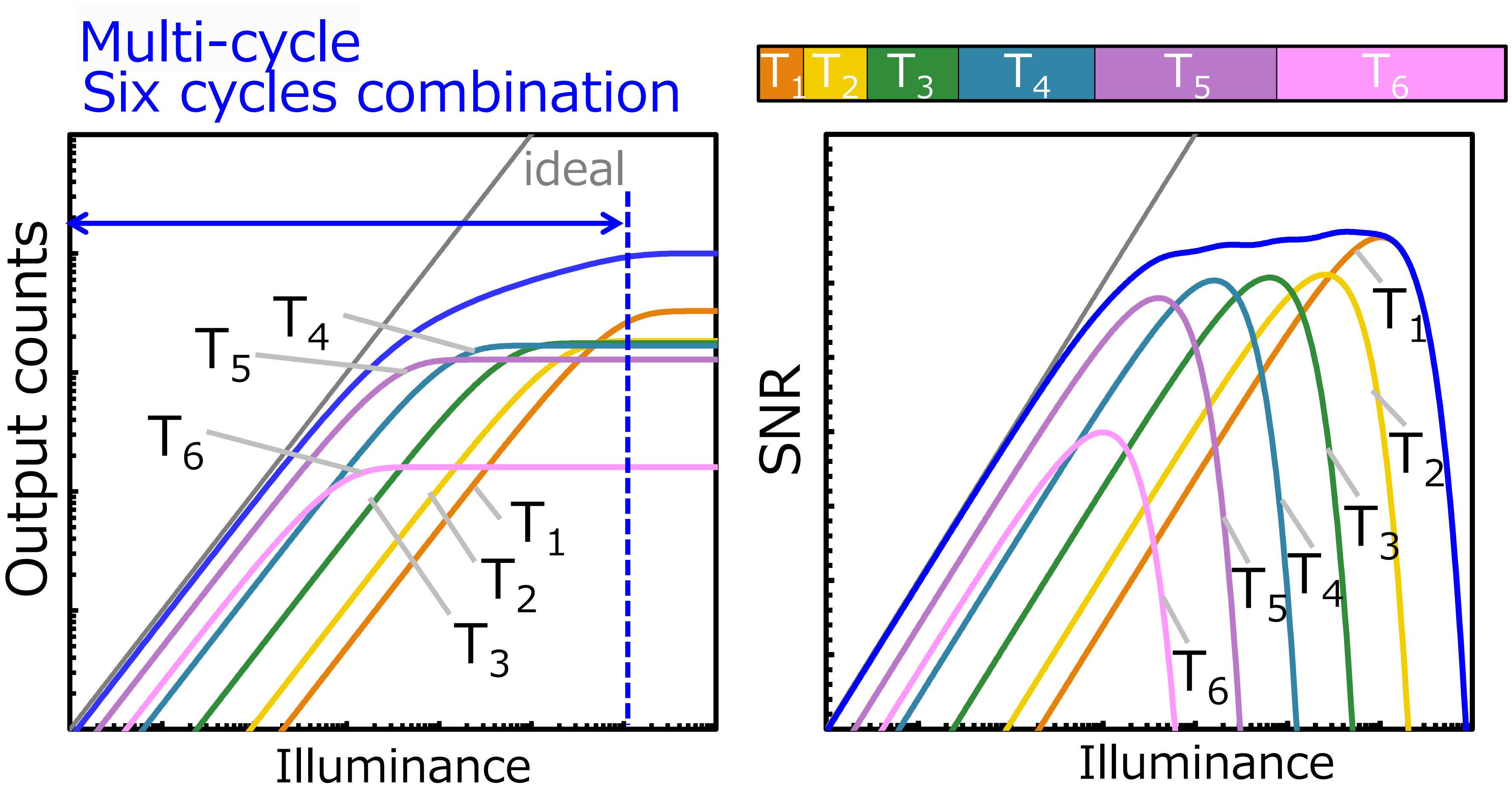


[5] Y. Ota et al., ISSCC 2022



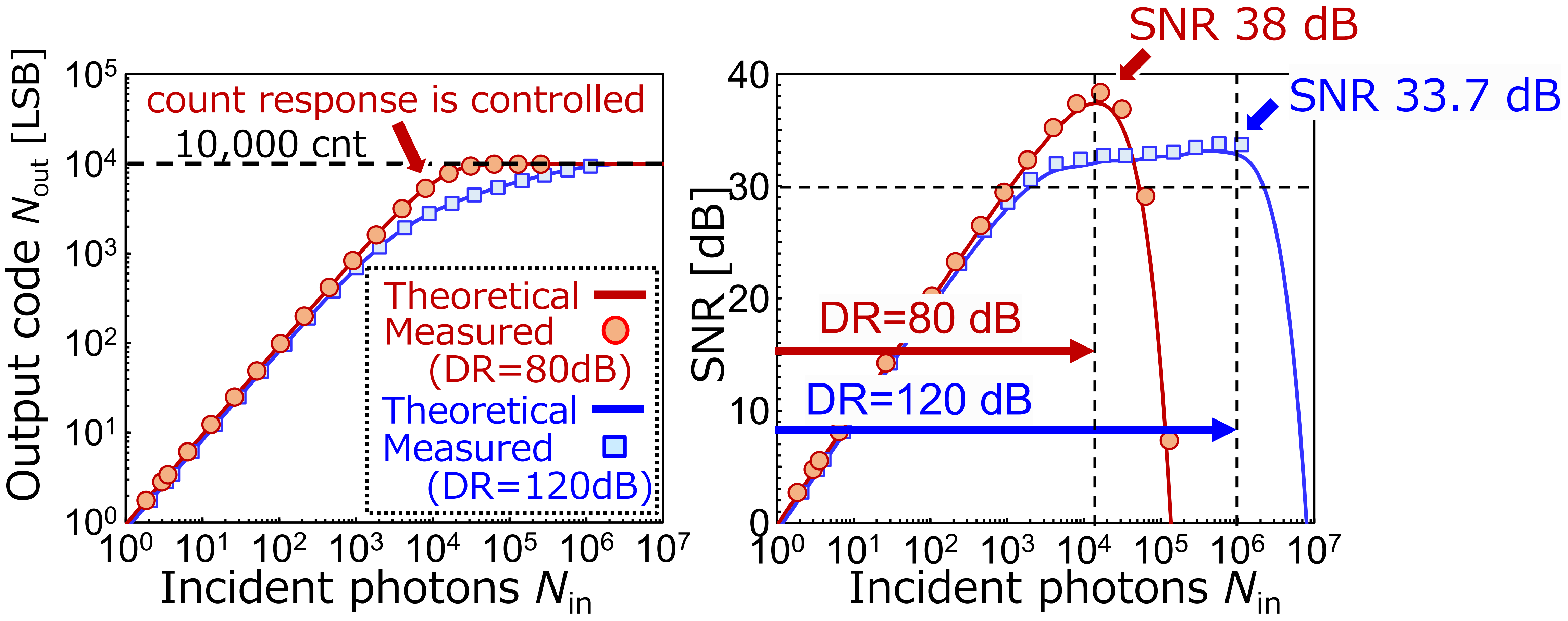
- Number of time slots wherein photons are incident once or more is counted.

Multi-cycle clocked recharging



- Six different time cycles are combined to achieve 120 dB DR and monotonic increase of SNR (no SNR dip)

SNR and DR control



- 120 dB DR is achieved with the multi-cycle clocked recharging.
- The blight-light response can be controlled with the clock setting.

[11] T. Takatsuka *et al.*, VLSI 2023

HDR image capturing

Exposure 1/150 s, Framerate 150 fps

- Global shutter movie with 120 dB DR and 150 fps is demonstrated.

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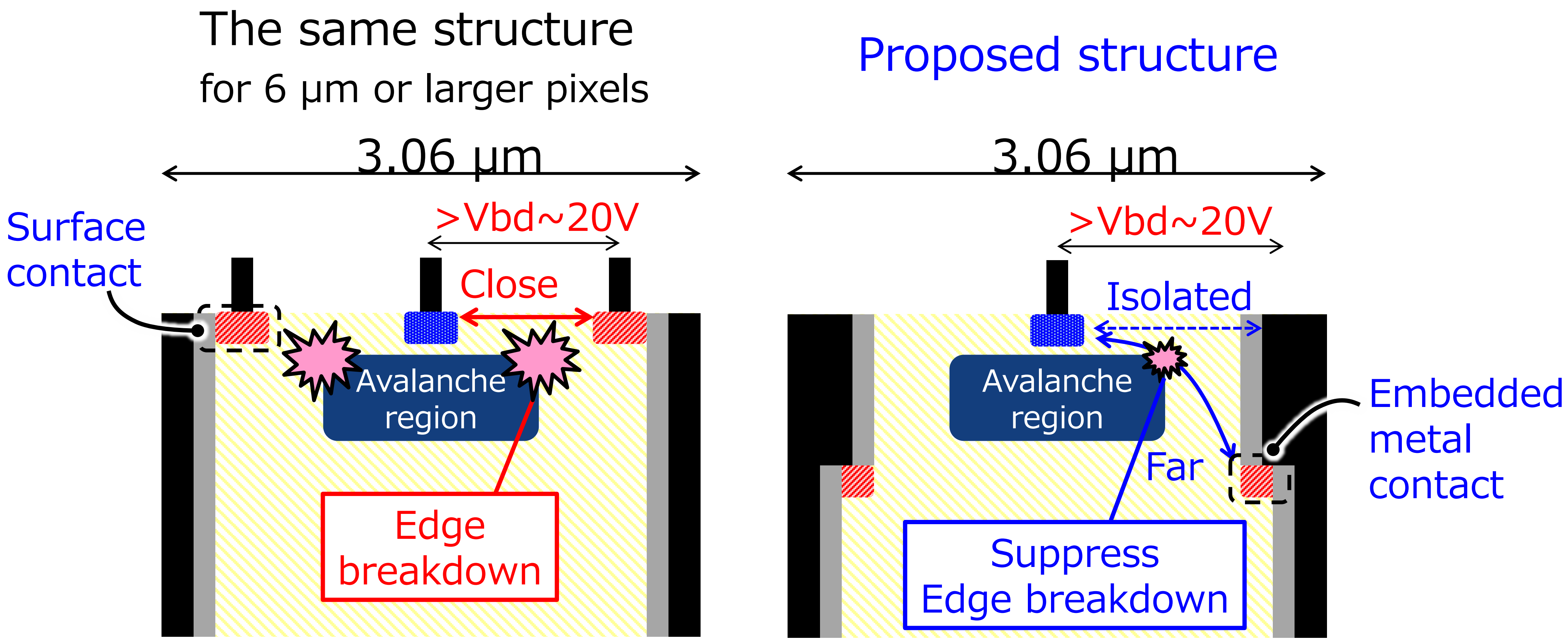
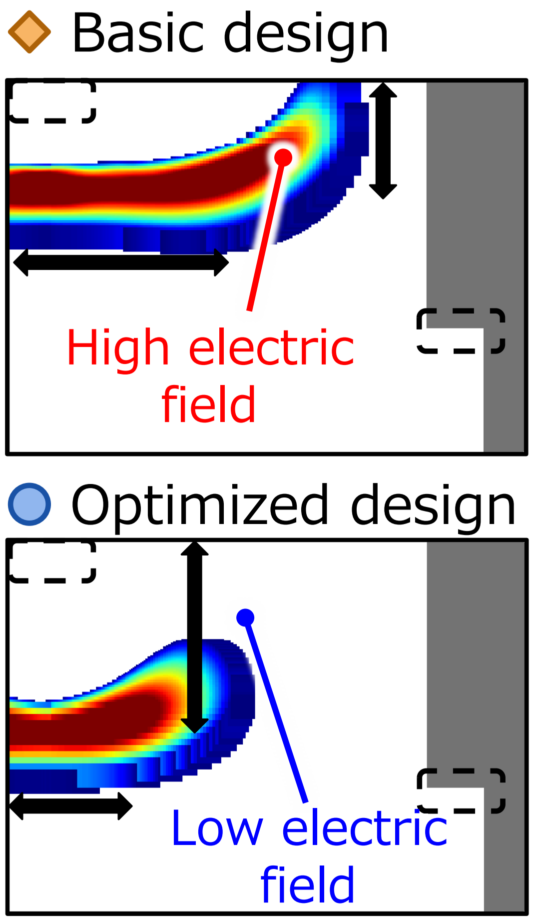
Embedded metal contact structure

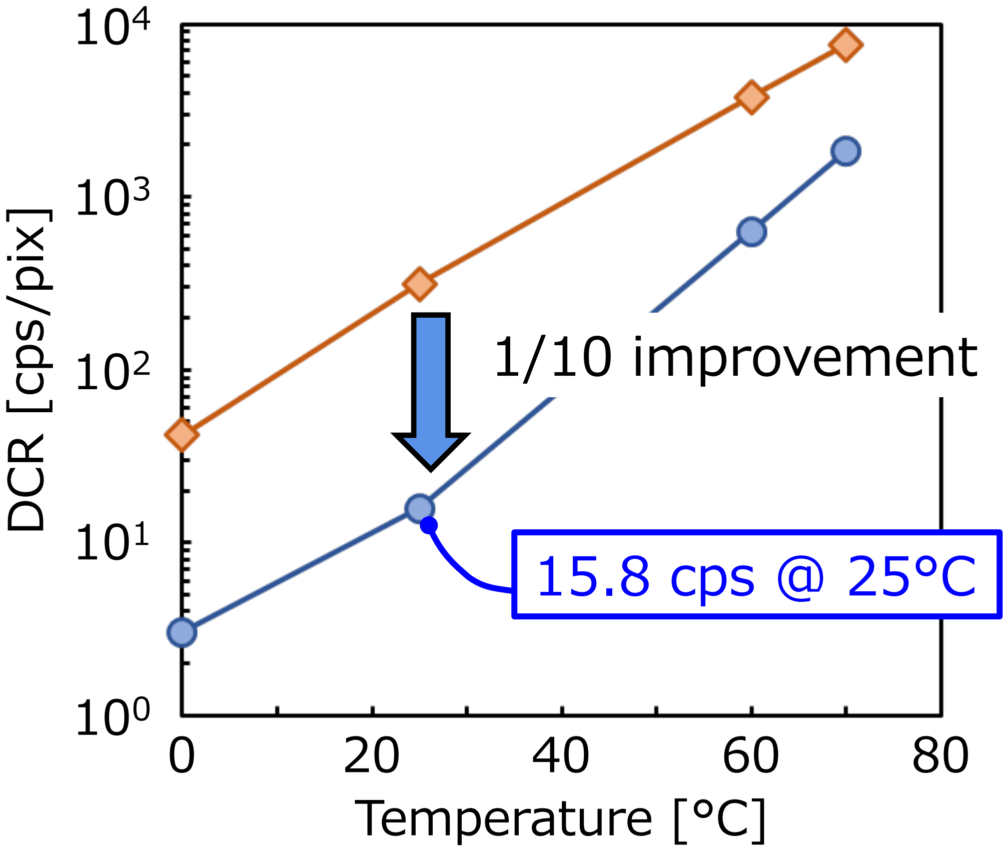


- The embedded metal contact contribute to suppress the edge breakdown by increasing distance b/w anode and cathode region.

[12] J. Ogi *et al.*, IISW 2023

The dark count rate

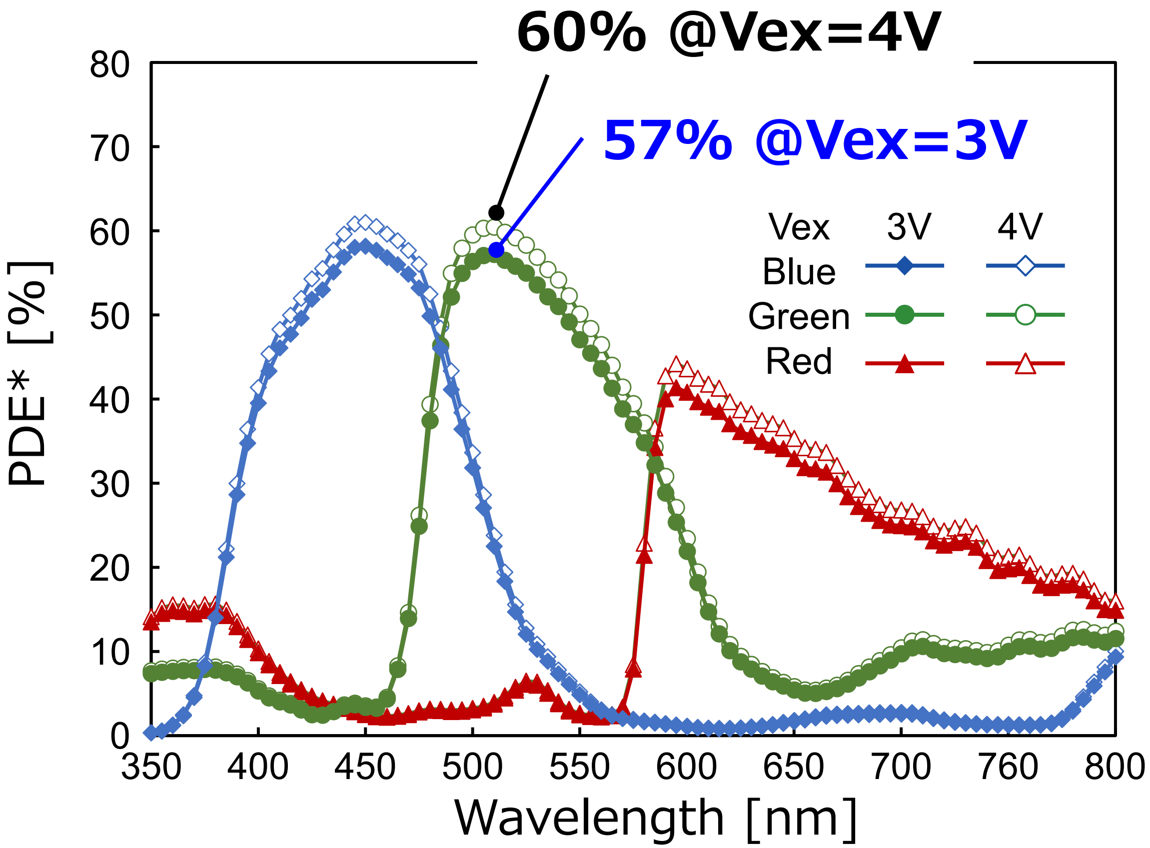




- DCR is successfully reduced with the embedded metal contact and the optimized design to decrease the electric field on the pixel edge.

[12] J. Ogi *et al.*, IISW 2023

The photon detection efficiency



Measured at 25 °C

*Photon detection rate to incident photons on the whole pixel area (3.06 μm□)

- The PDE is 57% even with the small pixel size because of the optimized potential slope for the electron transfer.

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Pixel size and performances.

	Unit	IEDM 2016 [13]	IISW 2017 [14]	JSTQE. 2018 [15]	ISSCC 2019 [2]	Optics 2020 [16]	IEDM 2021 [17]	IISW 2023 [18]	IEDM 2020 [7]	IEDM 2021 [8]	IEDM 2022 [9]		VLSI 2023 [10]	IISW 2023 [12]
Pixel pitch	µm	7.83	3	5	9.2	4	6.39	10.17	10	6	**3.3**	**2.5**	**6.0**	**3.06**
V_{bd}	V	12	15.8	N/D	28.5	22.1	30	18.6	20	22	19	18	22	20.9
V_{ex}	V	3	1.2	5.8*3	2.5	6	2.5	3.5	3.0	3	3	3	3.0	3
Peak PDE	%	11.6	6*3	12*2*3	23	14.2	69.4	34.4*2*3	53.5*1	69.4*1	**82.5**	**76.1**	**88.4**	**57**
PDE at 940nm	%	3.2	~1	N/D	N/D	N/D	24.4	22	14.2	20.2	22.5	20.4	**36.5**	N/D
DCR @25°C	cps	10974	1343	17.3*3	20.3	2.5	1.8	8.6*3	3	19	**2.2**	**173**	**10**	**15.8**
Jitter FWHM	ps	205	185	N/D	N/D	72	100	103	172	137	196	214	209	N/D
Cross-talk	%	N/D	<0.2*4	4.9*3	N/D	3.57	N/D	N/D	N/D	0.5	0.85	1.0	1.12	<0.4

- 3 - 6 µm pitch SPAD pixels have been reported with enhancement of PDE and maintaining low DCR.

Photon-counting image sensors

	Unit	Sensors2018 [19]	ISSCC2019 [2]	Optica2020 [20]	ISSCC2022 [6]	ISSCC2021 [4]	VLSI2023 [11]
Pixel pitch	μm	8.25	36.8 x 9.2	9.4	9.585	12.24	**3.36**
Pixel array	Pix	96 × 40	64 × 256	1024 × 1000	960 × 960	264 × 160	748 × 448
CMOS Technology	Nm	40	Stacked 90 / 40	180	Stacked 90 / 40	Stacked 90 / 40	Stacked 90 / 22
In-pixel counter	Bit	12	28	1	11+3bit latch	9	8
Max. frame rate	fps	60	30	0.45	90	250	150
Dynamic range	dB	109	129	108.1	143	124	120
SNR Max.	dB	~40	>40	30.5	33	40	33.7
SNR dipped	-	30	No dip	29.5	24	No dip	No dip
Motion artifact Suppression	N/A	No	Yes	No	No	Yes	Yes

- 3.36 μm pitch photon-counting image sensor has been reported with competitive characteristics.

Summary

- The SPAD pixel size has been reduced to improve the SPAD sensors performances.
- Back-illuminated and stacked technology are further reducing the pixel size.

- 3 - 6 μm pitch SPAD pixels have been reported with enhancement of PDE and maintaining low DCR.
- 940 nm PDE is improved to 36.5 % with 6-μm-pitch pixel
- 3.36 μm pitch photon-counting image sensor has been reported with competitive characteristics.

- SPAD pixel size is expected to be reduced further in the near future.

References

[1] A. R. Ximenes *et al*., ISSCC 2018.
[2] R. K. Henderson *et al*., ISSCC 2019.
[3] O. Kumagai *et al*., ISSCC 2021.
[4] J. Ogi *et al.,* ISSCC 2021.
[5] J. Ogi *et al.,* IISW 2021.
[6] Y. Ohta *et al.,* ISSCC 2022.
[7] K. Ito *et al.,* IEDM 2020.
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