Rethinking boundaries: 3D integration & advanced packaging as performance drivers

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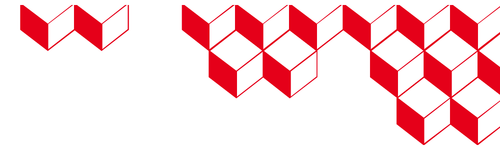
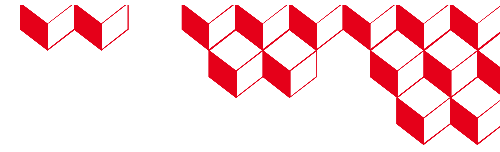
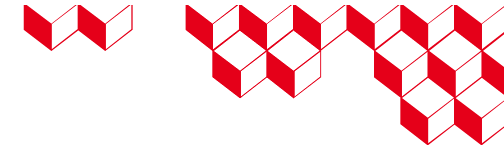


Outline

- Why going vertical ?
- 3D integration toolbox
- 3D integration for innovative architectures



Why going vertical ?



Three-Dimensional IC Trends

YOICHI AKASAKA

Invited Paper

VLSI will be reaching to the limit of minimization in the 1990s, and after that, further increase of packing density or functions might depend on the vertical integration technology.

Three-dimensional (3-D) integration is expected to provide several advantages, such as 1) parallel processing, 2) high-speed operation, 3) high packing density, and 4) multifunctional operation.

Basic technologies of 3-D IC are to fabricate SOI layers and to stack them monolithically. Crystallinity of the recrystallized layer in SOI has increasingly become better, and very recently crystal-axis controlled, defect-free single-crystal area has been obtained in chip size level by laser recystallization technology.

Some basic functional medels showing the concept or image of a future 3-D IC were fabricated in two or three stacked active layers.

Some other proposals of subsystems in the application of 3-D structure, and the technical issues for realizing practical 3-D IC, i.e., the technology for fabricating high-quality SOI crystal on complicated surface topology, crosstalk of the signals between the stacked layers, total power consumption and cooling of the chip, will also be discussed in this paper.

INTRODUCTION

The ultimate IC structure of the future is thought to consist of stacked active IC layers sandwiched by insulating materials.

Various devices or circuit functions, such as photosensors, logic circuits, memories, and CPUs, will be arranged in each active layer and, as a result, a remarkable improvement in packing density and functional performance will be realized.

In 1979, it was reported that polysilicon deposited on insulator can be melted and recrystallized by laser irradiation [1] and that the crystal perfection of the layer can be adequate to allow the fabrication of devices.

The quality of the recrystallized layer can be characterized by carrier mobility. As shown in Fig. 1, the electron mobility reported so far has increased year by year and has attained a value comparable to bulk crystals. This improvement was a trigger for starting research and development of 3-D ICs.

A partial 3-D structure has already been tried for a dynamic memory (DRAM) cell [2], [3]. For high-density RAMs,

Manuscript received January 23, 1986; revised August 8, 1986.
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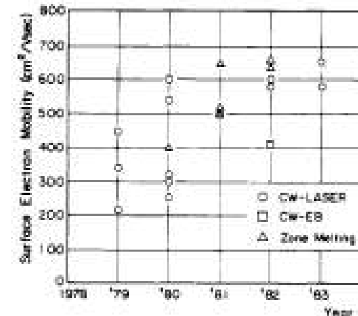

Fig. 1. Progress of surface carrier mobility of MOSFET fabricated on SOI layer. ○—CW laser; □—electron beam; △—carbon strip heater.

such as the 4-Mbit DRAM, the area of the memory cell capacitor is limited, so in order to increase the cell capacitance, a 3-D structure, i.e., a trench cell or a stacked capacitor cell, has been tried. This partial 3-D structure will be used in 2-D VLSIs within a few years.

To achieve a breakthrough in the packing density of advanced VLSIs, it is reasonable to consider a 3-D structure, containing either partially or completely stacked active layers. Fig. 2 shows a forecast of the development of 3-D ICs schematically, as 3-D technology progresses. This figure was obtained from the 3-D IC Research Committee of the 3-D

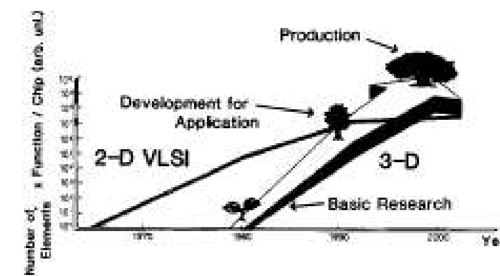

Fig. 2. Forecast of progress of 3-D technology.

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1986 review

Expecting 3D production around 2000

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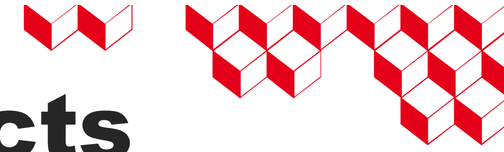
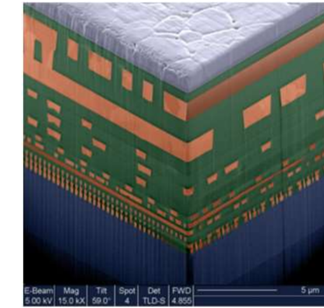


Moore's law puts pressure on interconnects

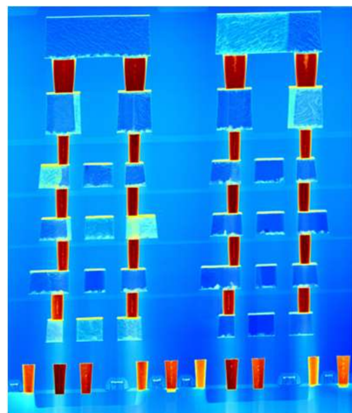
- **Consequences of miniaturization**
  Dramatic R.C increase → interconnect delay
- **Countermeasures to reduce R.C**
  Switch from Al to Cu & introduction off low-k dielectrics



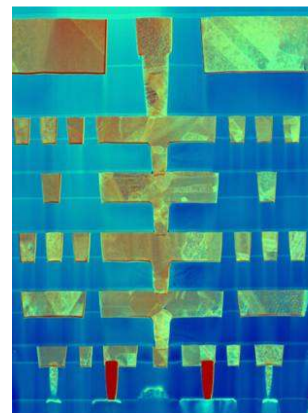
Circuit cross section

CMOS node	130 nm	32 nm
Interco. layers	6	9
M1 min. pitch	350 nm	112,5 nm
M4 min. pitch	756 nm	168,8 nm
M6 min. pitch	1204 nm	337 nm

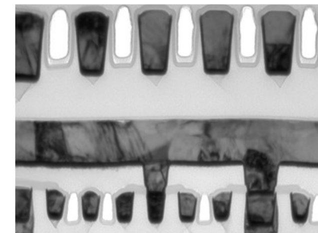
Back end of line design rules (Intel)



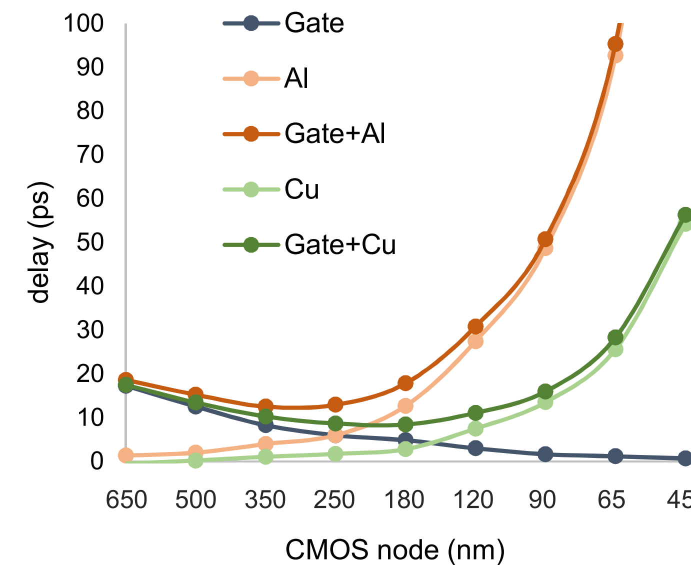
Al lines / W vias
SiO_2 dielectric



Cu line & via
Low-k dielectric



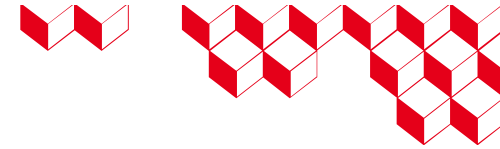
Intel 14nm CMOS BEOL



$$\tau_{BEOL} \propto RxC$$

$$\tau_{gate} = \frac{C_G \cdot V_{DD}}{I_{ON}}$$

- **R.C delay has become a major performance issue**

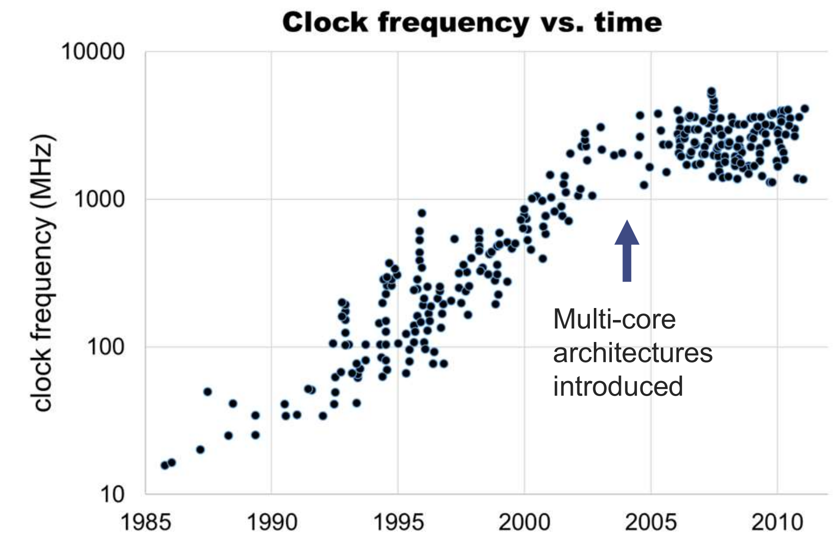


New paradigms are needed

- **Interconnects Bottleneck**
  Dramatic R.C increase → circuit frequencies limited

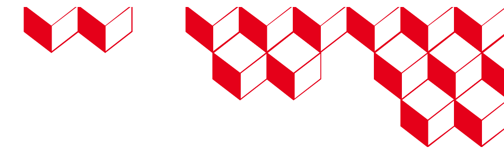
- **Scaling becomes costly**
  High manufacturing cost, low yield with large die
  High development cost (mask, IP porting, verif…)

- **Heterogeneous architectures needed**
  More processing (AI, perception accelerators…)
  More data to handle (memory capacity, fusion…)
  More modularity, scalability & sustainability



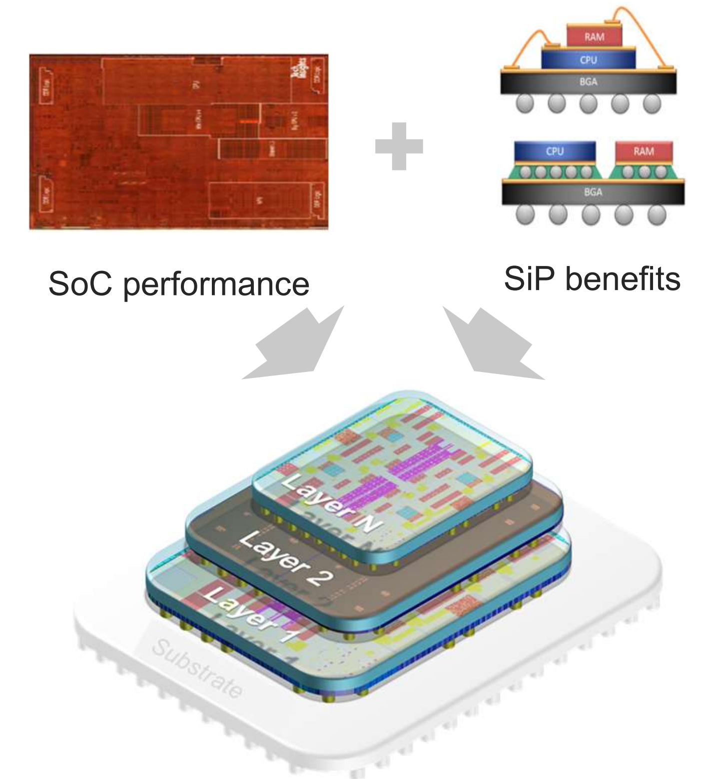
A. Danowitz (Stanford University)

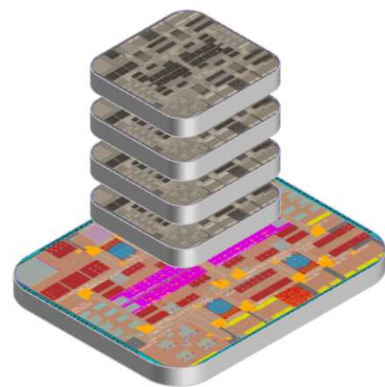
Cost of advanced designs (IBS, July 2022)



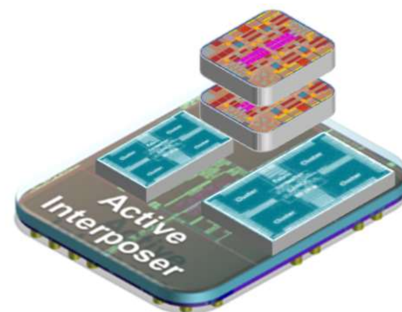
3D benefits for advanced systems

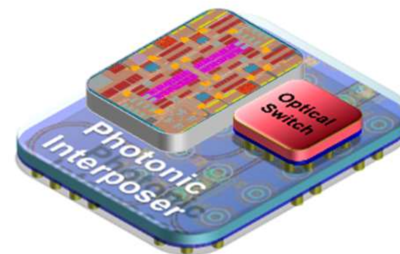
- **Best of all trends: Moore + more than Moore**
  Combination of SoC performance with SiP diversity
- **High-performance interconnections**
  Low R, L, C + massively parallel vertical processing
- **Modern answers to design needs**
  I/O number non limited, partitioning, IP reuse, scalability & density
  Mixed CMOS nodes & materials (Si, III-V, II-VI, passives, MEMS)



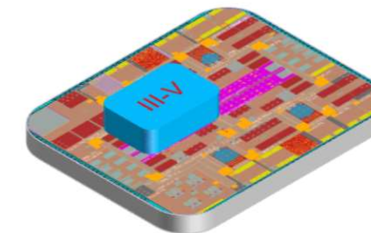


Memory on Logic

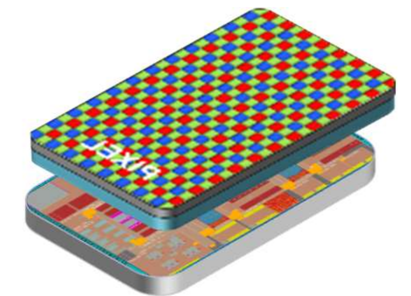




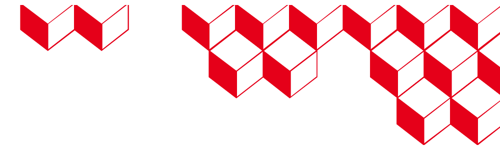
Chiplet-based integrations



III-V on Logic

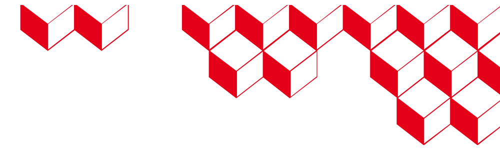


Sensor on logic



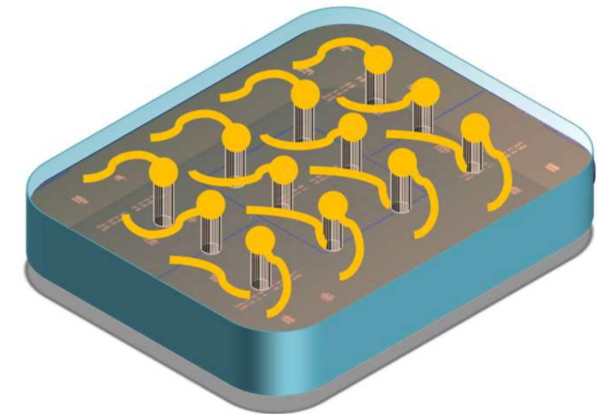
2.

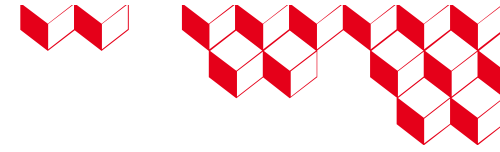
3D integration toolbox



Morphology of a 3D circuit

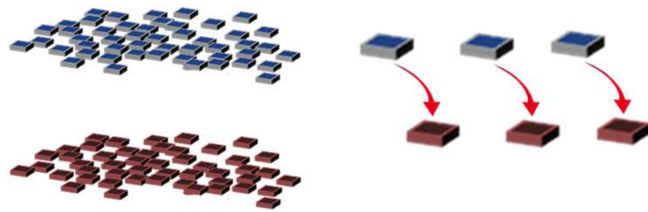
- **<u>Thin</u> stacked layers**
  Layer 1 (# bottom die) / (…) / Layer N (# top die)
- **Layer-to-layer vertical interconnects**
  Miniaturization trend: pillars, hybrid bonding …
- **Intra-layer vertical interconnects**
  Communication between frontside and backside of each layers
  Through silicon Vias (TSV)
- **Intra-layer in-plane interconnects (2D)**
  ReDistribution Layers (RDL)





Assembly configurations

Die to die

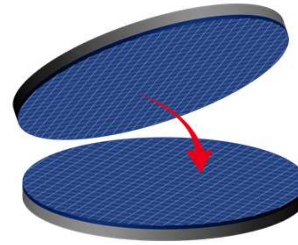


(+)
- Known Good Dies → yield
- Heterogeneous integration
- Flexible design

(−)
- Low assembly throughput
- Low alignment accuracy
- Very high cost

Pure packaging operation

Wafer to wafer

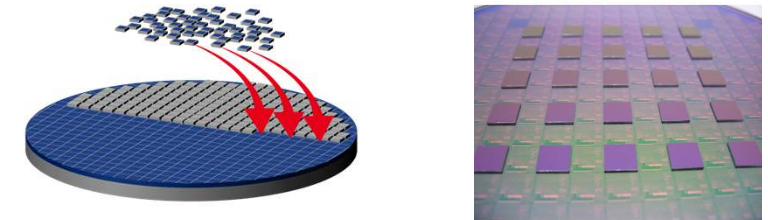


(+)
- Collective process
- High assembly throughput
- High alignment accuracy

(−)
- Yield loss
- Strong design limitation

Mass production for image sensors and memories

Die to wafer



(+)
- Known Good Dies → yield
- Heterogeneous integration
- Flexible design

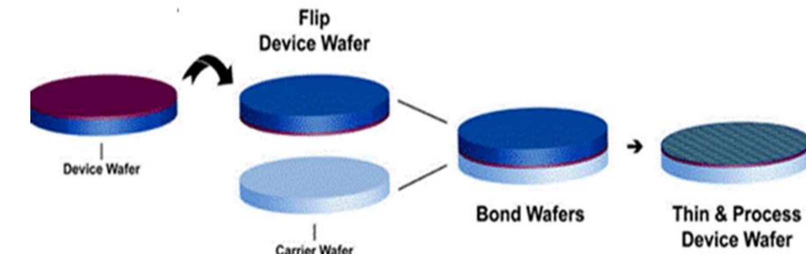
(−)
- Low assembly throughput
- Low alignment accuracy

Breakthrough processes needed

Wafer bonding techniques

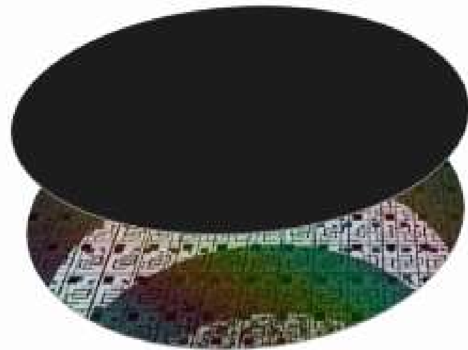
- **Why & how ?**
  Thin wafer processing (<300µm)
  Wafer-to-wafer 3D stacking
  Temporary or permanent bonding

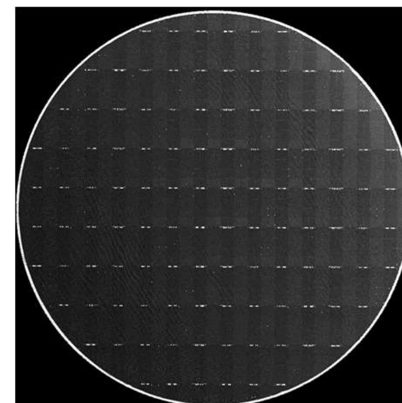
50 µm thin silicon wafer



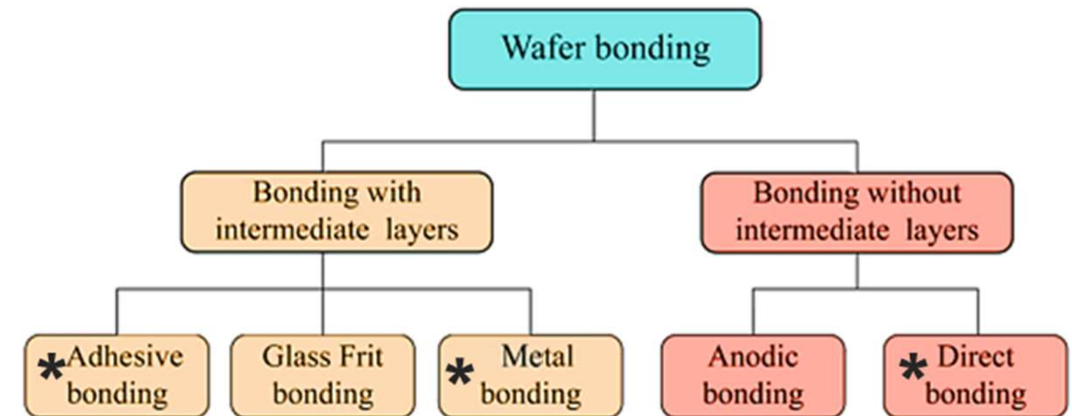
Thin wafer processing on carrier

- **A wide range of processes**
  Each with own strengths and weaknesses





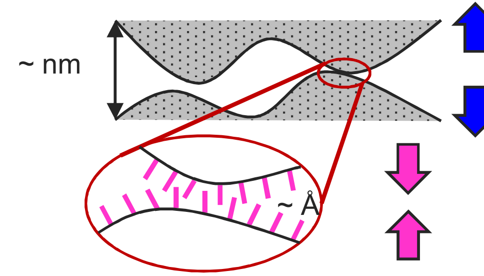
Scanning acoustic microscopy



*** most used processes**

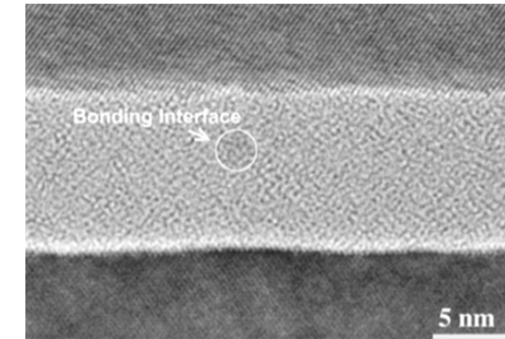
Direct bonding process

- **Bonding without added material**
  Based on attraction of very smooth surfaces
  Flatness & cleanliness at all scales → CMP

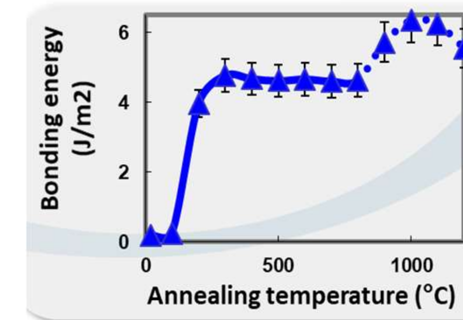


Bonding wave: glass to Si & Si to Si bonding

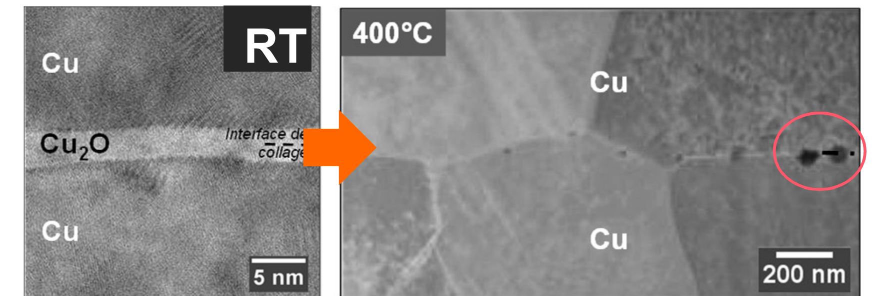
- **SiO_2/SiO_2 bonding**
  Required roughness < 0,65nm rms [1]
  Van der Waals interaction at T_{amb}
  Covalent bonds formed after annealing



SiO_2/SiO_2 interface after annealing

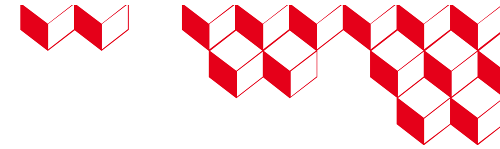


- **Cu/Cu bonding**
  Required roughness < 0,5nm rms [2]
  Cu recrystallization during annealing > 200°C [3]

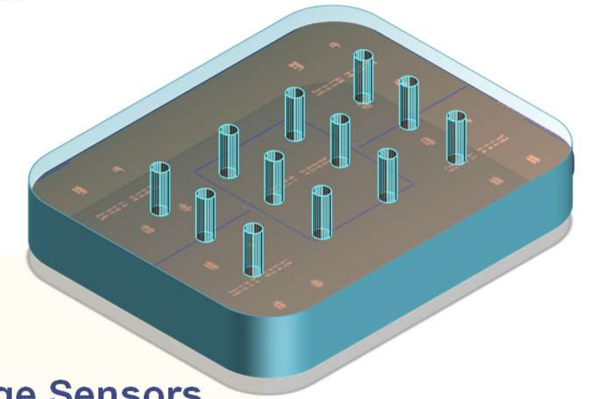


Cu/Cu interface before/after annealing

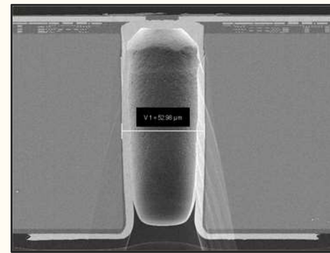
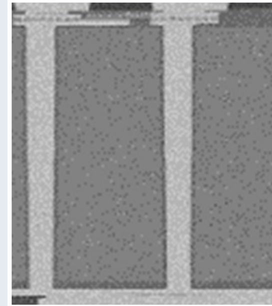
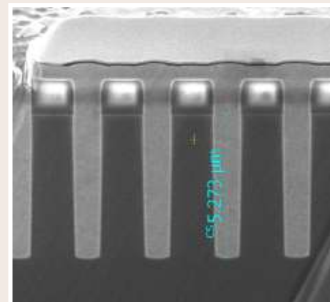
[1] F. Rieutord, et al. *ECS Trans.,* vol. 3, no. 6, pp. 205–215, 2006
[2] H. Moriceau, *Microelectronics Reliability*, vol. 52, no. 2, pp. 331–341, 2012
[3] L. Di Cioccio, et al., *J. Electrochem. Soc.*, vol. 158, no. 6, pp. P81–P86, 2011

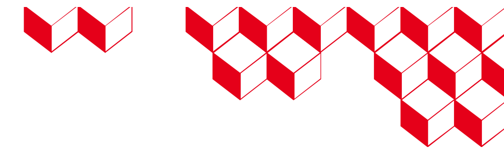


Through silicon via (TSV) technologies

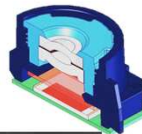


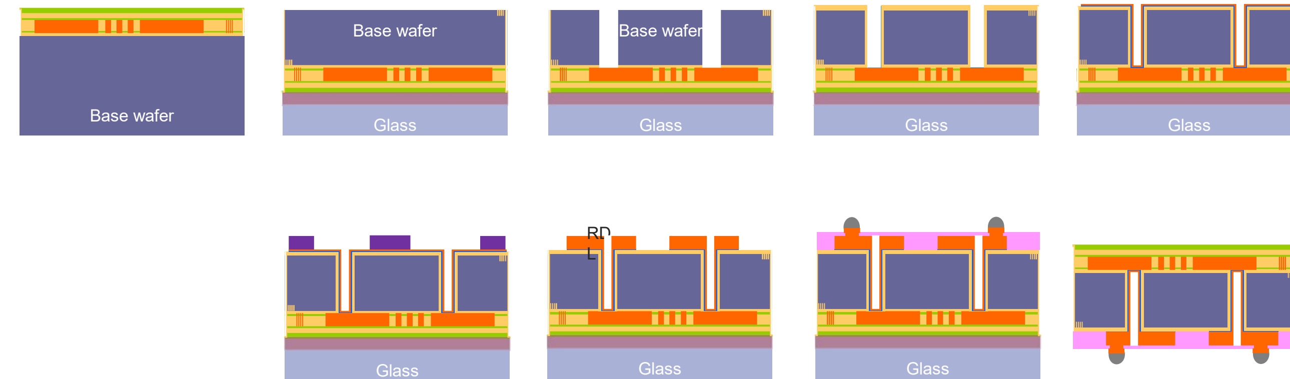
TSV pitch

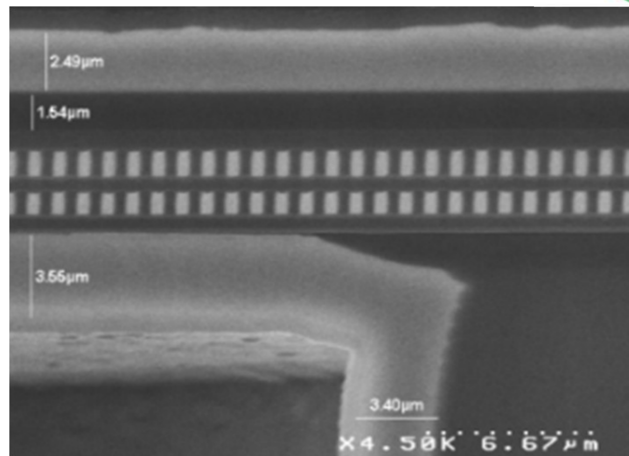
TSV pitch	Type	Image	Density	Applications
100-500µm Ø 40-100µm R_{TSV} = 2-10 mΩ C_{TSV} = 2 pF	**TSV last low density**		100 TSV/mm² ➔ low I/O	**CMOS Image Sensors** **X-Ray focal plane arrays** **IR sensors**
20-50 µm Ø 2-15 µm R_{TSV} = 20 mΩ C_{TSV} = 0.1 pF	**TSV middle**		1 000 TSV/mm² ➔ Core/Chips	**System in Package** **Interposers / Chiplets**
1-10 µm Ø <2 µm R_{TSV} = 0,5-1 Ω	**High density TSV**		100 000 TSV/mm² ➔ Logic blocs	**3D Imagers** **Displays** **Power Delivery Network**



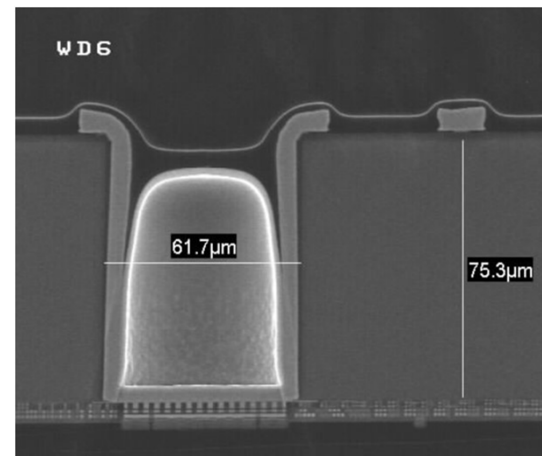
“TSV last” low density process

- **Done <u>after</u> full CMOS process [4]**
  Wafer bonding on carrier & low temp. process
  AR (= height/diameter) increased over time
  Keep out zone + alignment → area penalty
- **Industrially mature since 2008**
  CMOS image sensors 

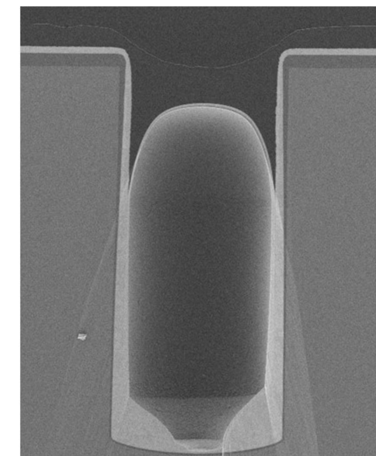




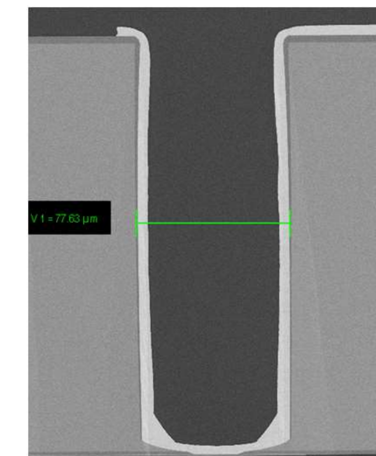
TSV contact on Metal1 layer



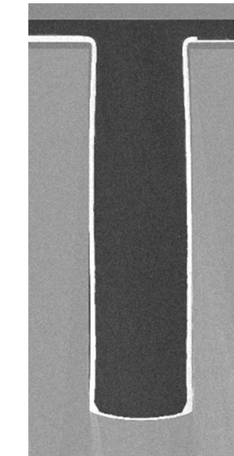
AR 1,2 after passivation



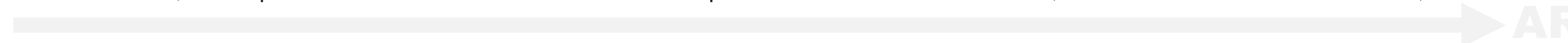
AR 2 after passivation



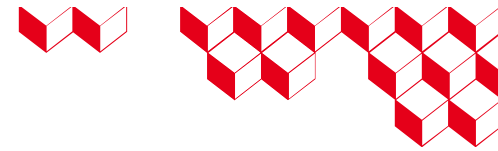
AR 2,5 after RDL



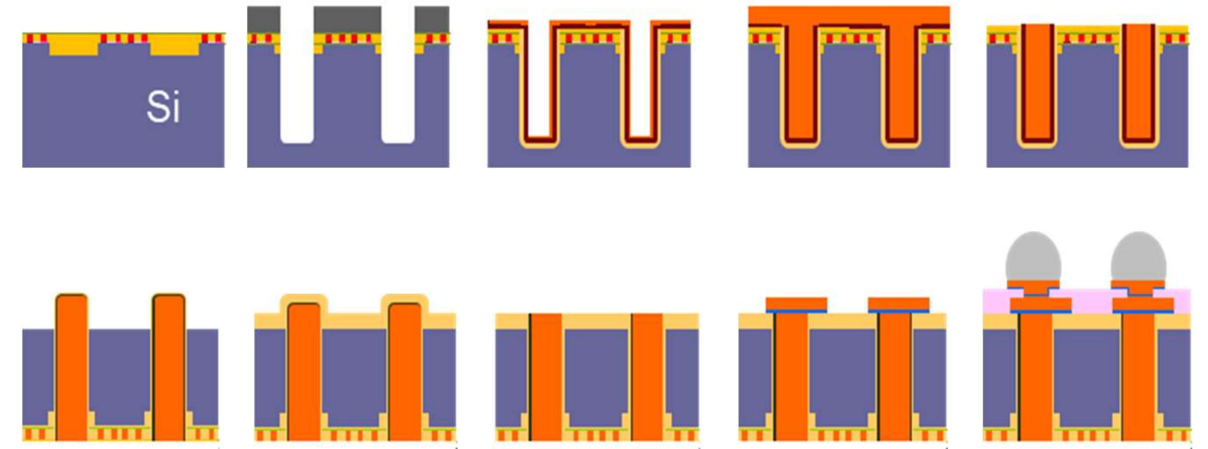
AR 3,7



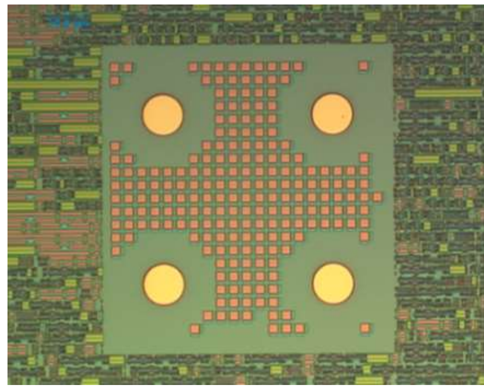
[4] D. Henry et al., Electronic Components and Technology Conference, 2008



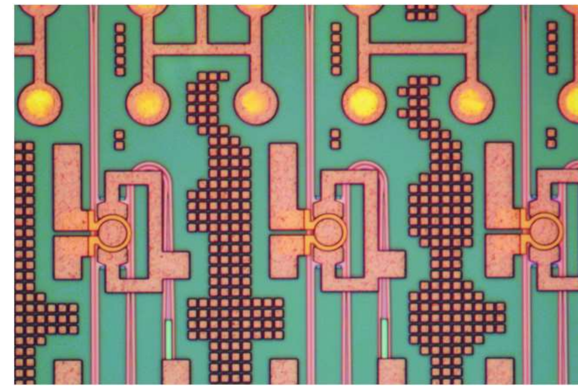
“TSV middle” process



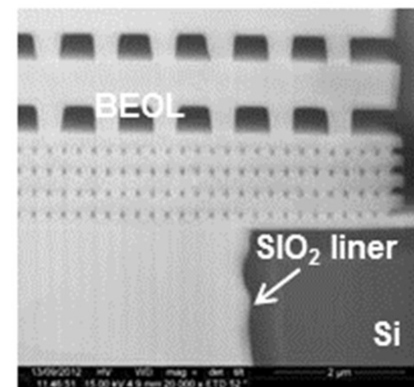
- **Done <u>during</u> CMOS process [5]**
  Aspect ratio usually > 10, Diameter 2-15 µm
  TSV etched & filled with Cu prior to BEOL process
  TSV revealed on backside after Si thinning
  Reduced keep out zone vs. TSV last
- **Industrially mature since 2013**
  DRAM stacks, FPGA (Xilinx)



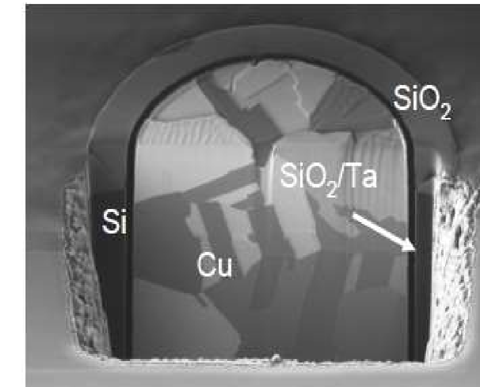
TSV Middle after CMP



TSV co-integrated with microring resonators

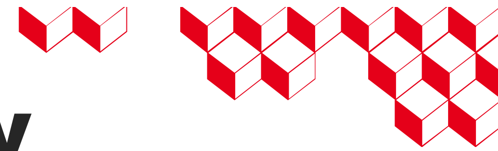


TSV & CMOS BEOL



TSV structure

[5] P. Coudrain et al., EPTC 2012



"High density TSV" (HD-TSV) process flow

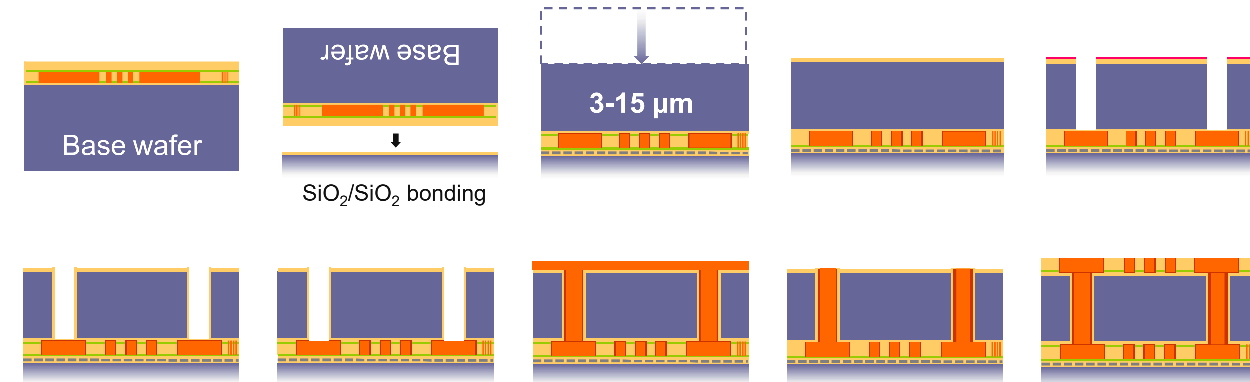
- **Done <u>after</u> circuit processing [6]**

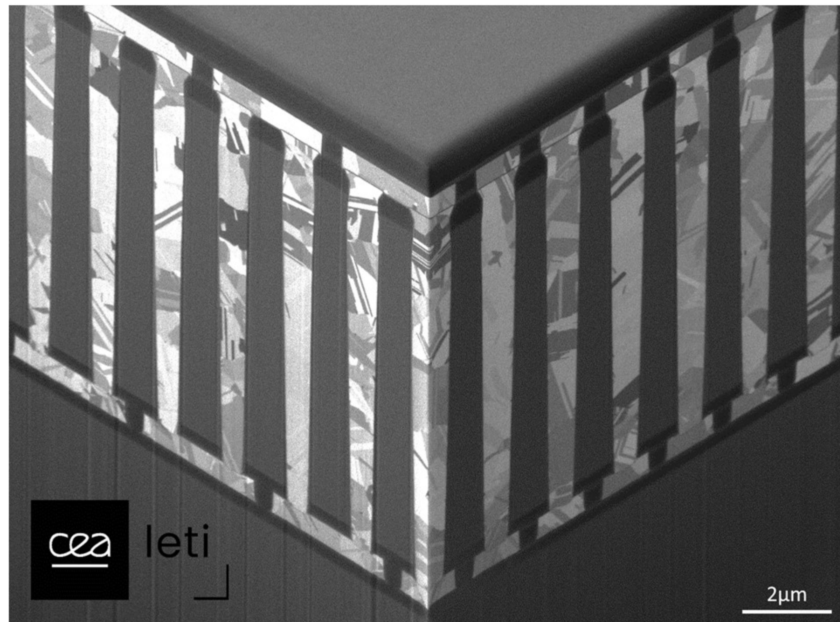
  Diameter typically < 2µm & height <15 µm

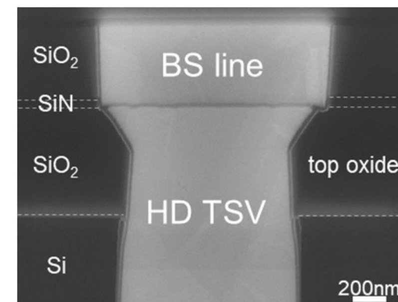
  Ultra-uniform Si thinning needed (TTV < 1µm)

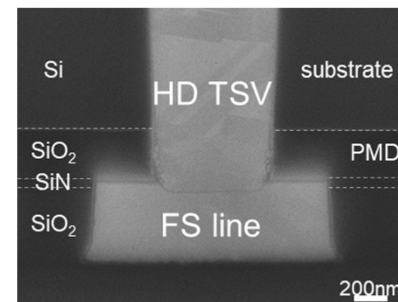
- **R&D activity**

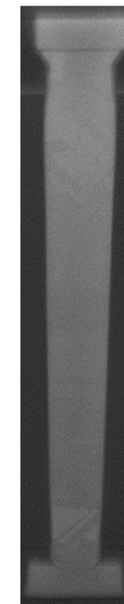
  Power delivery network (PDN), SPAD arrays





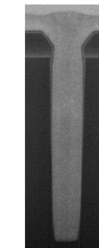






1x10 µm

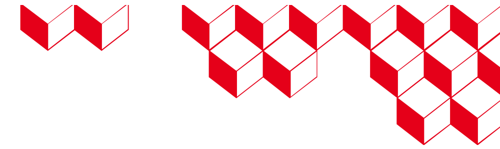
1x6 µm



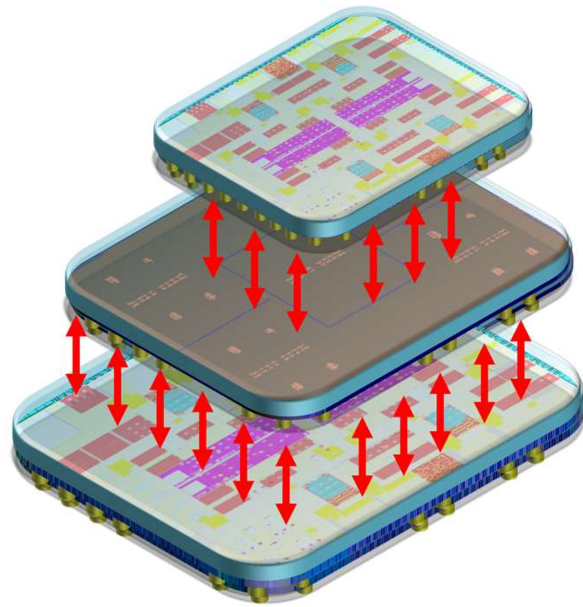
0.5x3 µm

TSV HD miniaturization trend

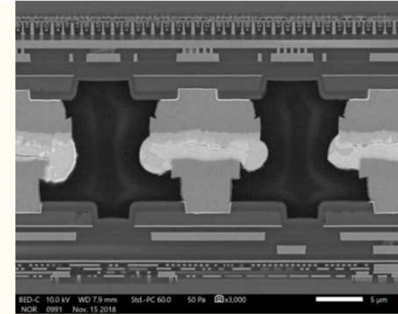
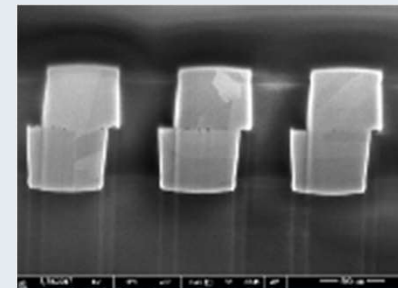
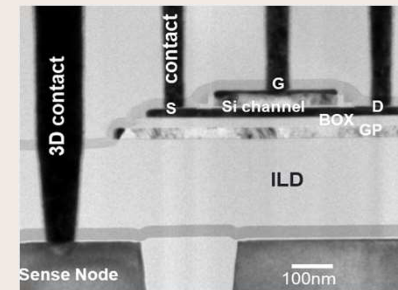
[6] S. Borel et al., ECTC 2023



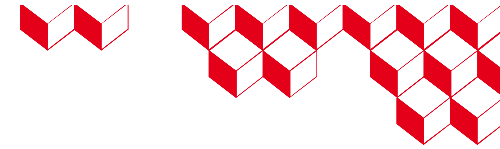
Technologies for 3D interconnects



3D pitch

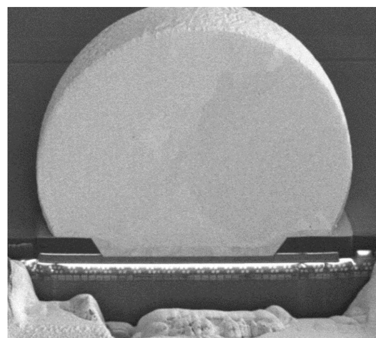
3D pitch	Technology	Image	Density	Integration
> 100µm	**Solder-based**		10^3/mm² Circuit level	Die to Die Die to Wafer Wafer to Wafer
100nm-10µm	**Hybrid bonding**		10^6/mm² Logic-block level	Die to Wafer Wafer to Wafer
<100nm	**Sequential 3D**		10^8/mm² Transistor level	Wafer to Wafer

cea

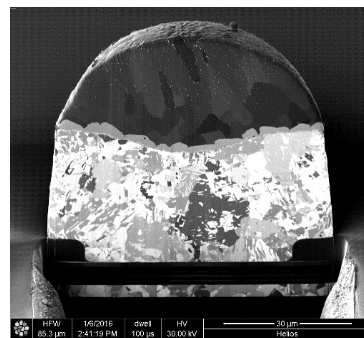


Solder-based interconnects for flip-chip

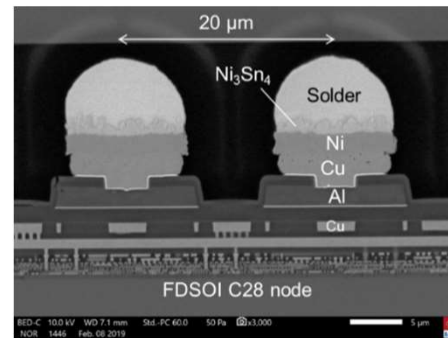
- **Solder choice vs. temperature**
  SnPb (183°C)→ historical, but Pb now forbidden in EU
  SnAg (221°C), SnAgCu (217°C), In (152°C)…
- **Interconnect process**
  Paste printing & ball serigraphy for large geometries
  Semi-additive process with (ECD) for reduced pitch
  Polymer underfill systematically added in free space



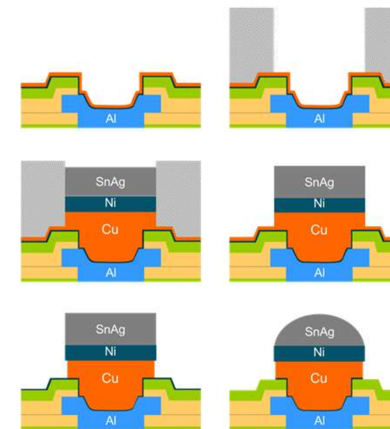
200µm diameter SnAgCu Paste printing



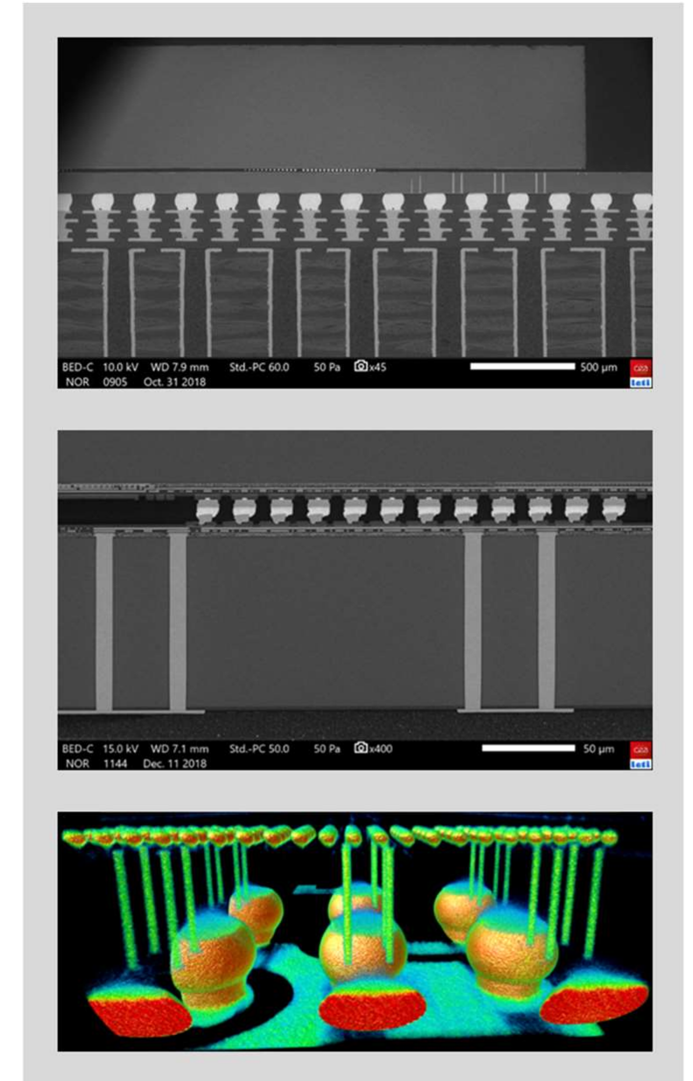
70µm diameter Cu/SnAg ECD



10µm diameter Cu/SnAg Pillars ECD



Semi-additive process

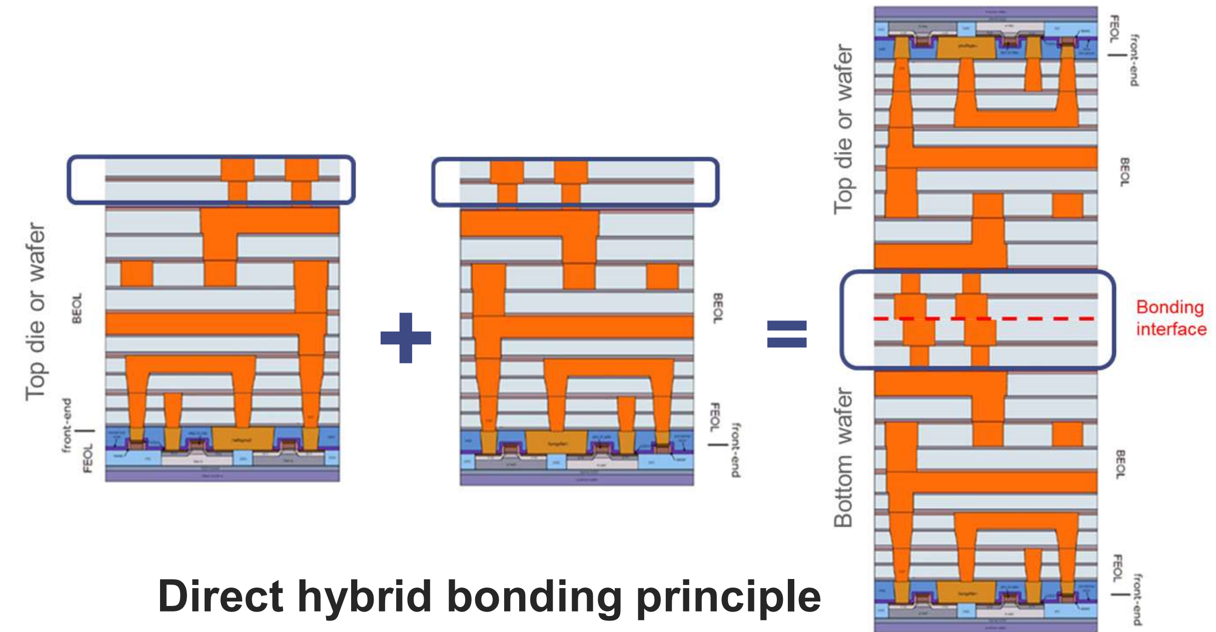


2-layer stack on BGA: 10µm Pillars between top and bottom and 70µm bumps between bottom and BGA [7]

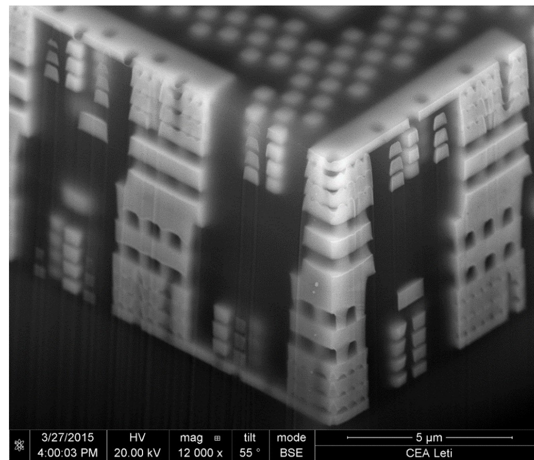
[7] P. Coudrain et al., ECTC 2019

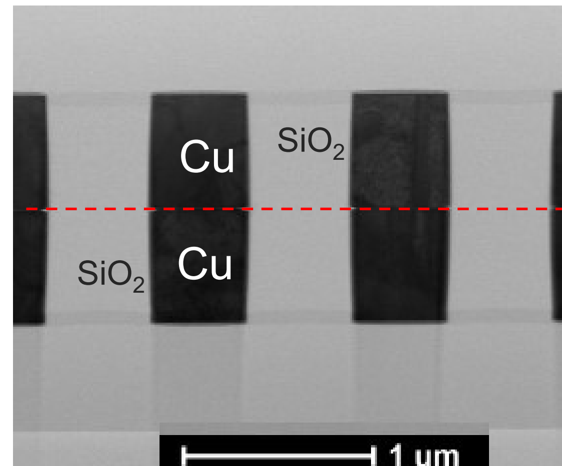
Direct hybrid bonding process: a hot topic !

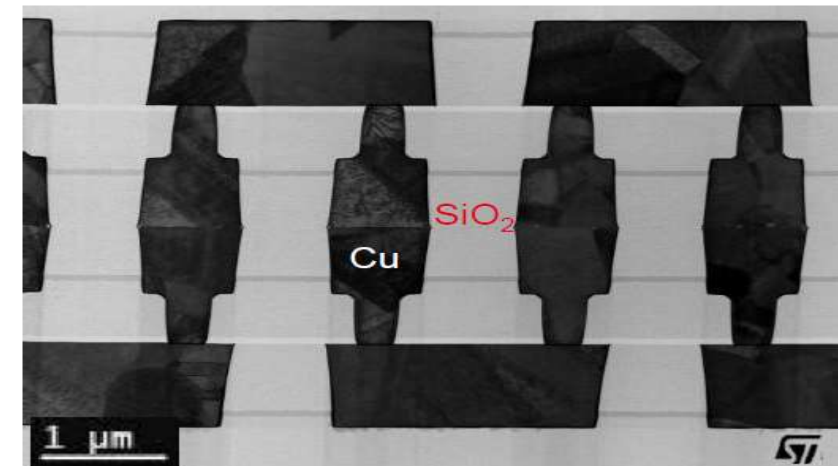
- **Mix SiO_2/SiO_2 & Cu/Cu bonding**
  Precautious CMP process
  Specific design rules to control dishing in Cu
- **Unprecedented interconnect pitch**
  1µm pitch demonstrated in 2017
  Precision alignment is key: 50nm expected in 2025



Direct hybrid bonding principle





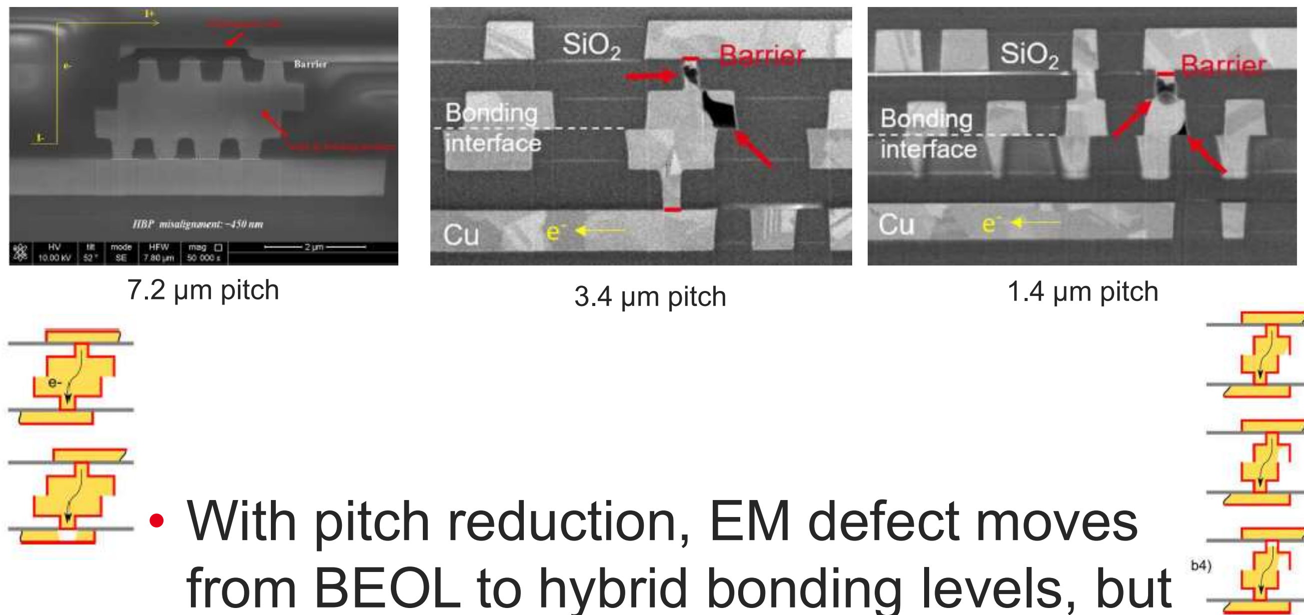


[9] Y. Beilliard, PhD Thesis, Univ. Grenoble Alpes, 2015

[8] J. Jourdon et al., IEDM 2018

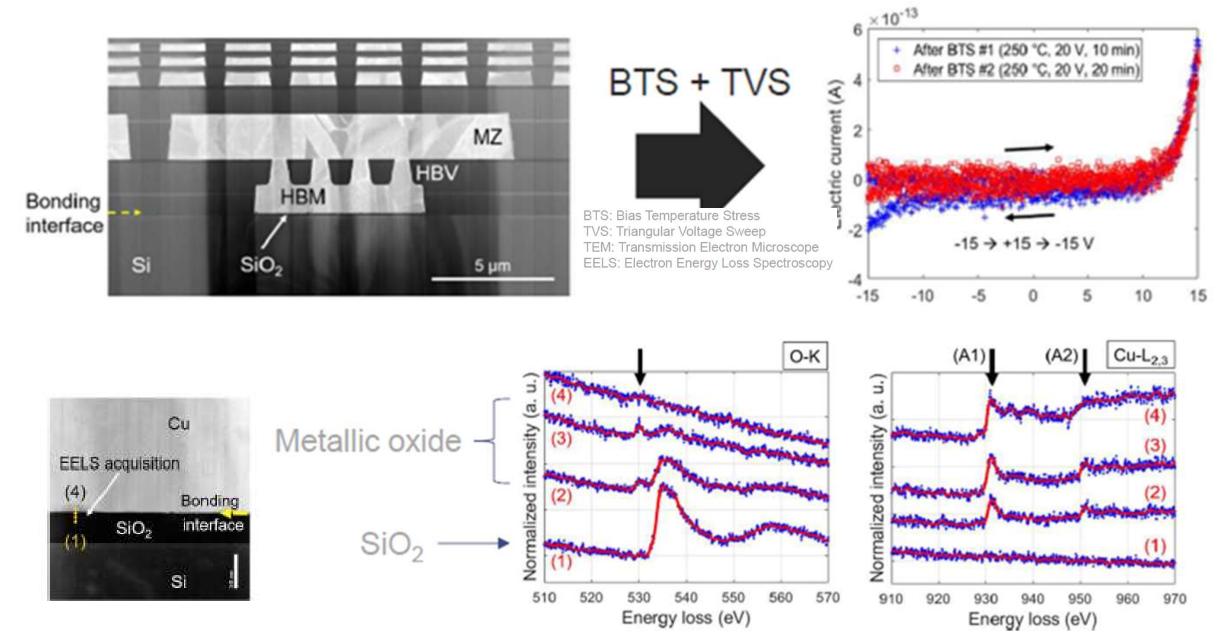
Extensive reliability studies on hybrid bonding

Electromigration performance vs. pitch reduction



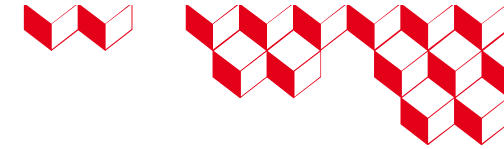
- With pitch reduction, EM defect moves from BEOL to hybrid bonding levels, but **extrapolated lifetimes are not affected at use conditions [10,11]**

Susceptibility to Cu diffusion ?



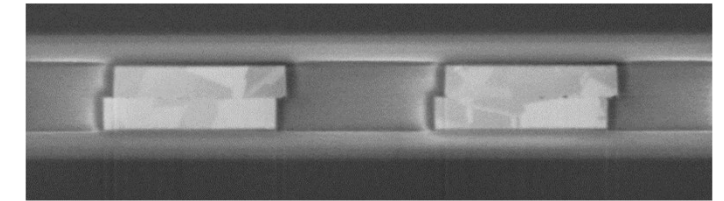
- **No diffusion identified**, thanks to the presence of 3 nm Cu_2O layer barrier, stable with time and temperature

[10] S. Moreau et al., ECTC 2016
[11] S. Moreau et al., IRPS 2023
[12] Ayoub et al., IRPS 2022
[13] Ayoub et al., Micro rel. 2023

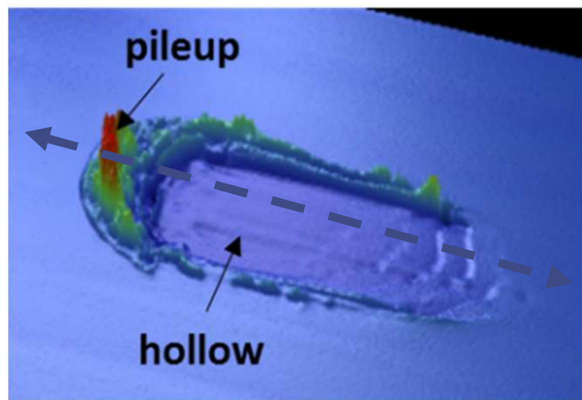


Die-to-wafer hybrid bonding challenges

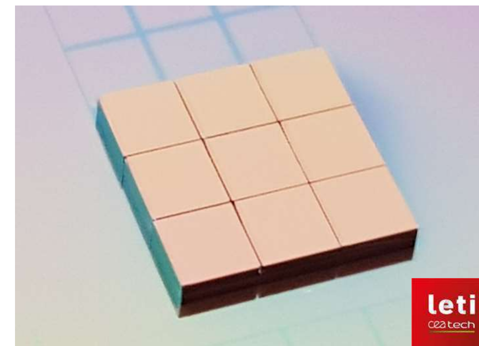
- **Known Good Die strategy** [14,15]
  Probing marks to make compatible with bonding
- **Pitch reduction trend** [16]
  Alignment precision is the key to success
  Multi-pitch for design flexibility, reduced interdie-space



5µm interconnection pitch



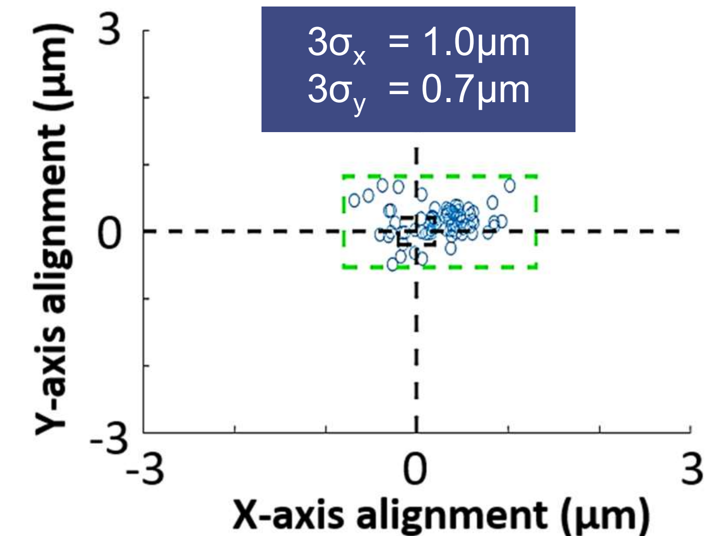
Probing marks



3 x 3 mm²

3 x 3 mm² post thinning

Die-to-wafer integration with 40µm inter-die spacing [17]

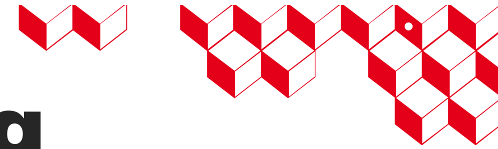


Alignment precision for 5µm pitch

- **500nm D-T-W alignment precision is expected in 2024-25**

[14] E. Bourjot et al., 3DIC 2019
[15] E. Bourjot et al., ECTC 2021
[16] E. Bourjot et al., ESTC 2022
[17] P. Metzger et al., Minapad 2022

Self-assembly approach for direct bonding

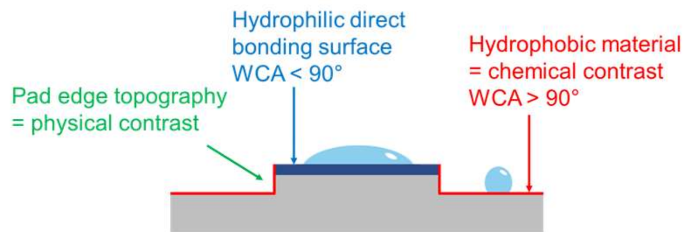


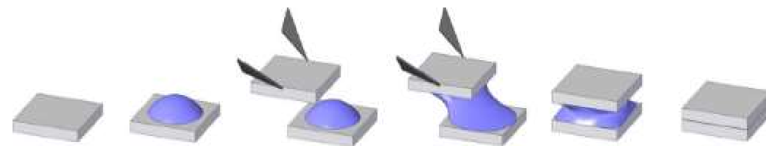
- **Capillary-assisted process [18-20]**

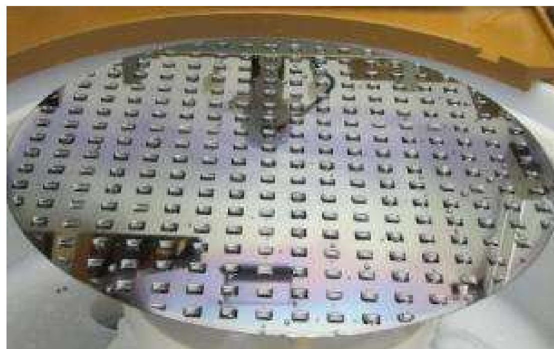
  Drop of water between chip and substrate

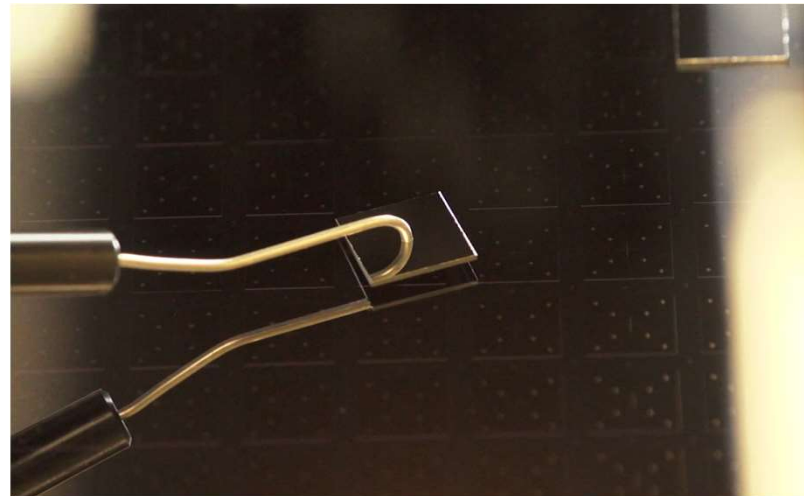
  Liquid capillary tension minimizes surface energy

  Water confinement controls alignment accuracy

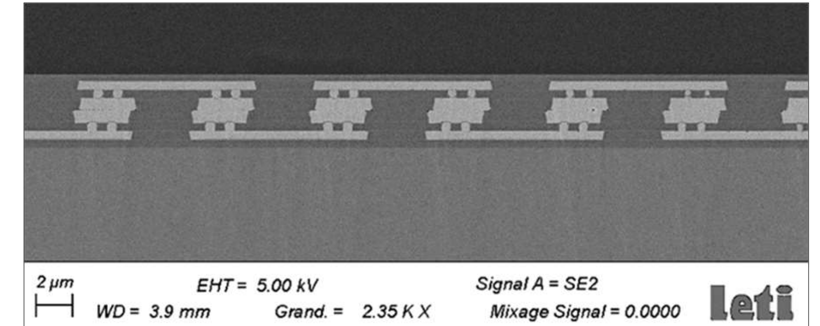




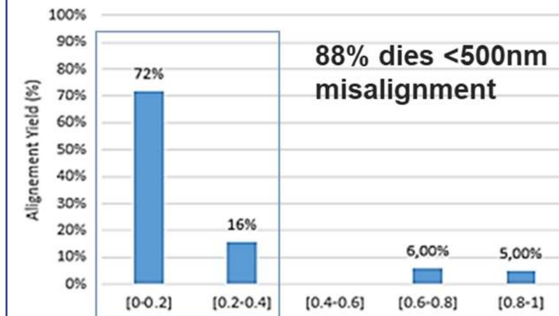


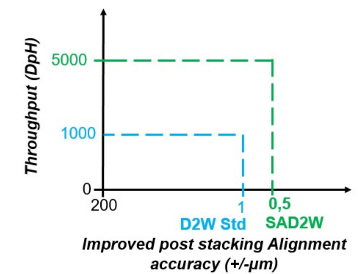


- **Performances [21,22]**



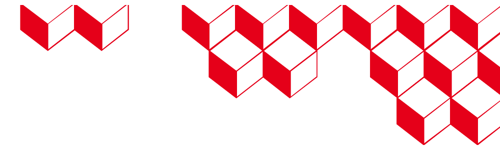
Daisy chains up to 50 000 connections with resistance similar to standard D-to-W]





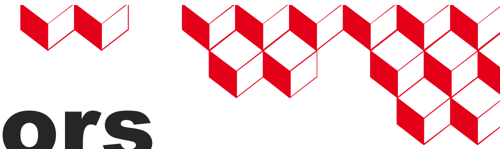
High throughput (> 5000 ph) with high precision (< 200 nm expected in 2025)

[18] S. Mermoz, PhD thesis, U. Grenoble, France 2015
[19] A. Jouve et al., ECTC 2019
[20] A. Bond et al., ECTC 2022
[21] E. Bourjot et al. ECTC 2023
[22] A. Thiolon et al., to be published at ESTC 2024



3.

3D integration for innovative architectures

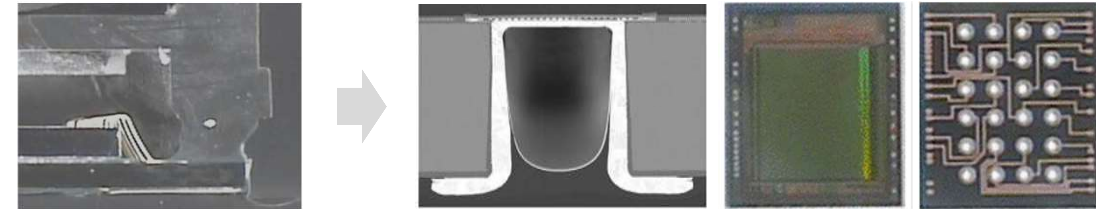


Benefits of 3D Integration for image sensors

- **Dimensions**

  Reduced form factor (x,y,z)

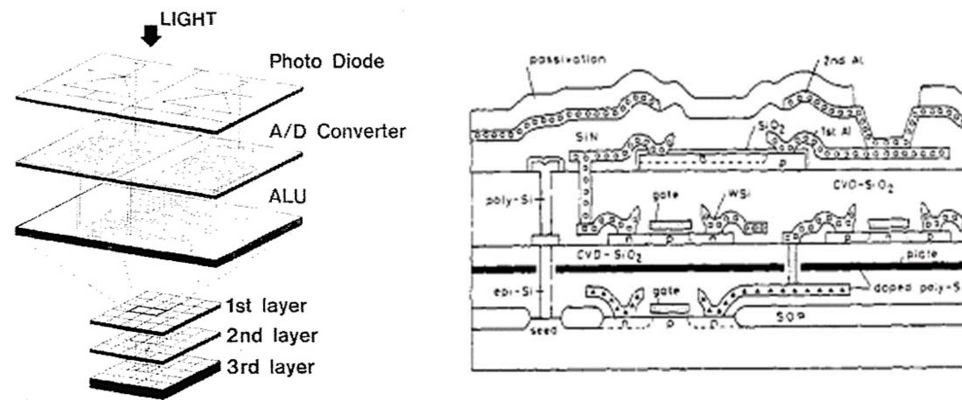
  Abuttable sensors for RX & IR sensing



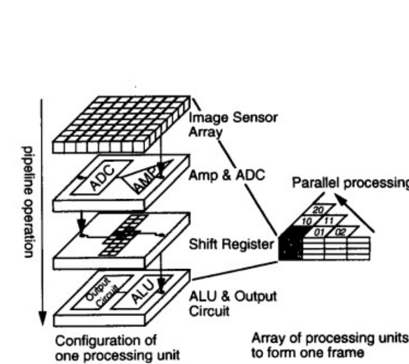
- **New architectures!**

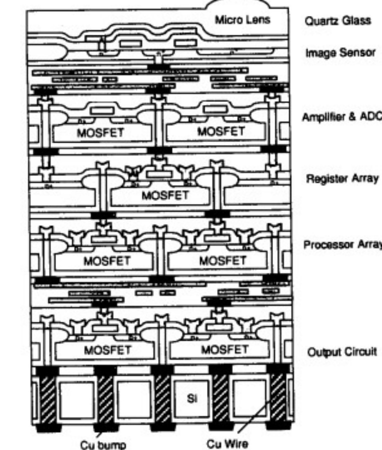
  Parallel pixel processing

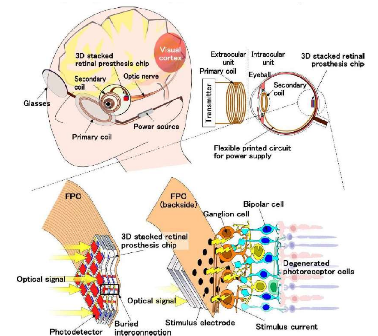
  Layers functionalization & optimization



Mitsubishi [23]







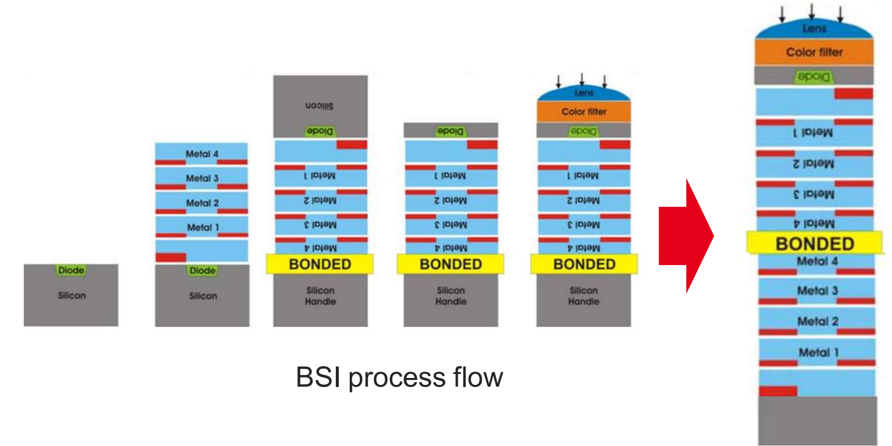
Tohoku University [24,25]

[23] T. Nishimura et al., IEDM, 1987

[24] H. Kurino et al., IEDM, 1987
[25] T. Tanaka et al., IEDM, 2007

Backside illumination as an enabler for 3D CIS

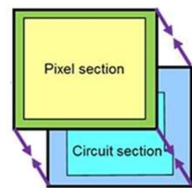
- **Backside illumination process requires wafer bonding on a carrier. There's just one step to 3D integration: replace carrier by a functional wafer!**

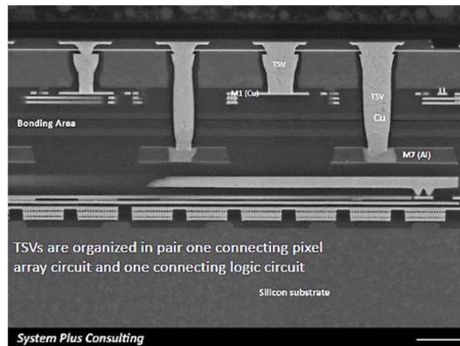


BSI process flow

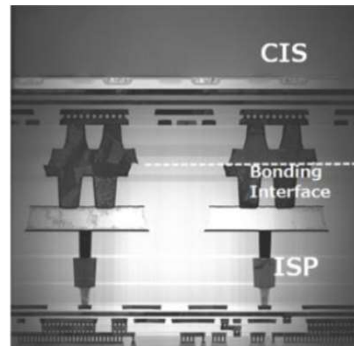
- **2-layer CIS (2013)**

Oxide bonding [26] followed by hybrid bonding [27]





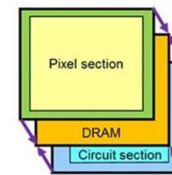
SiO2/SiO2 bonding

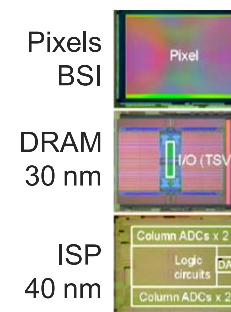


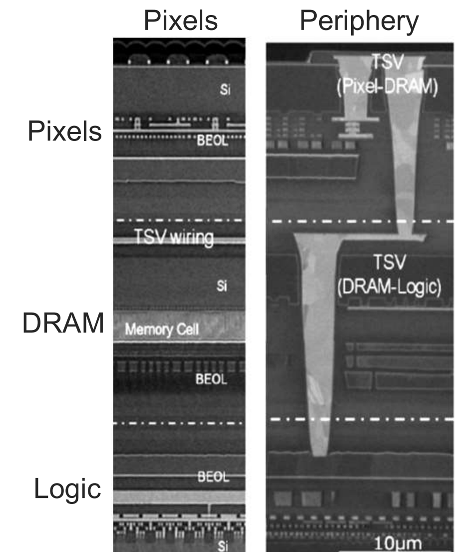
Hybrid bonding

- **3-layer CIS (2017)**

Intermediate DRAM layer [28]



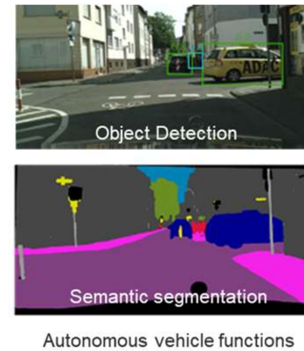




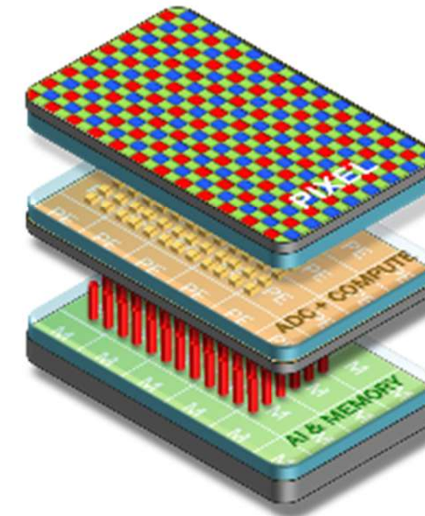
[26] Sony ISX014 1/4 Inch 8 MP, 1.12 µm Pixel Size Exmor RS Stacked Back Illuminated CIS Imager Process Review
[27] Y. Kagawa et al., IEDM, 2016
[28] H. Tsugawa et al., IEDM, 2017

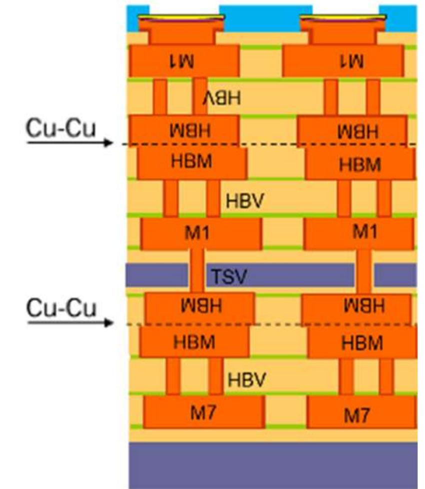
Smart imager developments

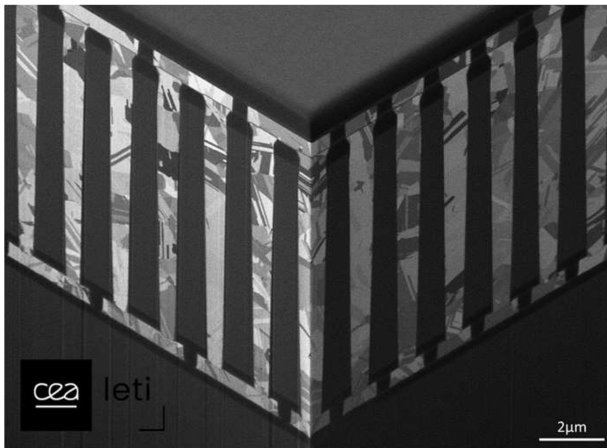
- **From imagers to vision sensors**
  Edge-AI applications for autonomous vehicle
- **3-layer scheme [29]**
  Pixel array / Readout IC / AI & memory layer
  2 hybrid bonding with 1x10µm HD-TSV



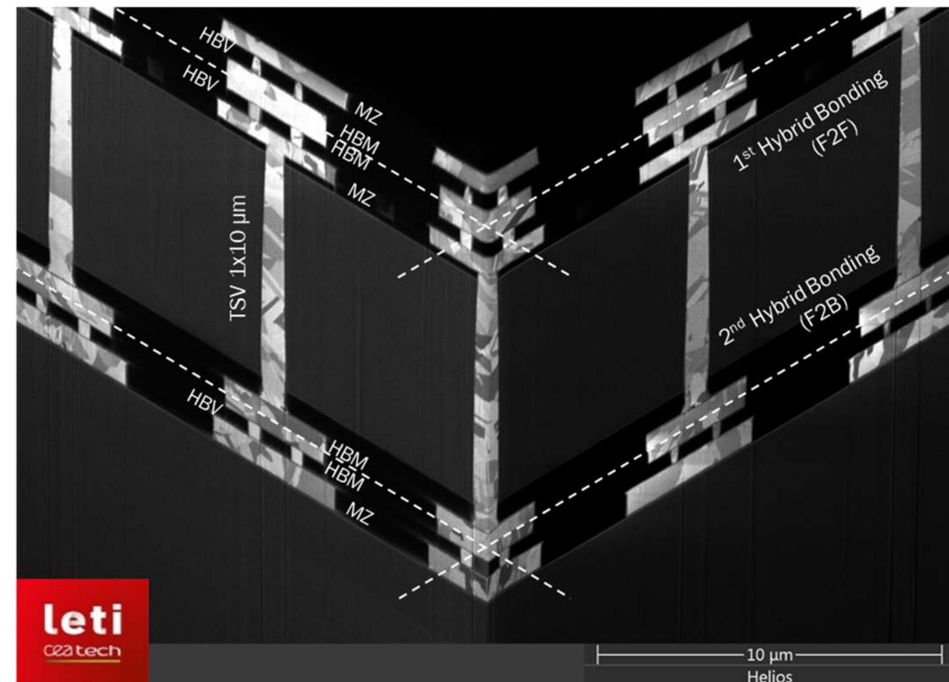
Autonomous vehicle functions



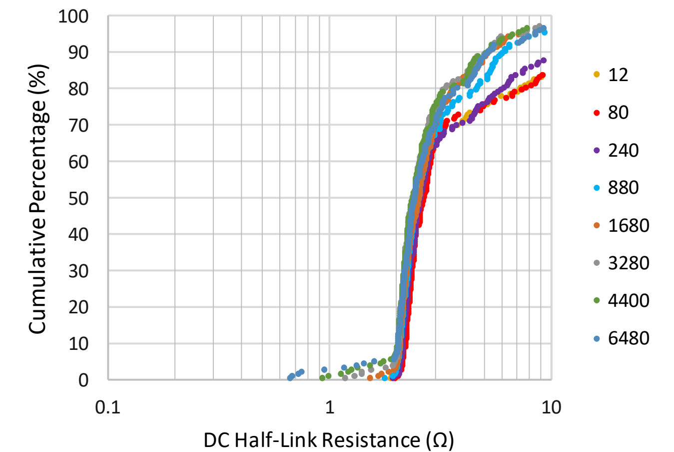




1x10µm TSV (2µm pitch), R_{TSV} = 500mΩ
Misalignment HB2: max. 1 µm (avg 200 nm)
Misalignment HB1: max. 350 nm (avg 100 nm)



Complete structure with 2 hybrid bonding and 1x10µm HD TSV [30]

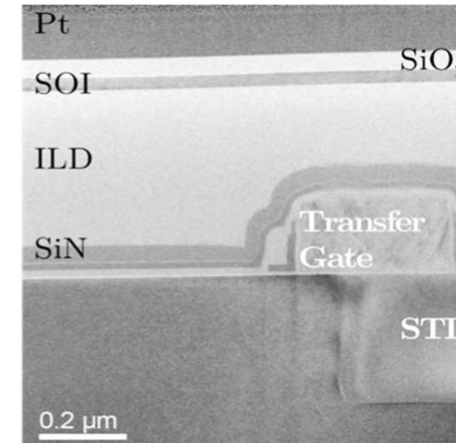


Electrical characterization of hybrid bonding/HD TSV transitions

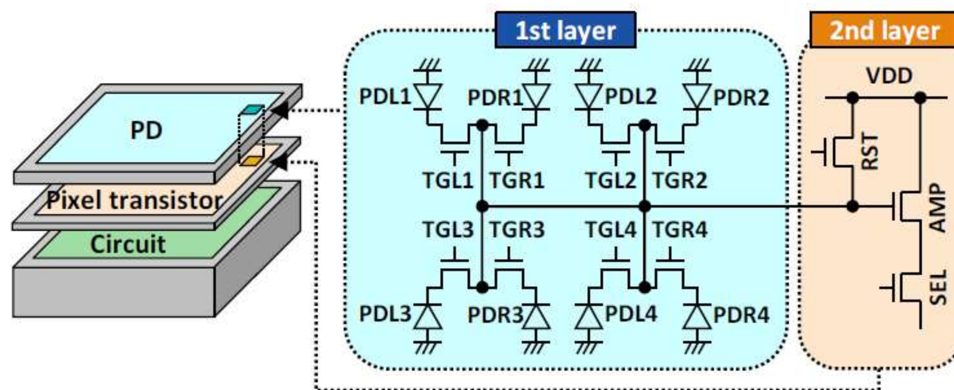
[29] J. J. Suarez Berru et al., ECTC 2023
[30] S. Nicolas et al., ECTC 2024

2-layer stacked 4T pixels CMOS Image Sensors

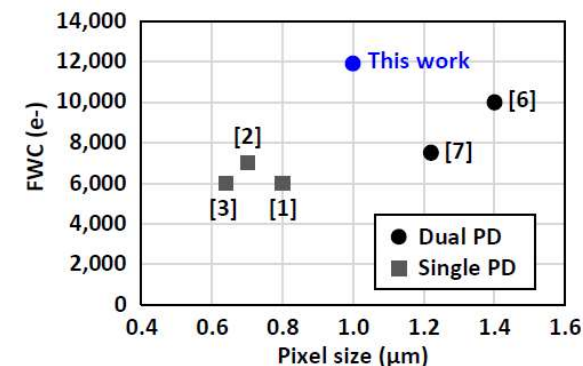
- **Pixel split for FWC increase [31]**
  BSI pinned photodiode + transfer gate on layer 1
  RST, source follower & read transistors on layer 2
- **Sequential integration mandatory**
  Misalignment between layer << 1 µm
  Mono. Si transfer + low temp. CMOS process

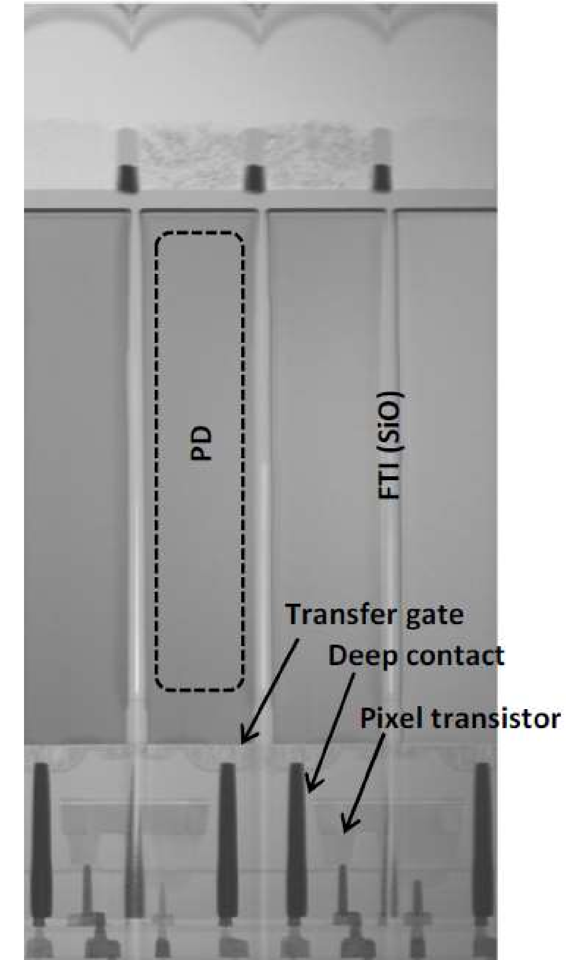


Monocristalline Si layer transfer [1]



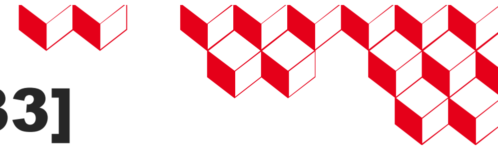
2-layer pixel schematics based on 3D sequential integration



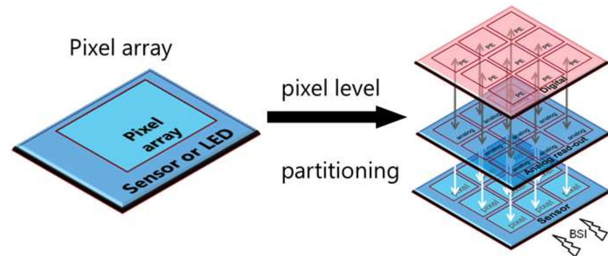


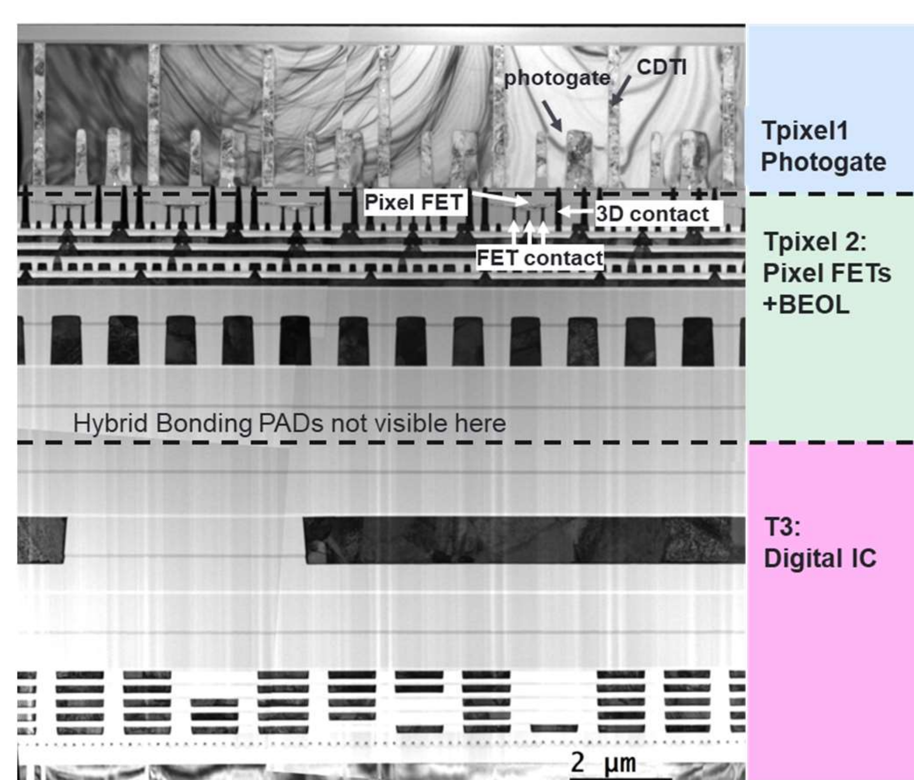
Deep photodiodes, oxide-based full trench isolation (FTI), 1µm dual photodiodes [32]

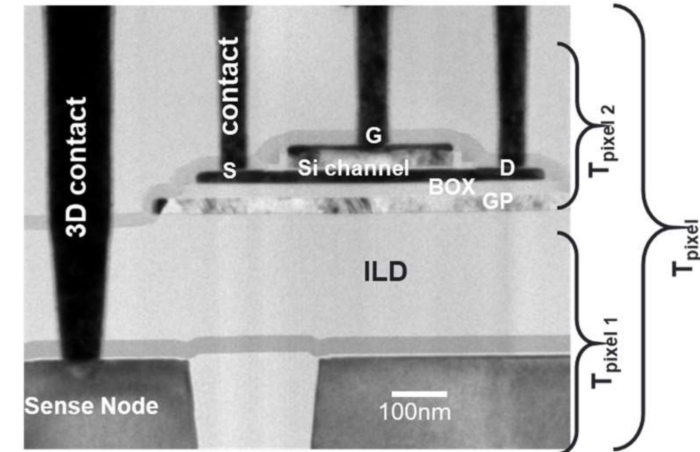
[31] P. Coudrain, IISW 2009
[32] K. Zaitsu et al., VLSI symp. on technology & circuits, 2022



Sequential 3D pixel with hybrid bonding [33]







Increased diode area

44% for 1.4µm pitch

Smart pixel

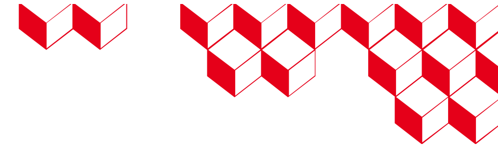
Adaptation, calibration
Pre-processing

- Sequential CMOS process
- Low temperature top level
- Nm-scale alignment between gate levels
- Applicable to heterogeneous and CMOS 3D

Combining sequential integration with hybrid bonding offers a great opportunity for pixel partitioning with pitch in the 1 µm range and distributive computing for high efficiency

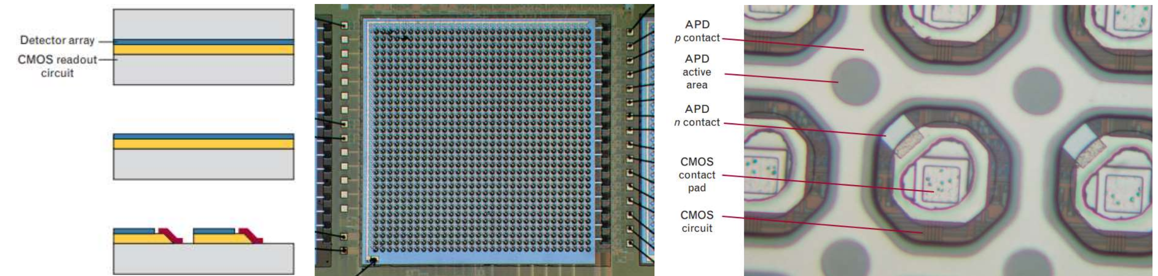
cea

[33] F. Guayder et al., IEDM 2022

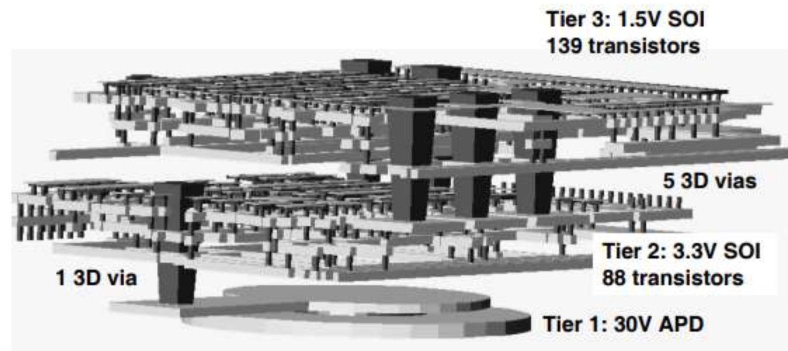


3D integration in SPAD

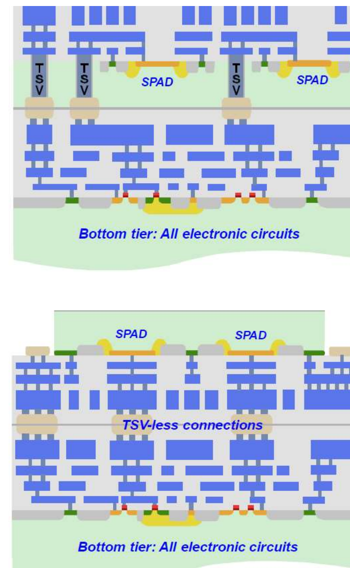
- **Separation detection & readout [34]**
  Layer optimization: CIS (90nm) & CMOS (22nm)
  Better sensitivity, high FF, low DCR & functionality
- **3D technology has evolved**
  Bridges [35], oxide bonding with metal vias [36]
  Bumping, hybrid bonding [37,38]



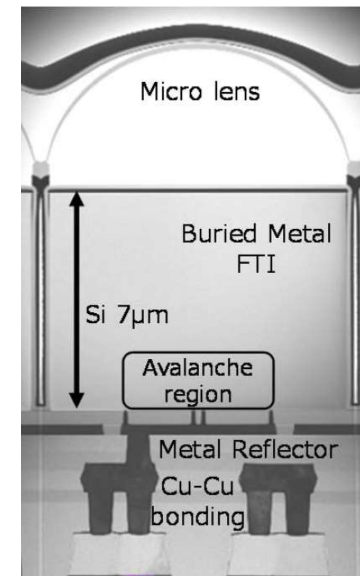
32 × 32 array “bridge-bonded” APD/CMOS [35]



3D Geiger-Mode APD with Two SOI Timing Circuit Layers [36]



Front illuminated vs. back-illuminated 3D stacked SPAD image sensors [34]



BI 10 μm SPAD pixel with FTI & Cu-Cu bonding [38]

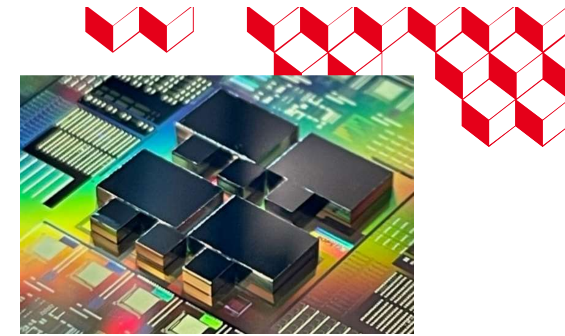
3D SPAD at IISW 2024

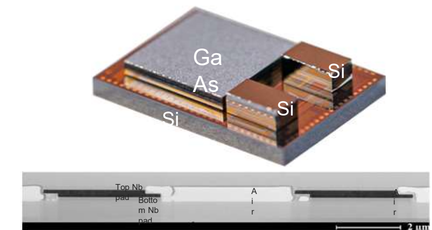
R01.1 – Ogi (Sony)
R01.2 – Gola (FBK)
P1.09 – Tashiro (Sony)
P1.10 – Wojtkiewicz (U. Edinburgh)
P2.08 – Leitner (onsemi)
P2.09 – Vachon (U. Sherbrooke)
R06.2 – Kappel (ams-OSRAM)
(… ?)

[34] E. Charbon, C. Bruschini & M.-J. Lee, ICECS 2018
[35] B. Aull et al., Lincol Lab J.; Vol 13, no. 2, pp. 335-350, 2002
[36] B. Aull et al., ISSCC 2006
[37] T. Al Abbas et al., IEDM 2016
[38] K. Ito et al., IEDM 2020

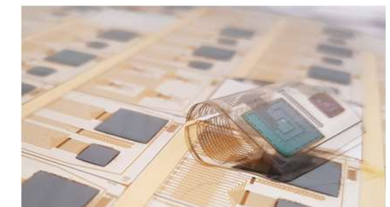
Take-home messages

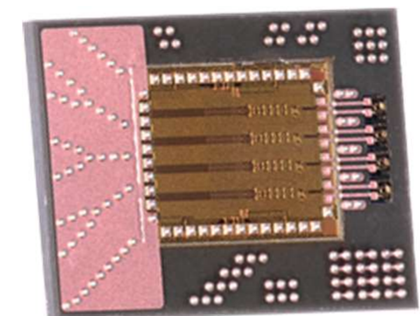
- **3D integration is far from a new idea!**
- **Imaging has played a pioneering role in the industrialization of these technologies: TSV, oxide & hybrid bonding**
- **It is now conceivable that any vertical architecture can be realized in one way or another. But… the right cost/performance compromise needs to be found**
- **Designers are often not fully aware of the technical toolbox available → come & discuss!**

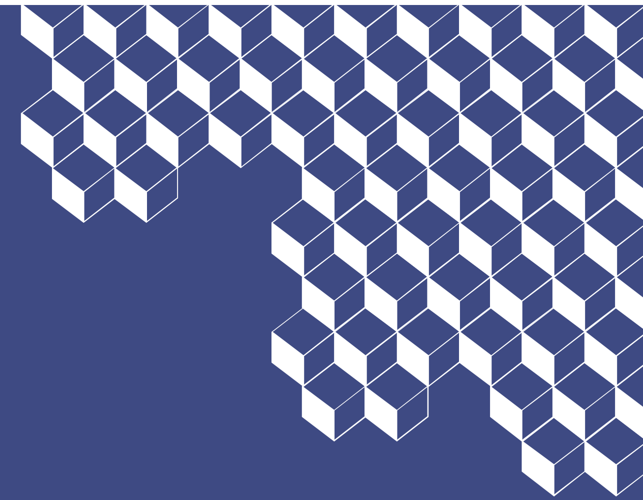

Chiplets on photonic interposer



Superconducting Nb/Nb bonding for quantum interposers


Flexible heterogeneous SiP


Optical transceiver



Thanks !

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