ISSW 2024

Invited Talk

CMOS Flash LiDAR Sensors with In-pixel Zoom Histogramming TDC Architectures

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ULSAN NATIONAL INSTITUTE OF SCIENCE AND TECHNOLOGY

SOLIDVUE

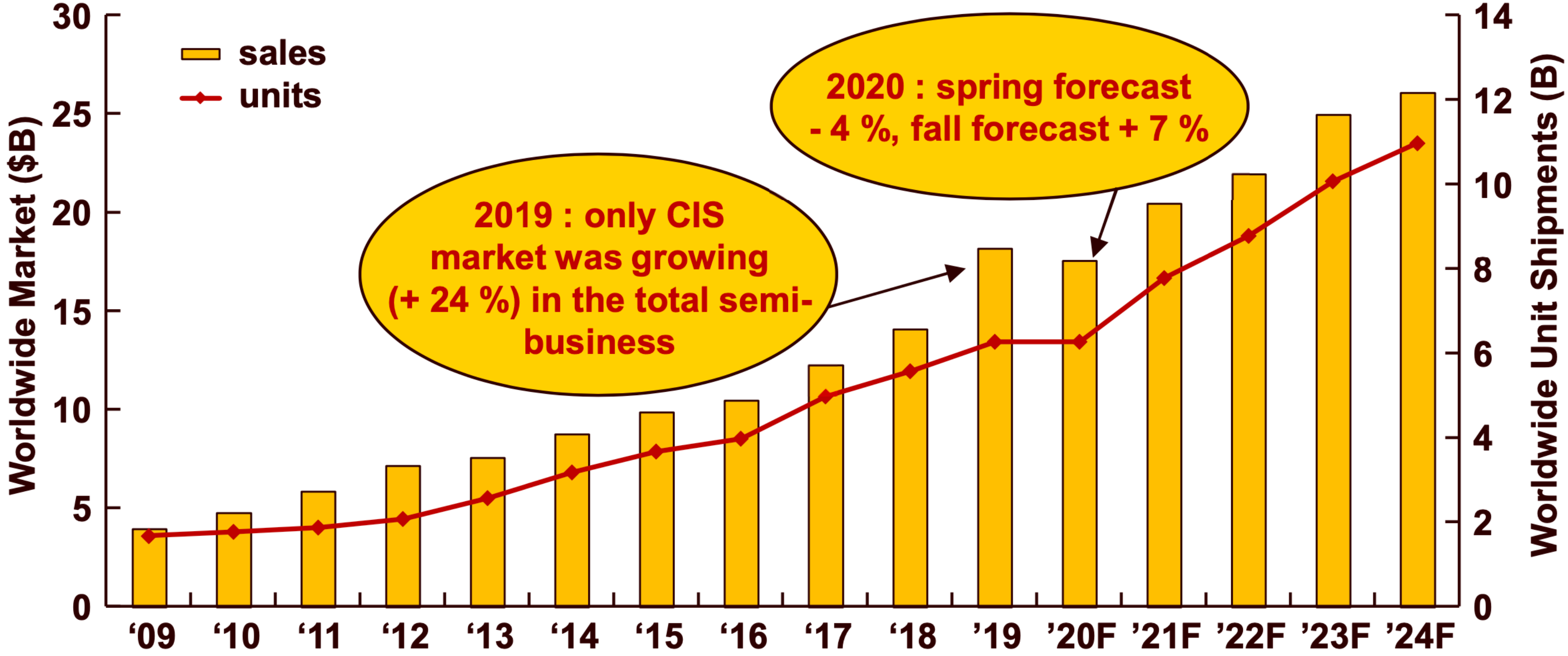
BIO INSPIRED ADVANCED SENSOR

Outline

- Introduction to LiDAR Sensors
- On-Chip Histogramming TDC Architecture
- Proposed In-pixel Histogramming TDCs w/ Measurement Results
  - Zoom hTDC Architecture
  - Quaternary Searching hTDC Architecture
  - Analog-Assisted SA hTDC
- Conclusions

Cameras in Our Life

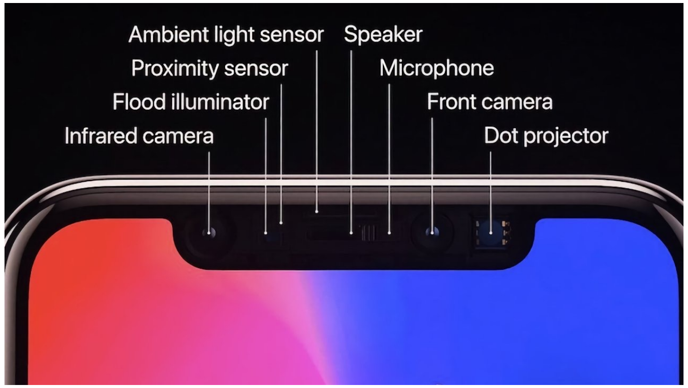
CIS Market

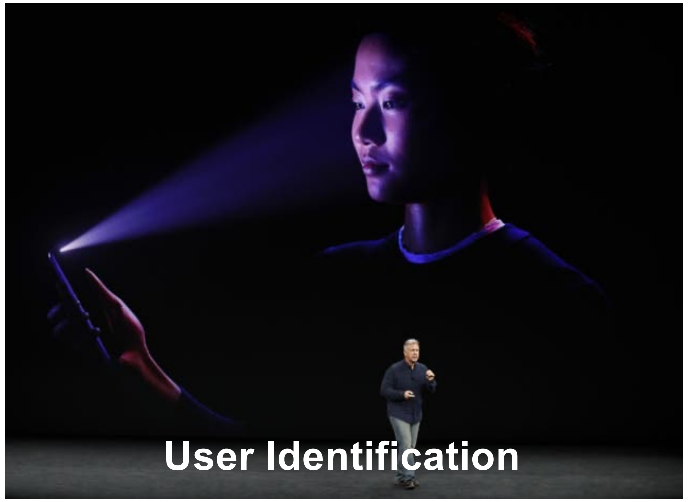


6.1B units in 2019 → 11B units in 2024!

A. Theuwissen, ISSCC 2021

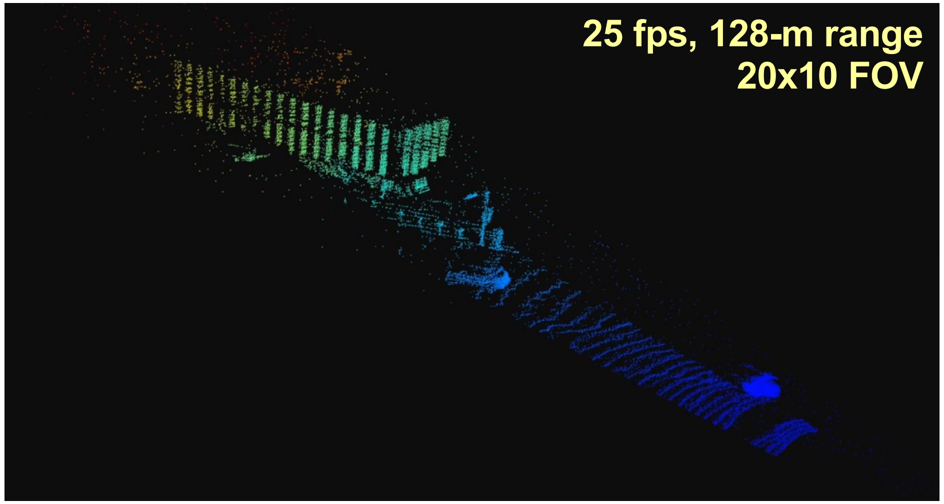
Emerging Application: Ranging

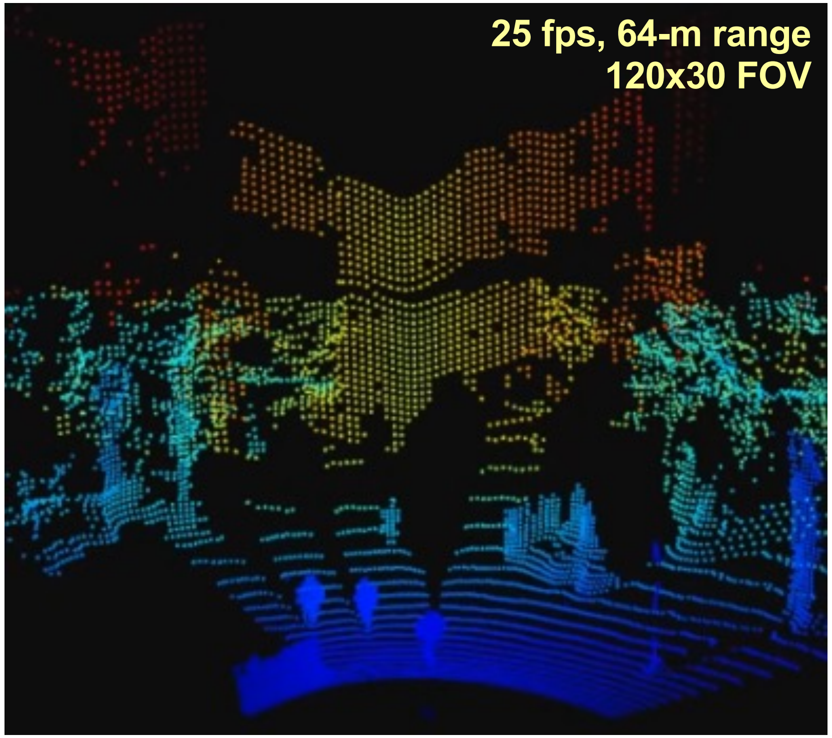


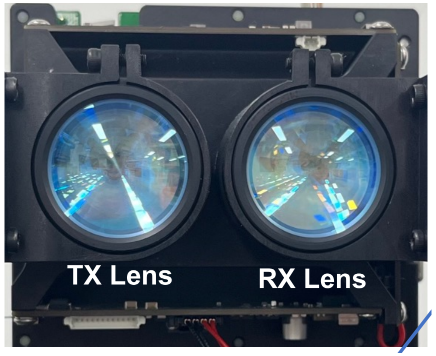


Ref: Apple

Ranging in Automotives



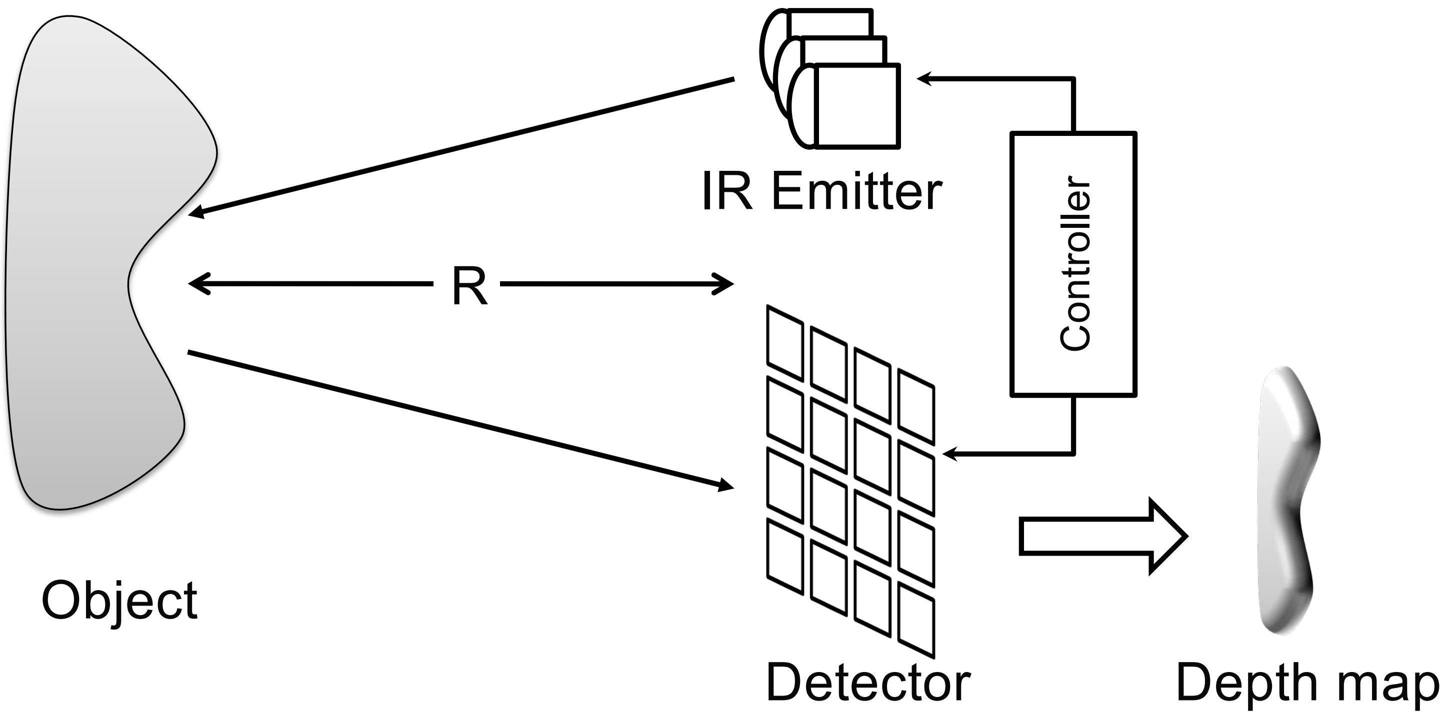




Solid-State LiDAR

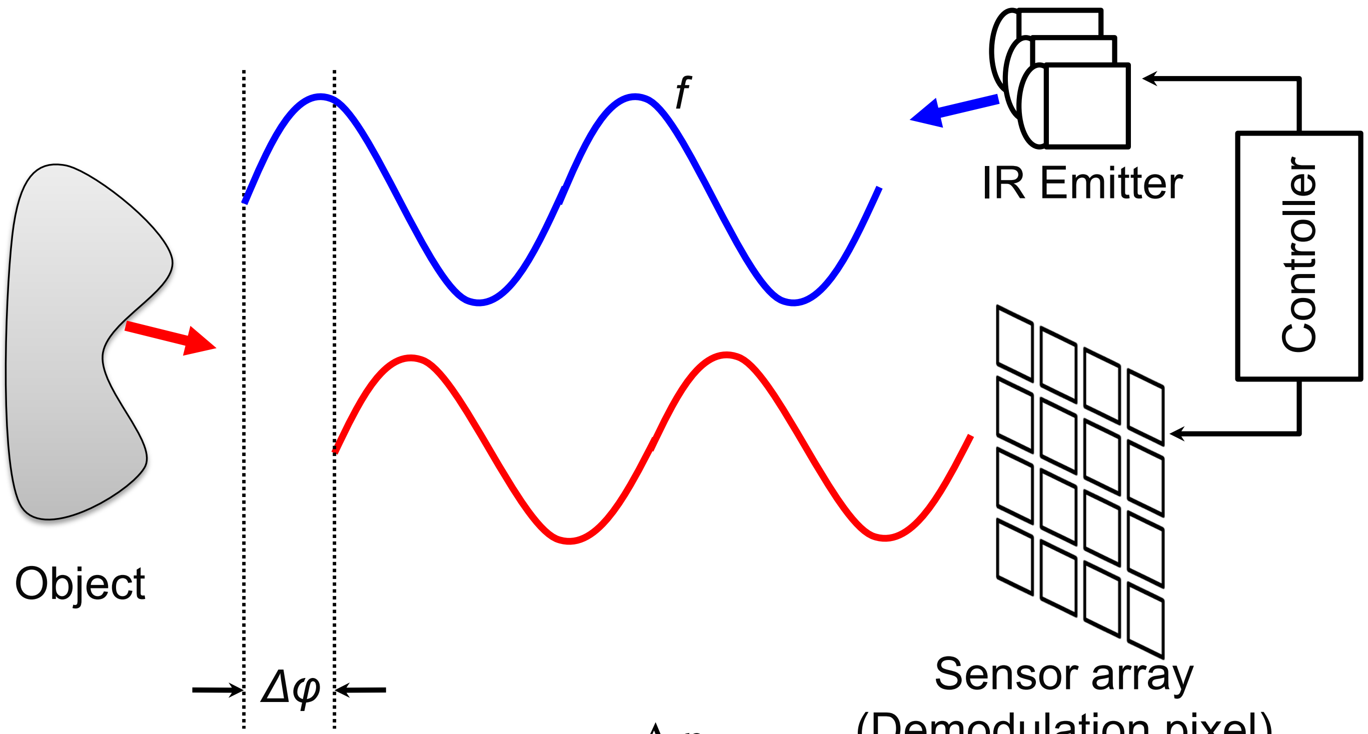
Ref: SolidVue (LiDAR Sensor)
SOSLAB (TX + Platform)

Time-of-Flight for LiDAR



- To measure the round-trip time of emitted light for acquiring the distance

Indirect Time-of-Flight (iToF)



$$D = \frac{c}{2}\frac{\Delta\varphi}{2\pi f}$$

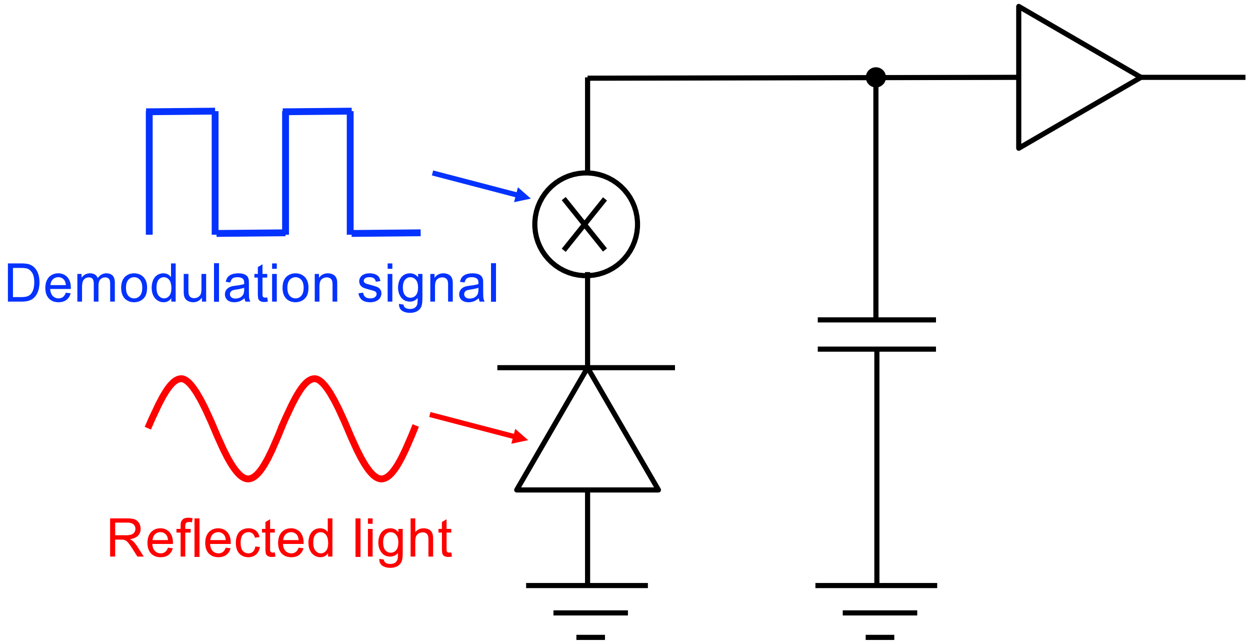
Detecting phase difference

Demodulation Concept

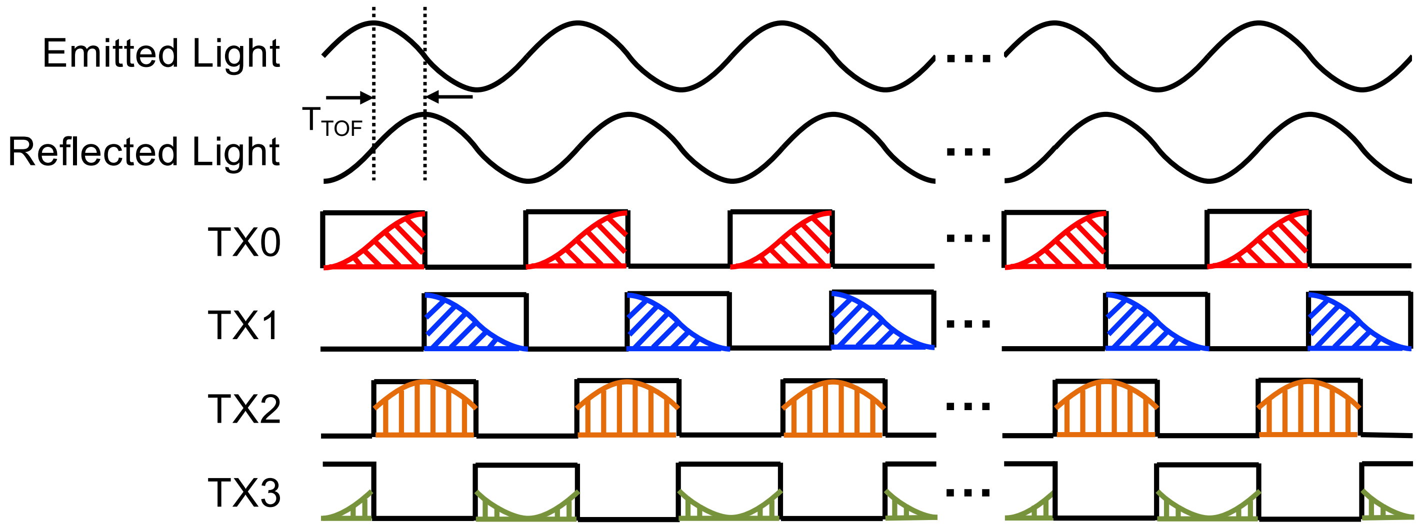
$$s(t) = Asin(\omega t - \Delta\varphi)$$
$$g(t) = sin\omega t$$

$$c(t) = s(t)\otimes g(t)$$
$$\frac{A}{2}[cos\Delta\varphi - cos(2\omega t - \Delta\varphi)]$$

LPF → DC extract



Phase Measurement



$$N_0 = ni_{ir}\int_0^{\pi}\left(a\sin(\theta - T_{TOF}) + a\right)d\theta = 2ni_{ir}a\left(\cos T_{TOF} + \frac{\pi}{2}\right)$$

$$N_1 = ni_{ir}\int_{\pi}^{2\pi}\left(a\sin(\theta - T_{TOF}) + a\right)d\theta = 2ni_{ir}a\left(-\cos T_{TOF} + \frac{\pi}{2}\right)$$

$$N_2 = ni_{ir}\int_{\frac{\pi}{2}}^{\frac{3\pi}{2}}\left(a\sin(\theta - T_{TOF}) + a\right)d\theta = 2ni_{ir}a\left(\sin T_{TOF} + \frac{\pi}{2}\right)$$

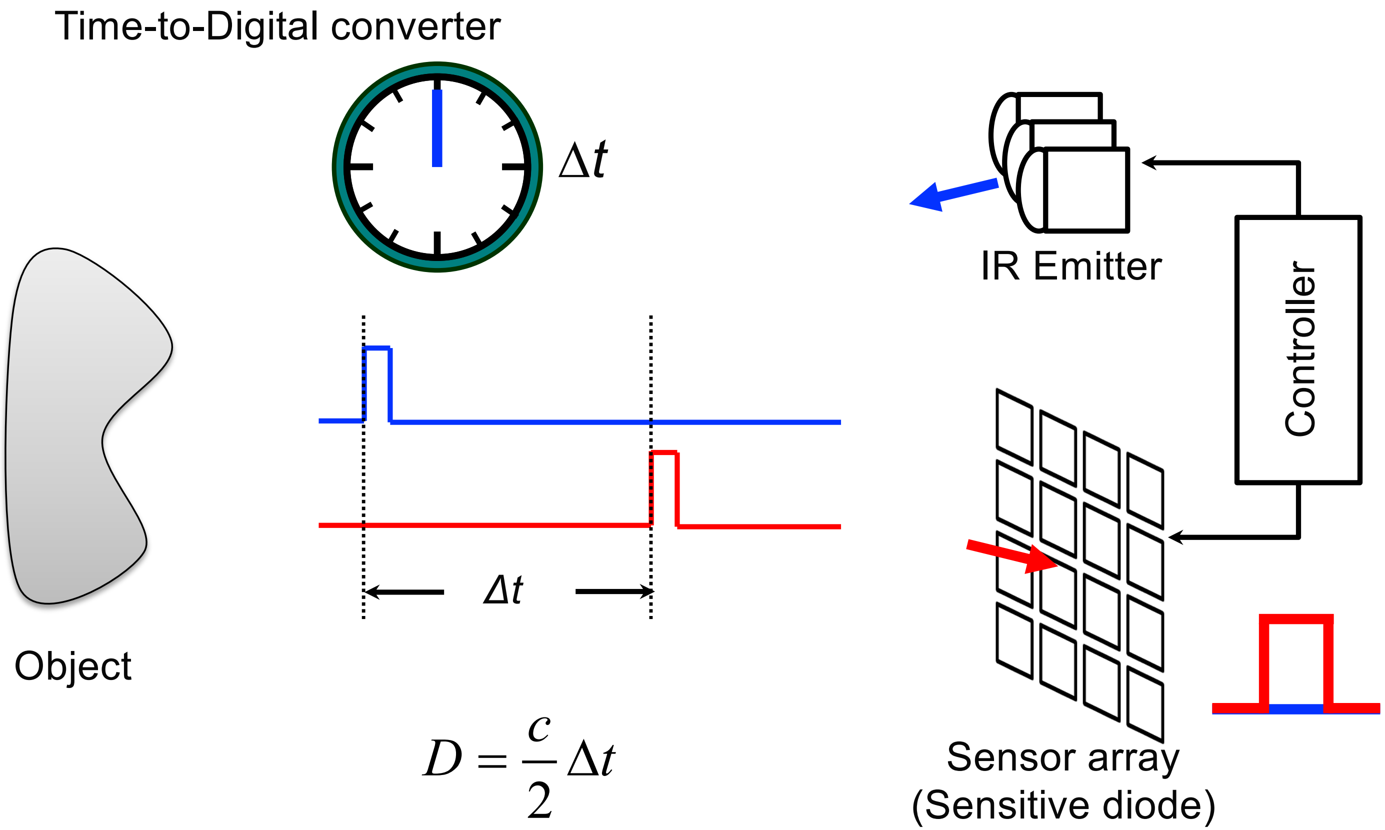
$$N_3 = ni_{ir}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}}\left(a\sin(\theta - T_{TOF}) + a\right)d\theta = 2ni_{ir}a\left(-\sin T_{TOF} + \frac{\pi}{2}\right)$$

$$\Rightarrow \frac{N_2 - N_3}{N_0 - N_1} = \frac{\sin T_{TOF}}{\cos T_{TOF}} = \tan T_{TOF}$$

$$\Rightarrow T_{TOF} = \arctan\left(\frac{N_2 - N_3}{N_0 - N_1}\right)$$

$$\therefore R = \frac{c}{4\pi f}T_{TOF} = \frac{c}{4\pi f}\arctan\left(\frac{N_2 - N_3}{N_0 - N_1}\right)$$

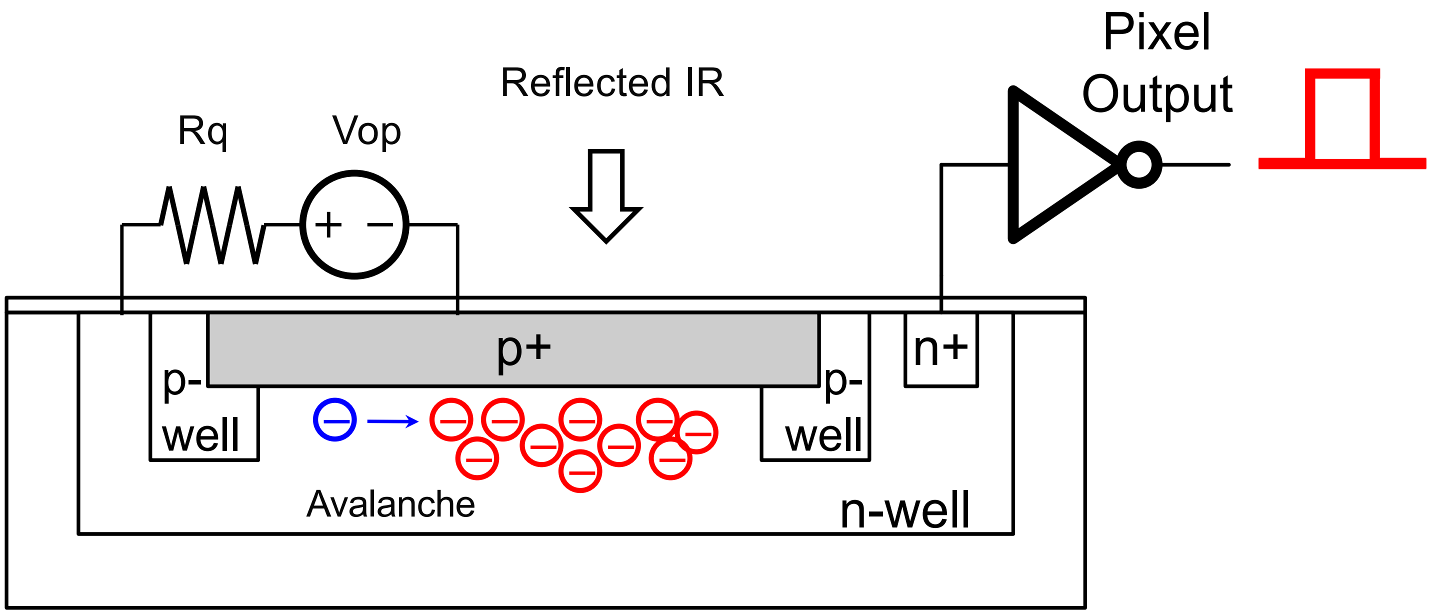
Direct Time-of-Flight (dToF)



$$D = \frac{c}{2}\Delta t$$

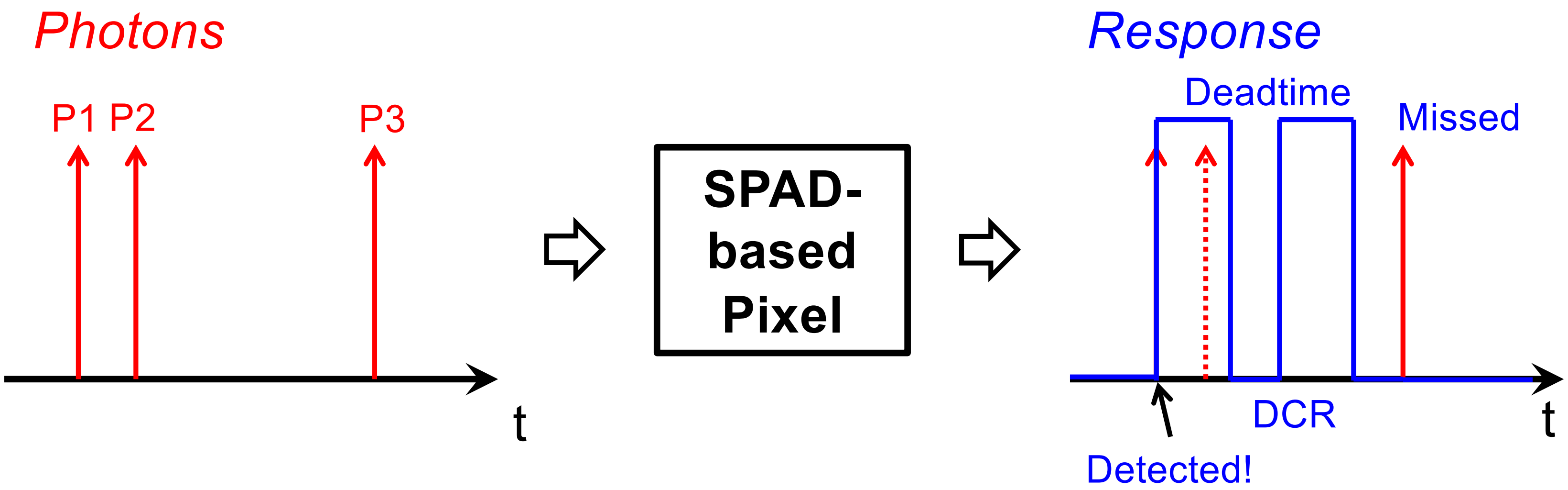
Detecting direct time difference

Single Photon Avalanche Diode (SPAD)



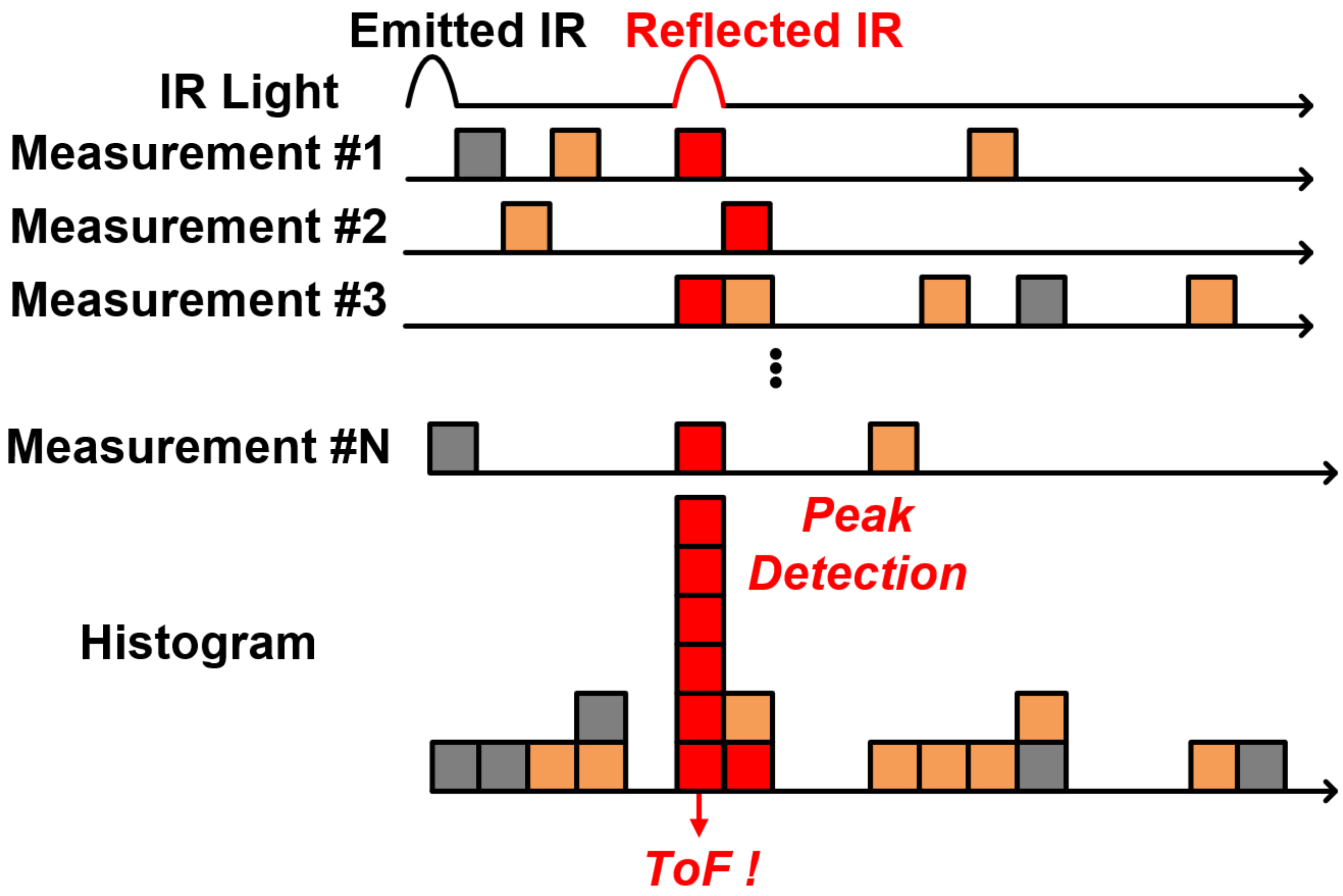
- Geiger mode operation (virtually infinite gain)
  → Possible to detect a single photon
- Digital output interface (pulse generation)

SPAD High Level Behavior



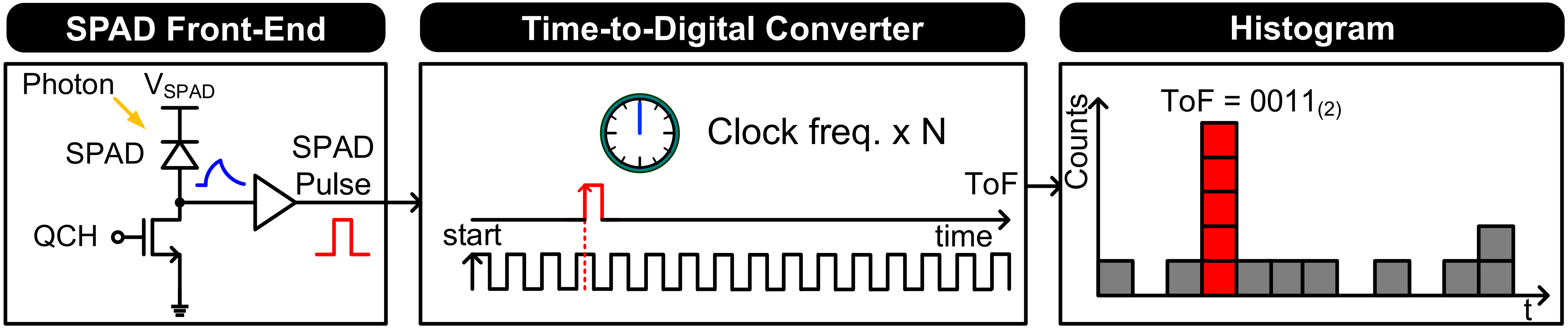
- Detected photons generate digital pulses.
- Not all the photons are detected (PDP).
- Pulses can also be generated in the dark (DCR).
- Jitter noise should be added.

Time-Correlated Single Photon Counting



- Repeat and histogram ToF measurements.
- Finally, a peak value is detected as the ToF.

Block Diagram of SPAD-Based LiDAR



Detecting photons

Converting arrival time of SPAD pulse to digital bit

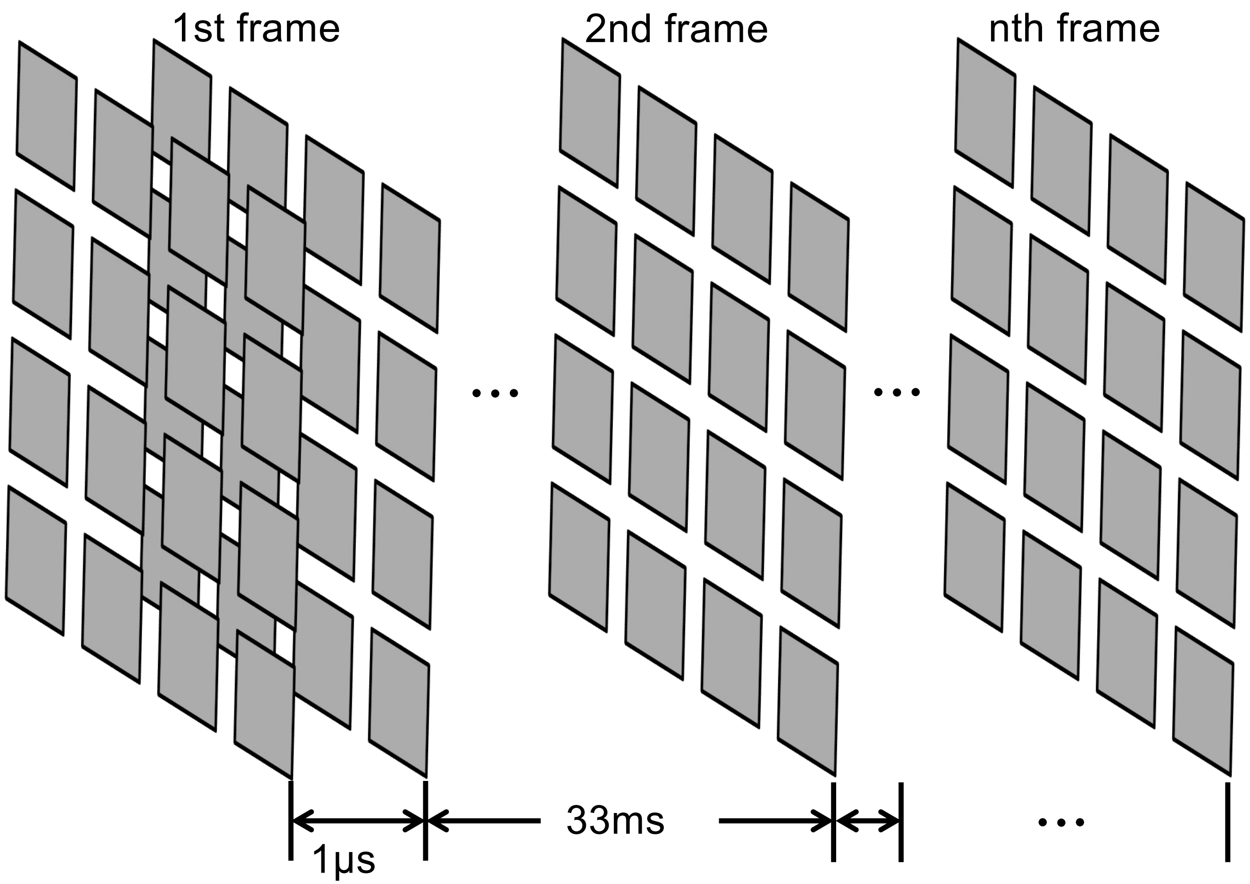
Extracting the peak value (ToF)

Distance

$(Distance = \frac{c}{2}\Delta t)$

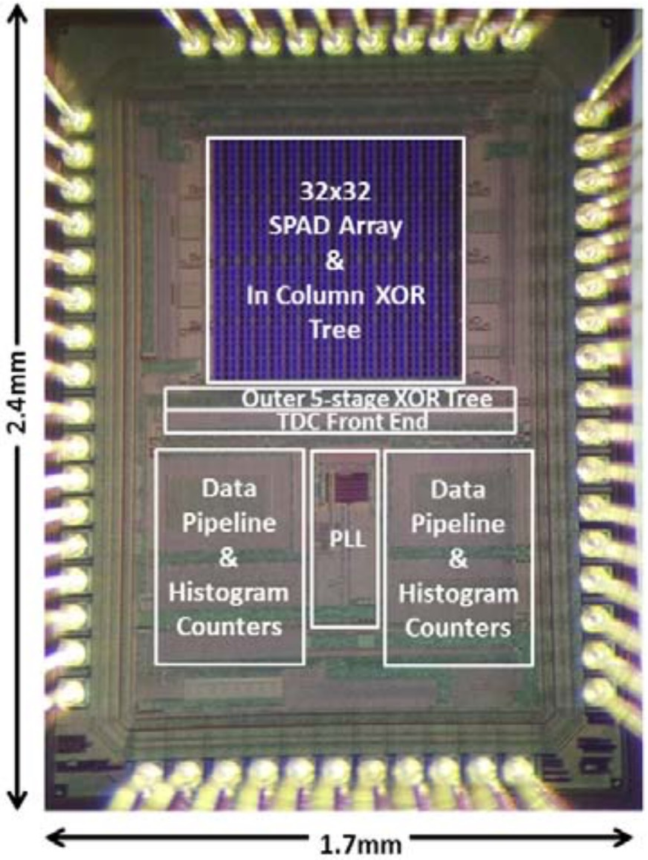
How many ToFs are generated?

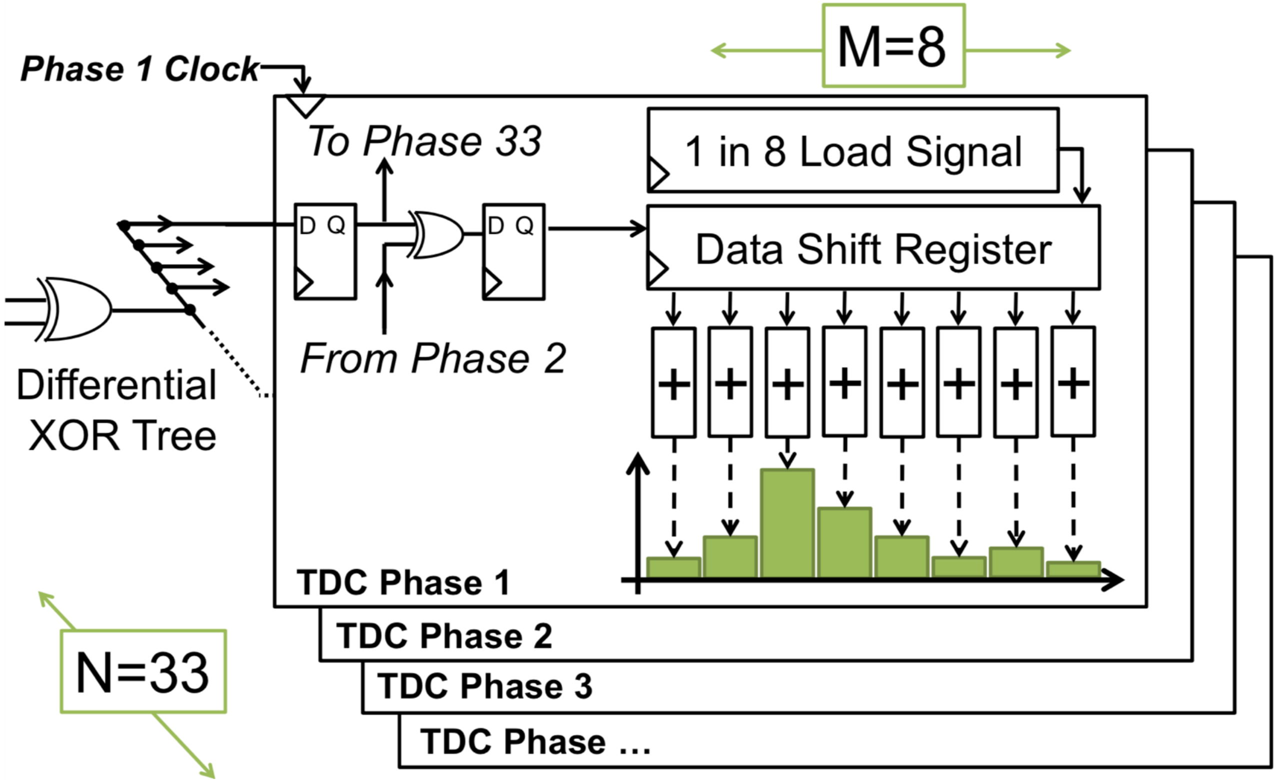
Data Rate of Flash dToF



- Assumption
  - Resolution: 160×120
  - Frame rate: 30fps
  - TDC: 10b
  - Repetition: 1MHz
  - Synchronous readout
- Data rate
  =160×120×10b×1M
  =**192Gbps!!**

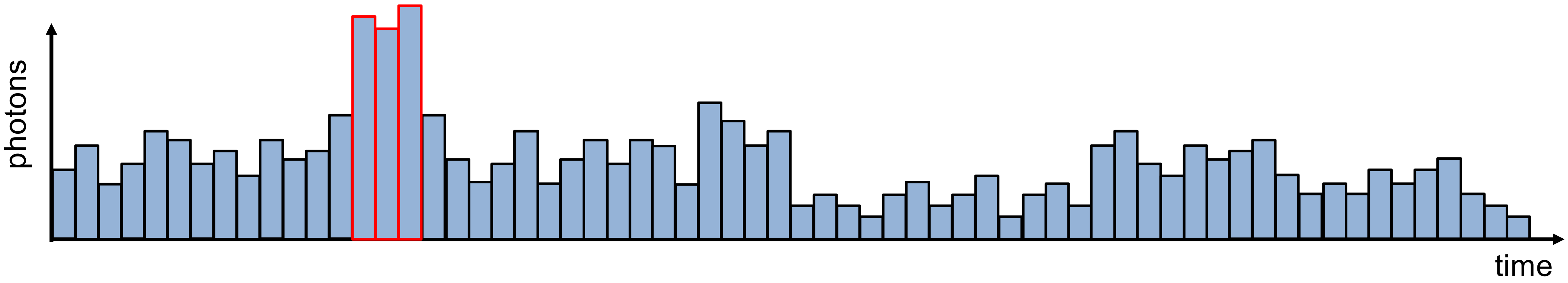
On-Chip Histogramming TDC (hTDC)





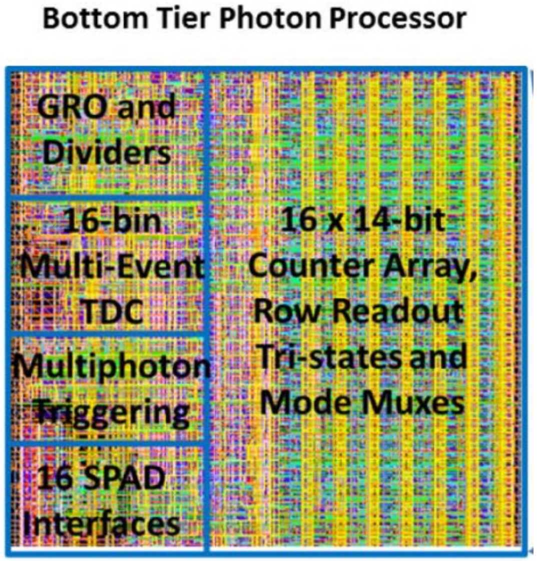
N. Dutton, ISSCC 2015

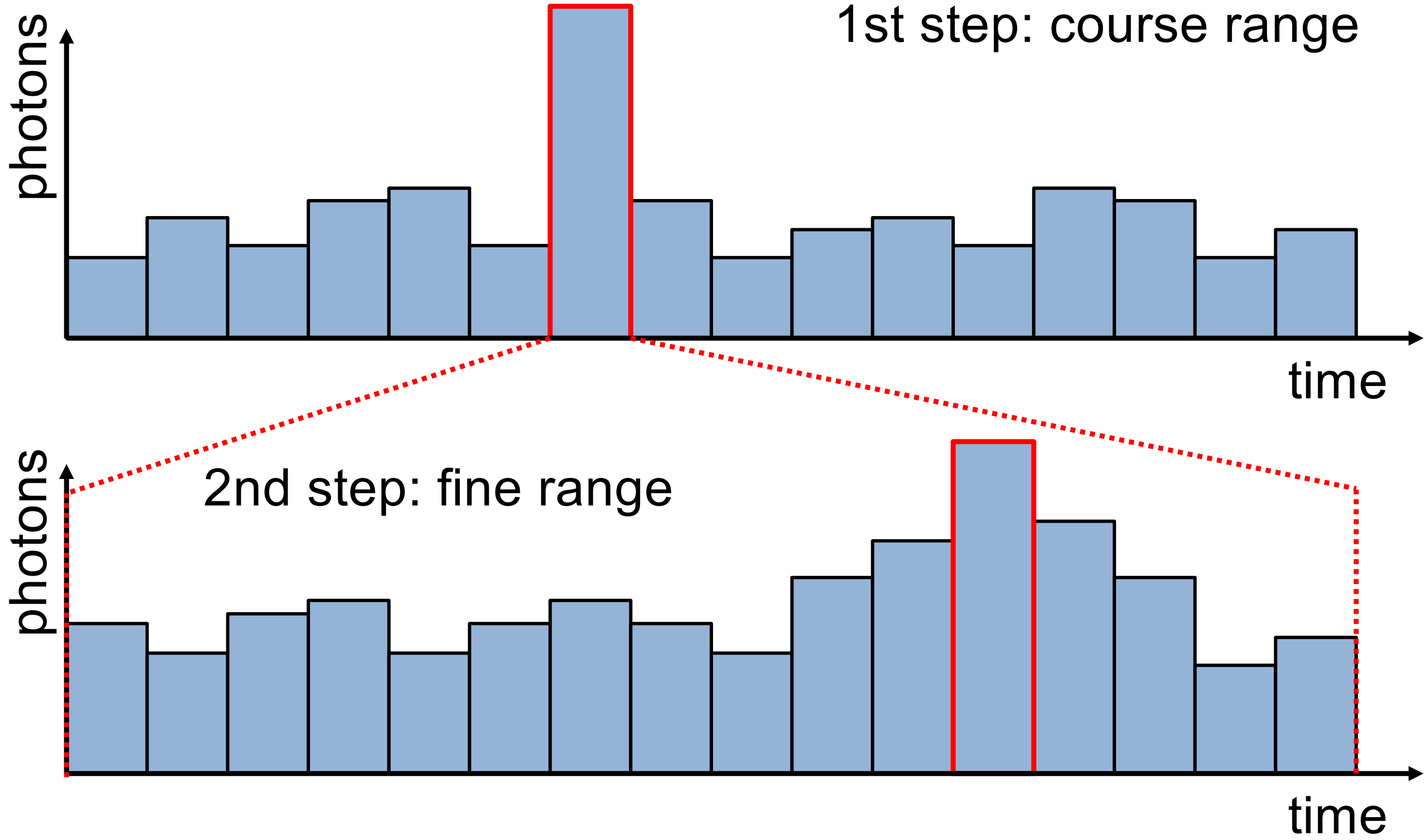
One-Step Histogram



- Each bin has a corresponding counter to accumulate responses.
- Intuitive operation and possible to capture multi-echo simultaneously.
- Large memories are required. (# of counters = # of time bins)
- Suitable for column-parallel or single TDC architecture.

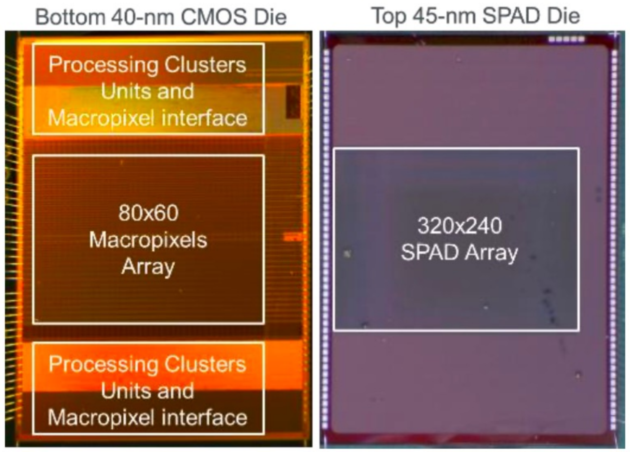
Two-Step Histogram

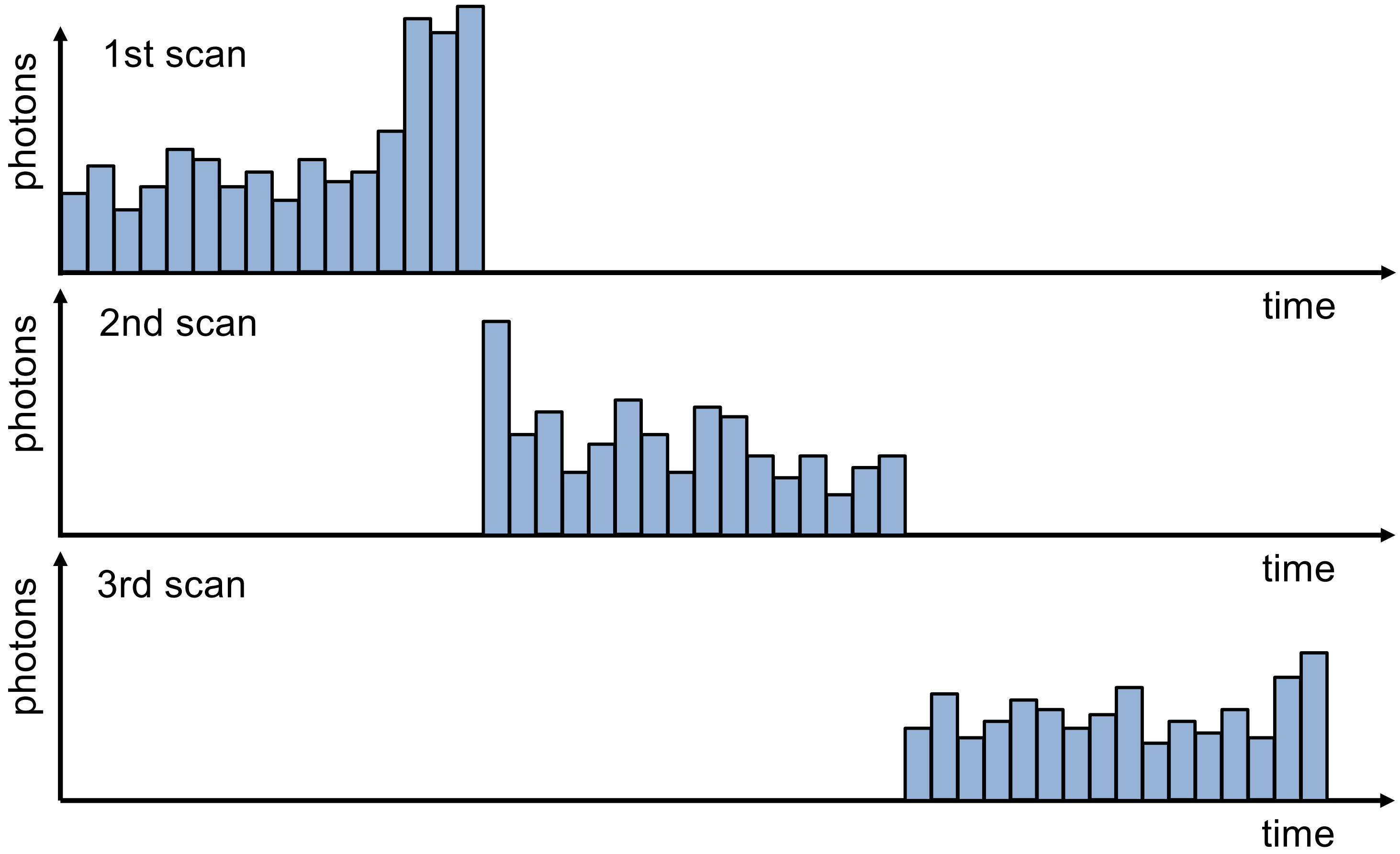




S. Hutchings, JSSC 2019

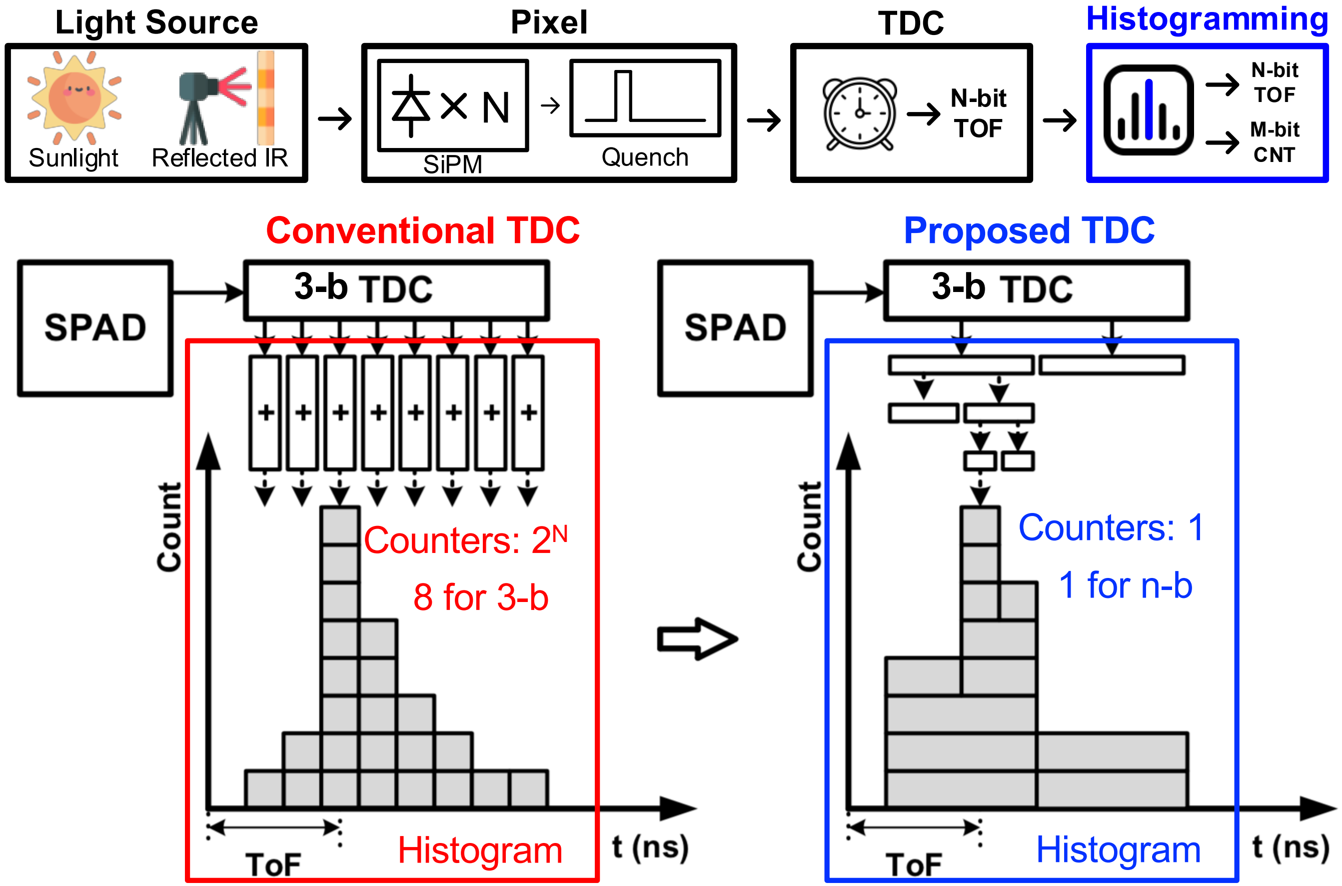
Histogram Scanning





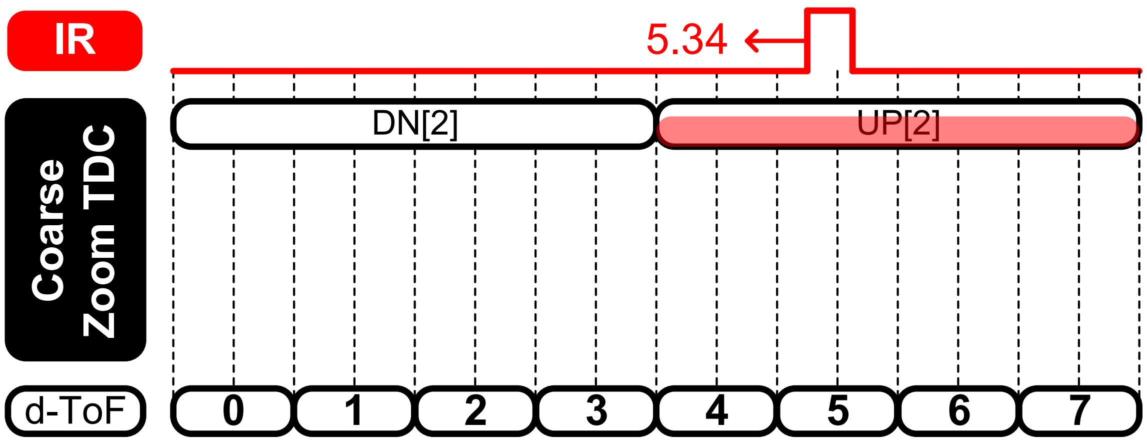
D. Stoppa, IISW 2021

SA hTDC Architecture



B. Kim, ISSCC 2021

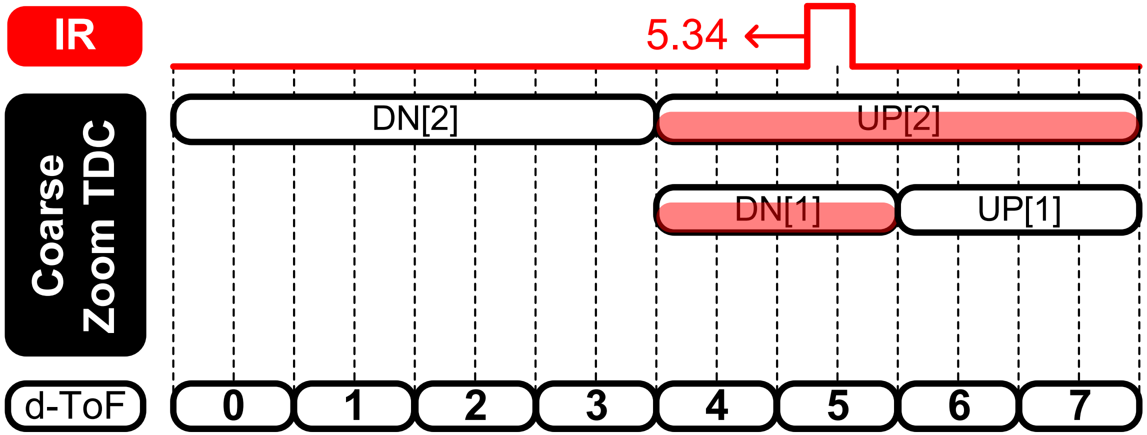
Operating Principles [1/4]



Start ToF=000

DN<UP → ToF=100

Operating Principles [2/4]

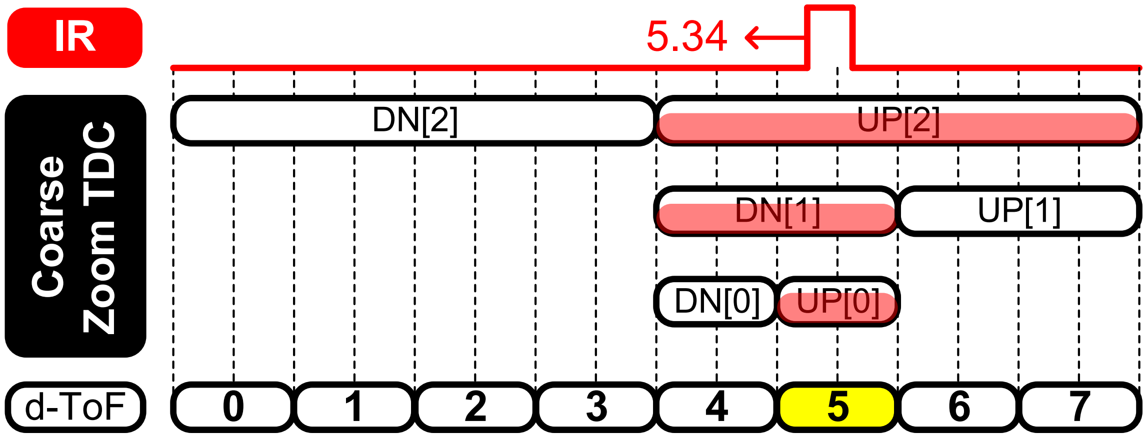


Start ToF=000

DN<UP → ToF=100

DN>UP → ToF=100

Operating Principles [3/4]



Start ToF=000

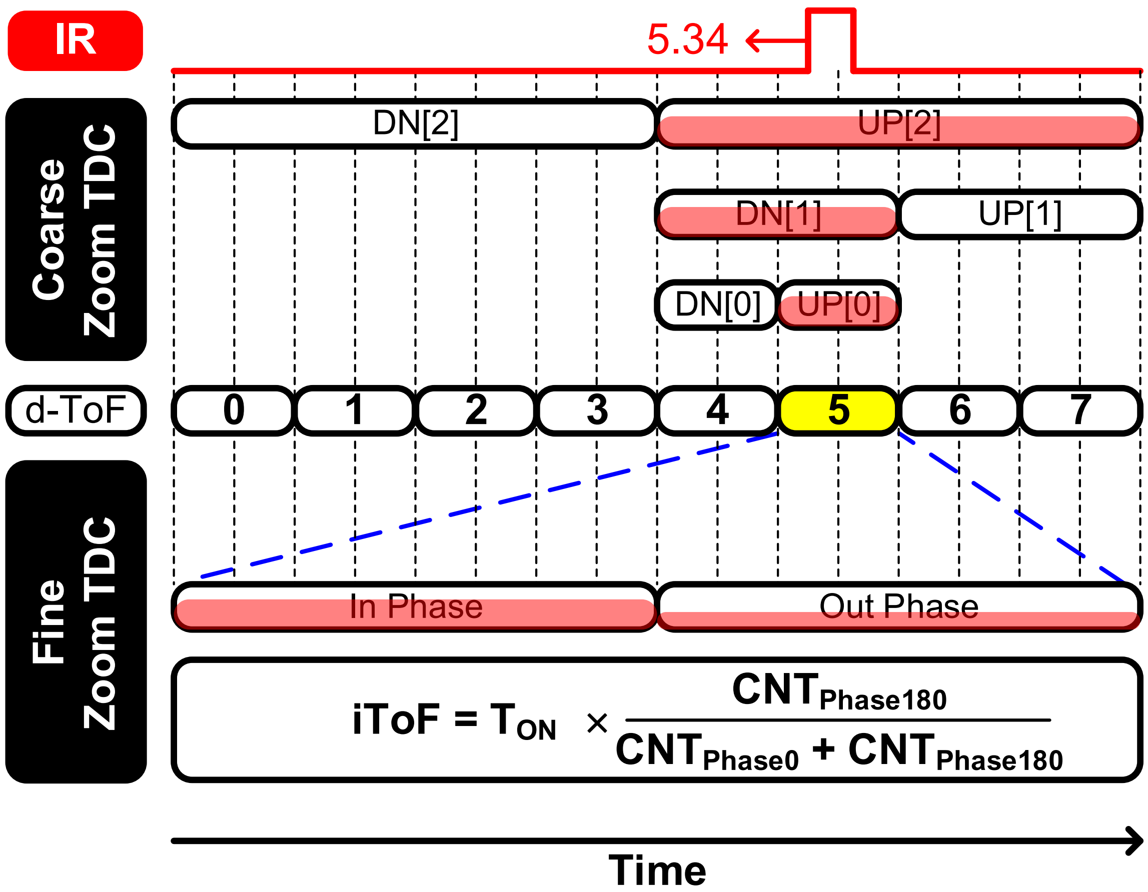
DN<UP → ToF=100

DN>UP → ToF=100

DN>UP → ToF=101

Coarse ToF = 5

Operating Principles [4/4]



Start ToF=000

DN<UP → ToF=100

DN>UP → ToF=100

DN>UP → ToF=101

Coarse ToF = 5

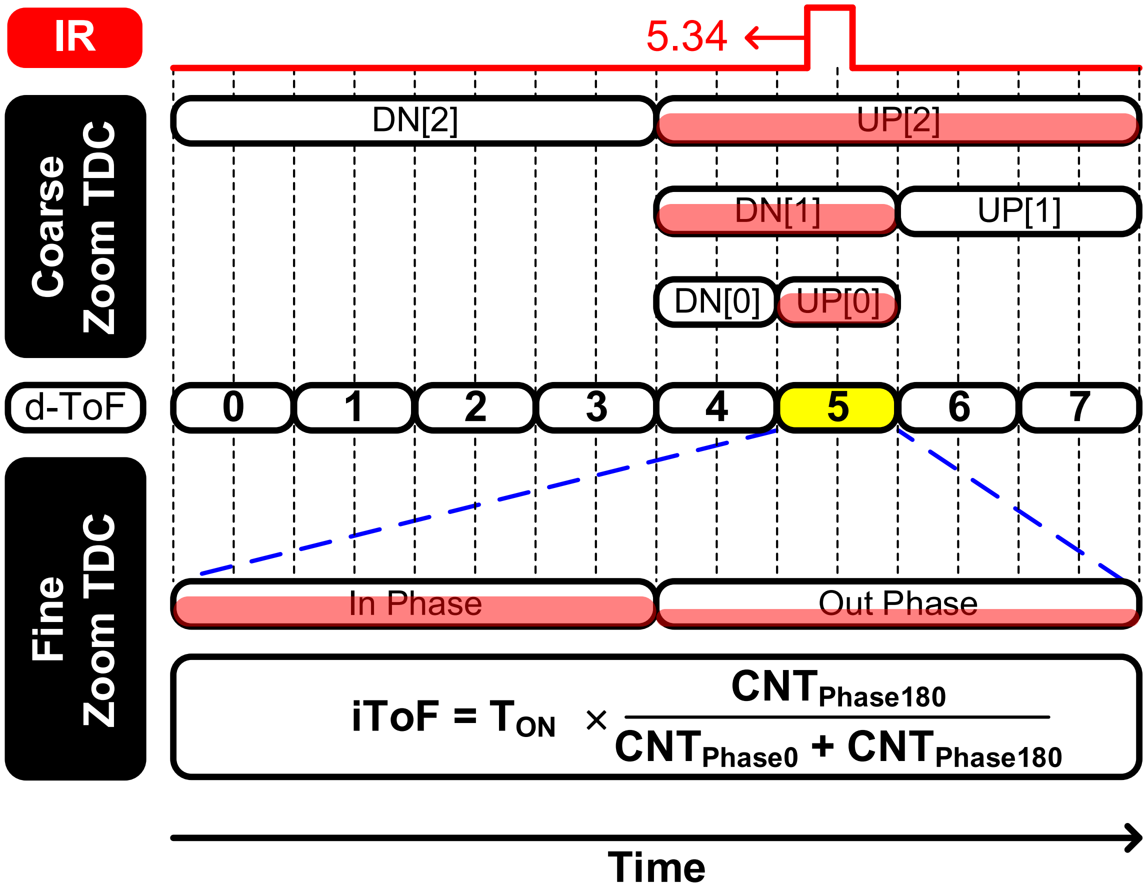
In-phase = 101100010

Out-of-phase=010110101

Fine ToF = 0.34

ToF = 5.34

Two-Step Zoom hTDC



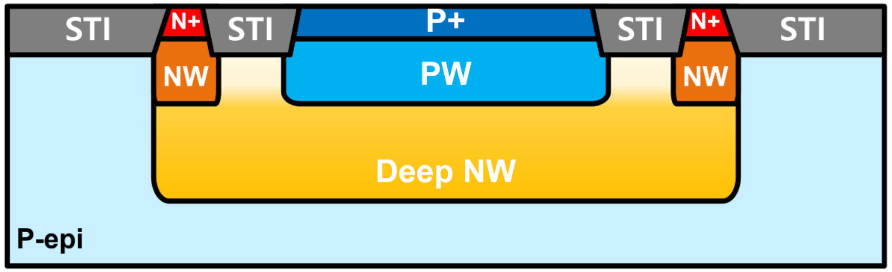
SAR coarse TDC

+

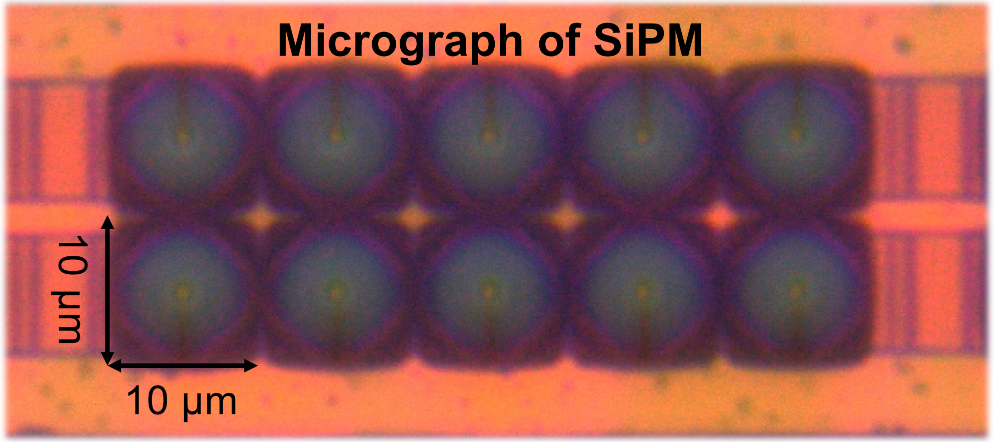
iToF fine TDC

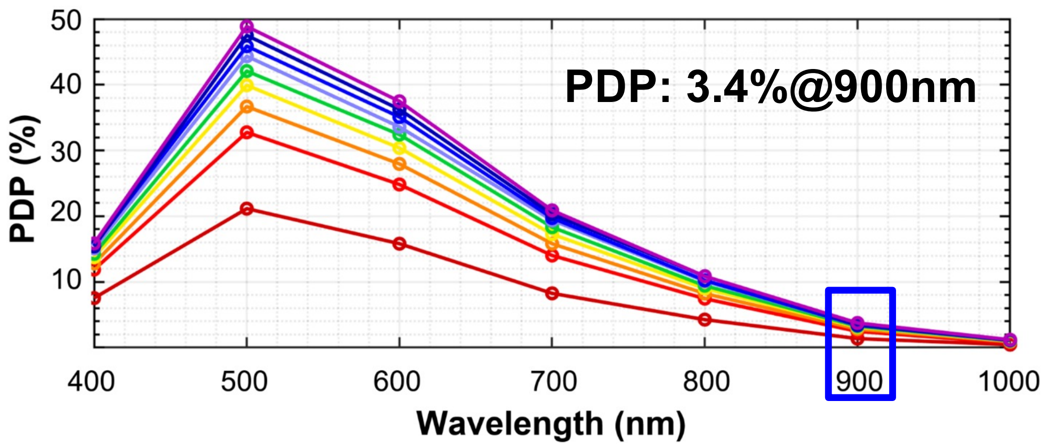
SPAD Design

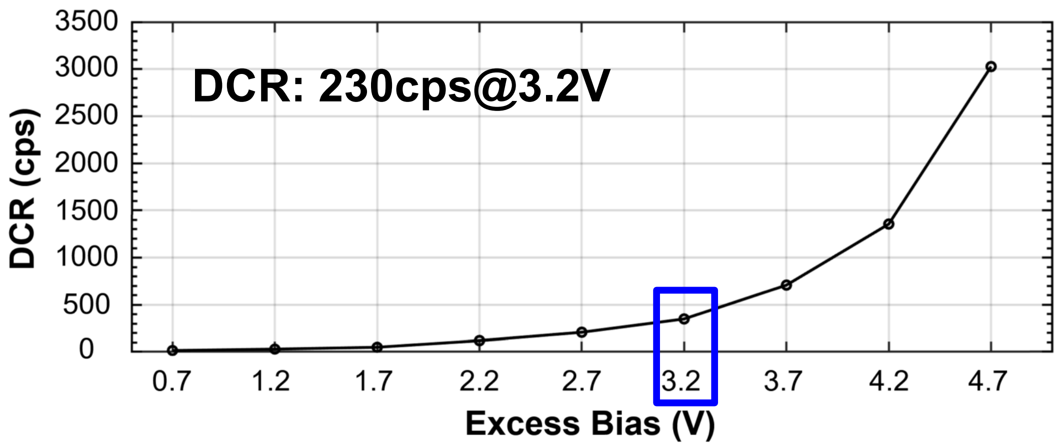
SPAD Structure (110nm FSI)



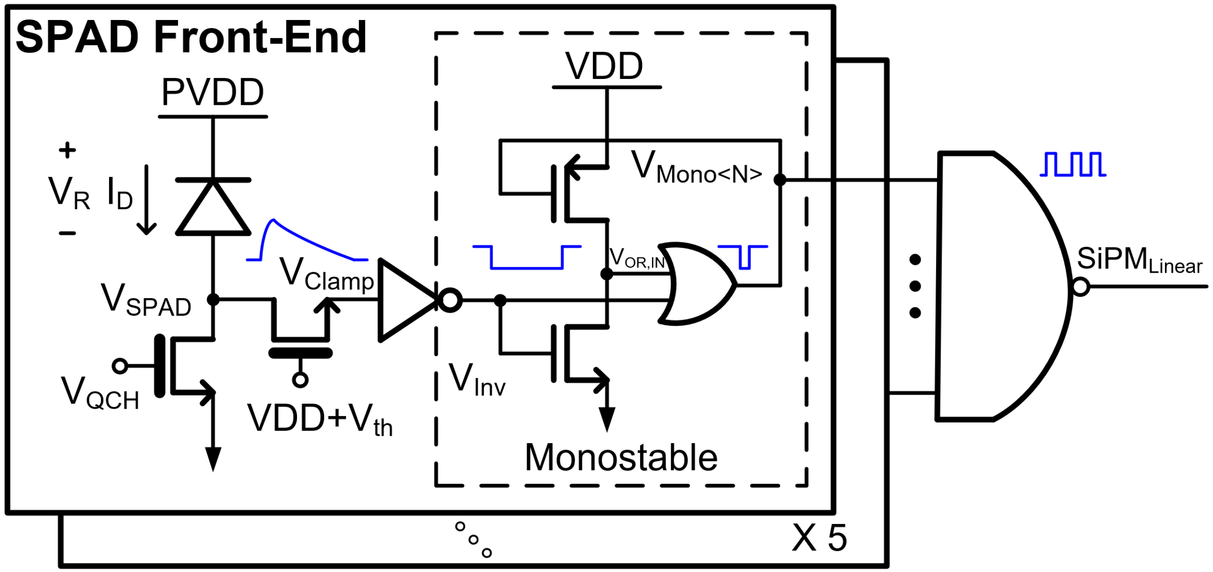
Junction of P-well/Deep N-well

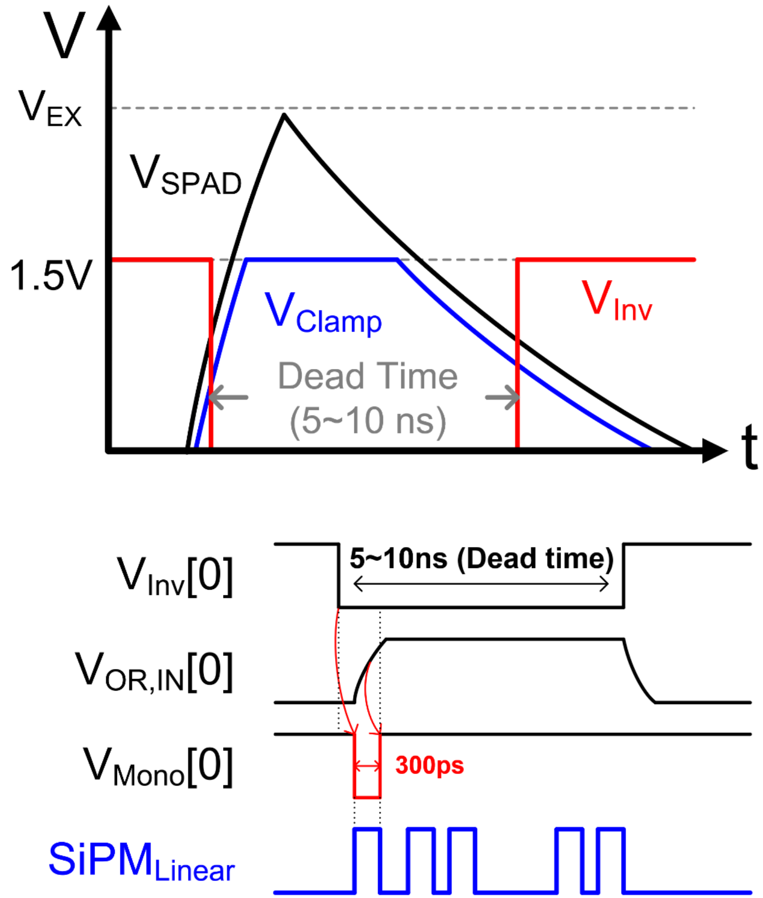






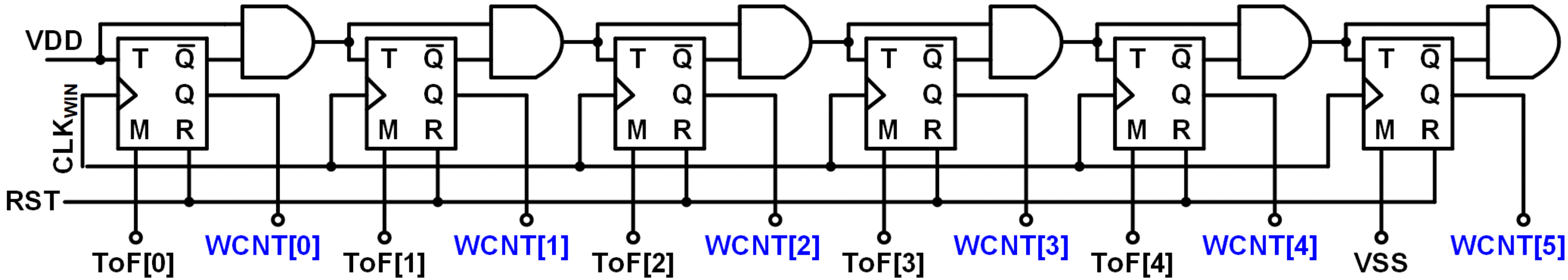
SPAD Front-End

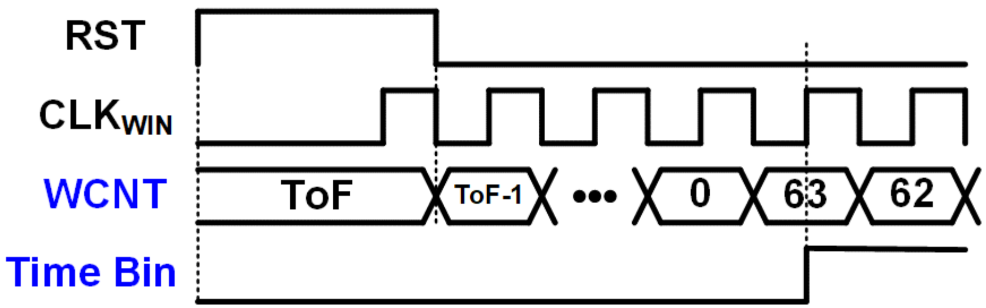




- Passive quenching/recharging circuit
- Multiple SPADs for coincidence detection
- Monostable circuit for serialization

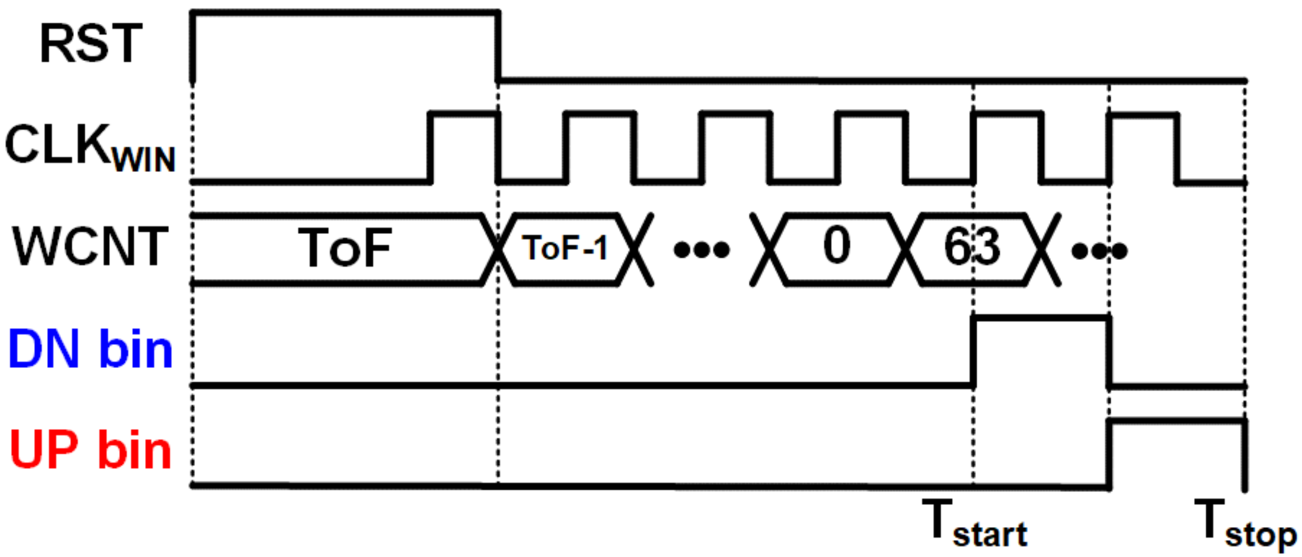
Window Generator





- Window generator creates a time-gate window, which filters the SPAD pulses.
- It governs the duration and location of the time bin depending on the previous ToF value.
- All T-FFs are reset to the ToF value.

Time Bin Generation

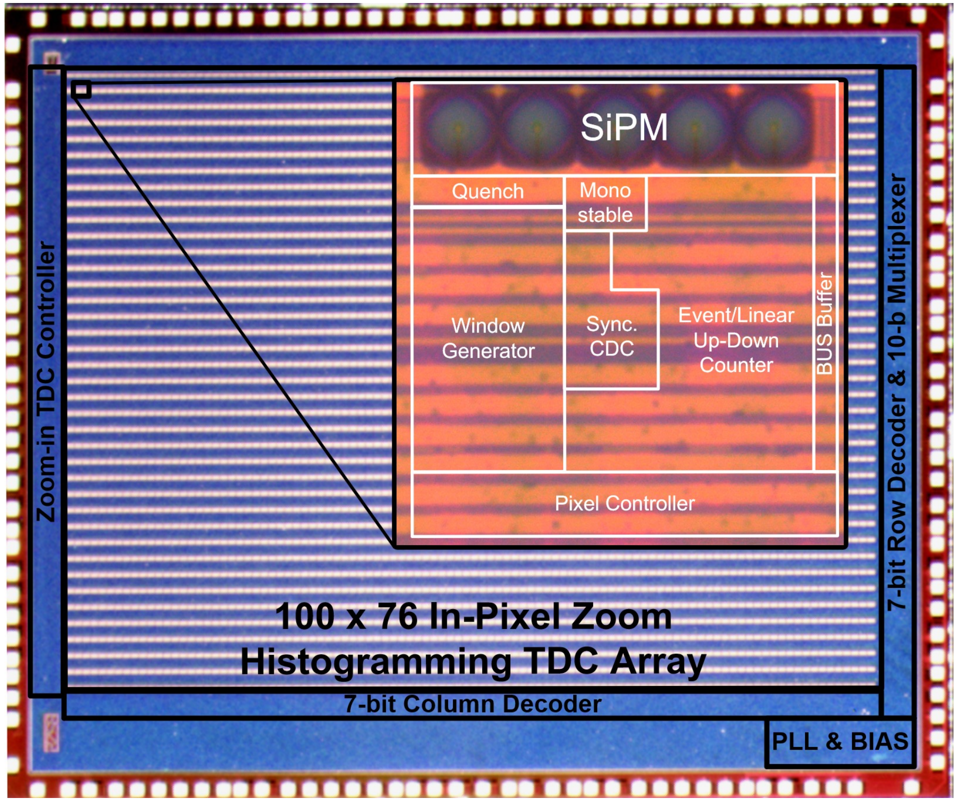


$$T_{start} = \begin{cases} 0 & , k = 1 \\ \sum_{i=2}^{k} 2^{N-i+1} \times ToF[N-i+1] & , k > 1 \end{cases}$$

N: TDC resolution
k: Present coarse step

$$T_{stop} = T_{start} + 2^{N-k+1}, WCNT[N-k]$$

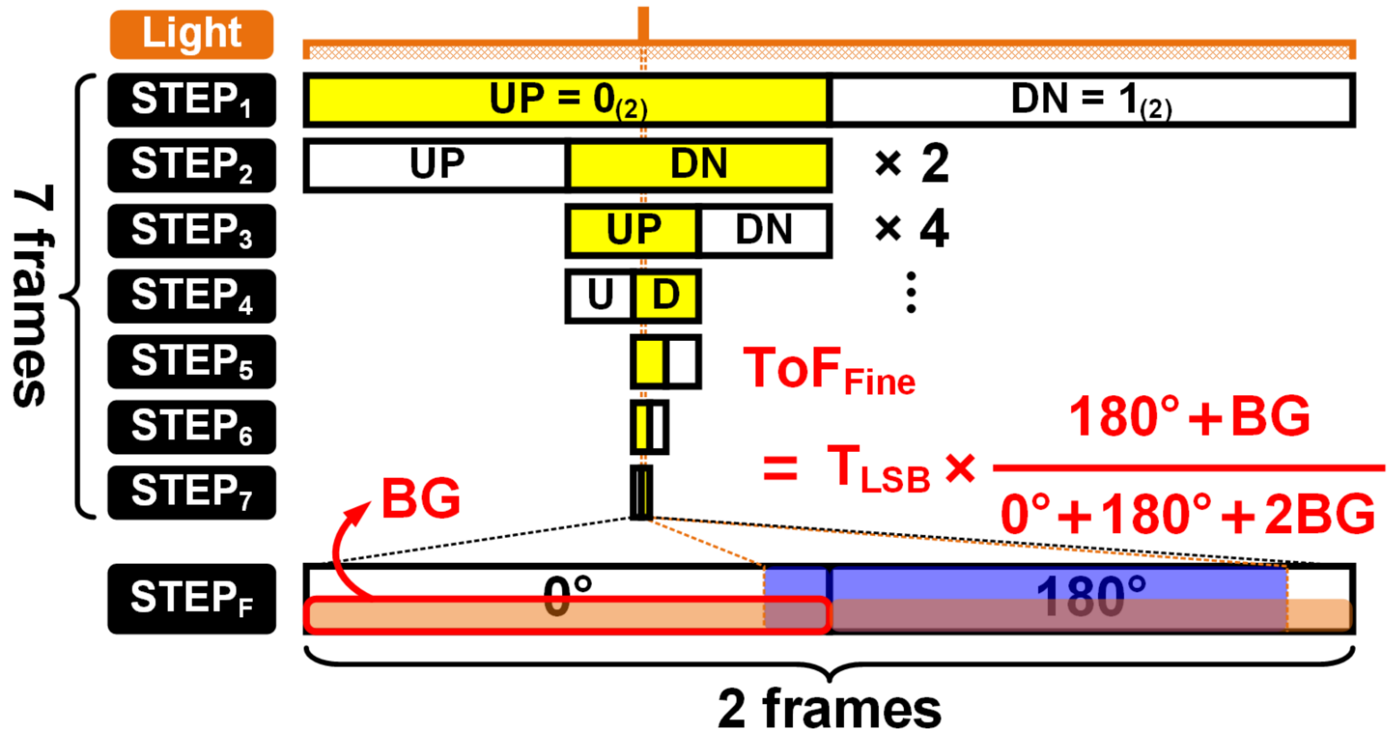
Chip Photograph



- Fabricated in 110nm BSI
- 5 SPADs per pixel
- Chip size: 7.03 × 5.9mm^2
- Pixel pitch: 60 µm
- Spatial resolution: 100 × 76
- TDC resolution: 5 ns / 300 ps

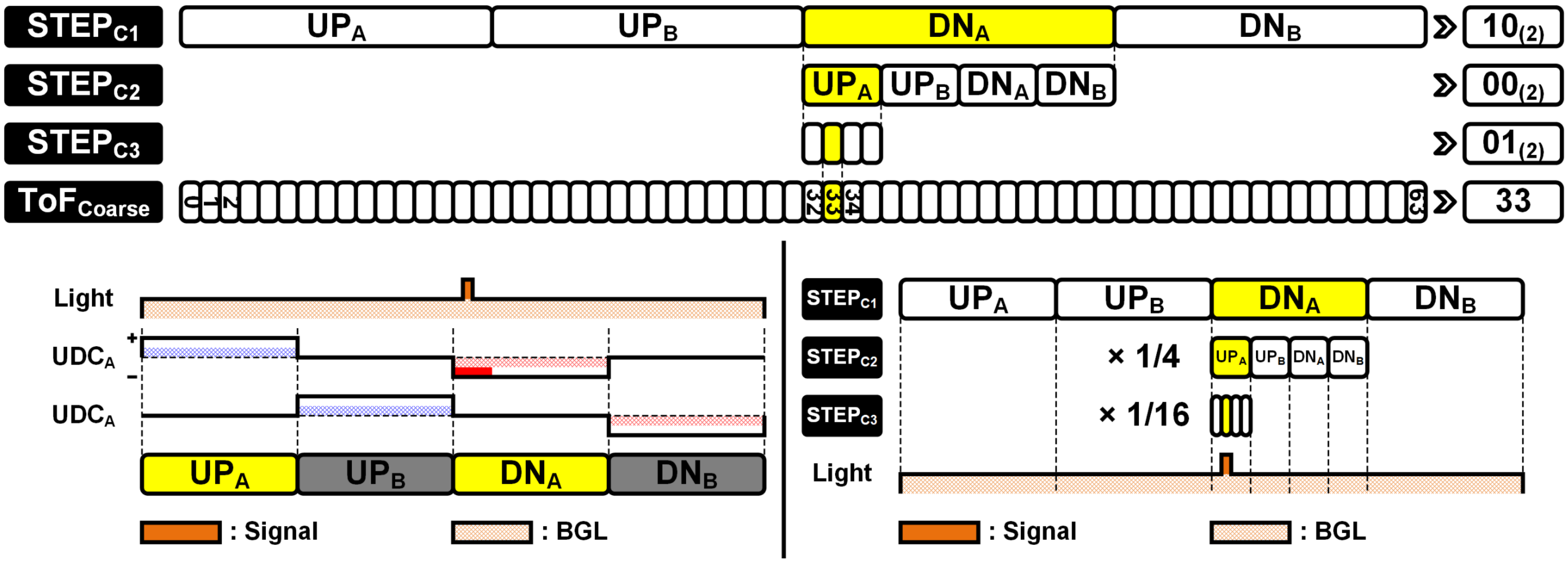
Under review

Issues in Zoom hTDC Architecture



- Synthesis of 9 sub-frames: low frame rate, motion artifact
- Low signal to background ratio (SBR)
- Slow SBR improvement
- Phase detection error by background light
  → Need to have another background sub-frame

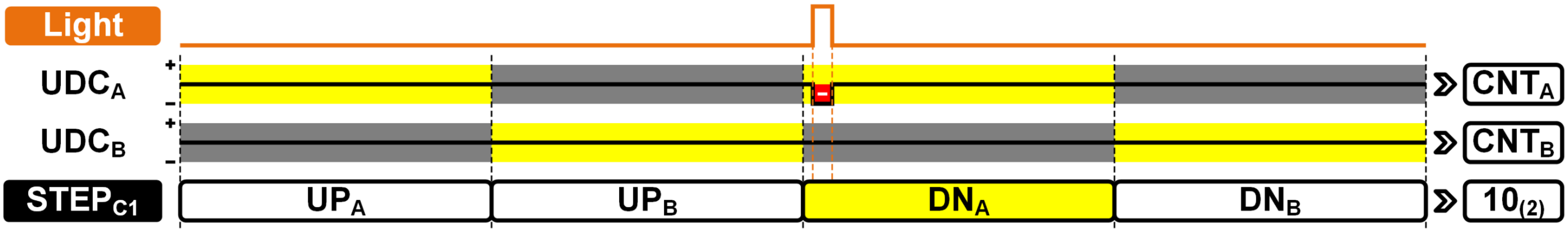
Quaternary Search hTDC

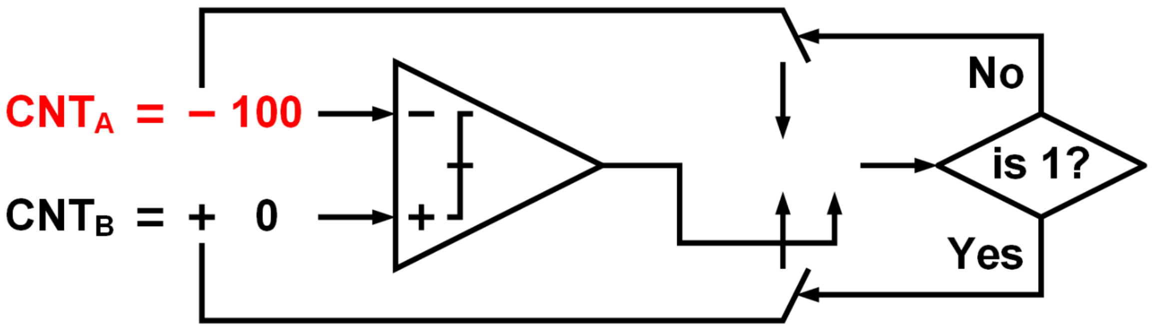


- The whole range is divided by four.
- UP and DN bins are compared to determine ToF[MSB].
- Either counter A or B determines ToF[MSB-1].

S. Park, ISSCC 2022

Quaternary Searching Algorithm [Step 1]

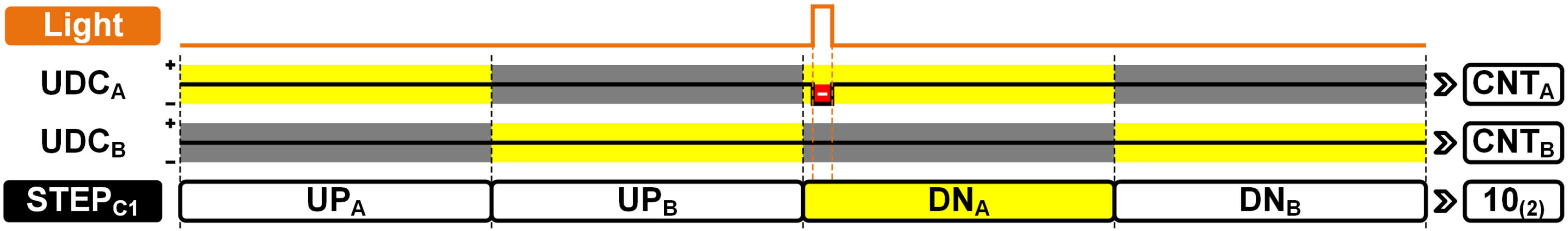


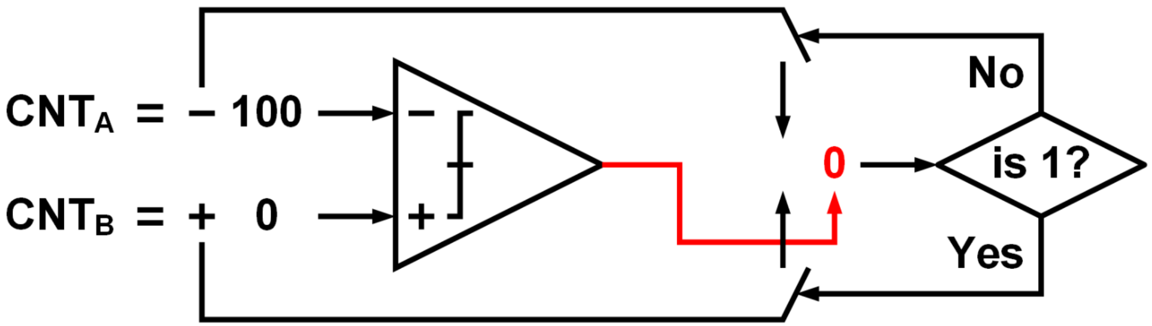


$|CNT_B| > |CNT_A|$? → Lower bit

Sign of winner? → Upper bit

Quaternary Searching Algorithm [Step 1]

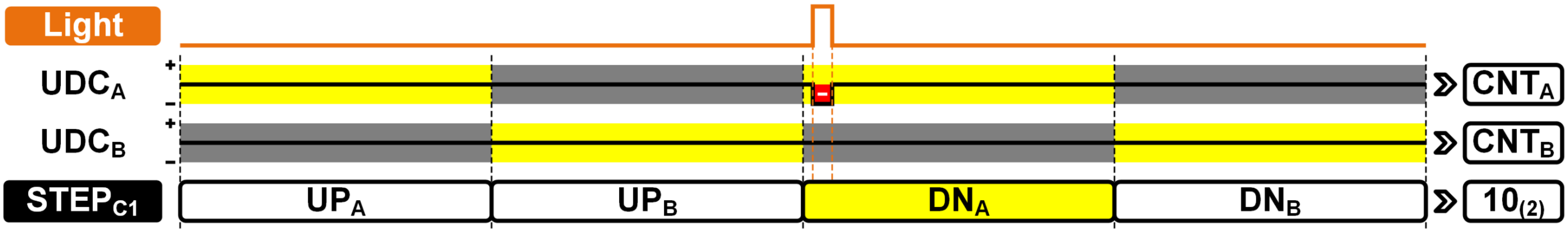


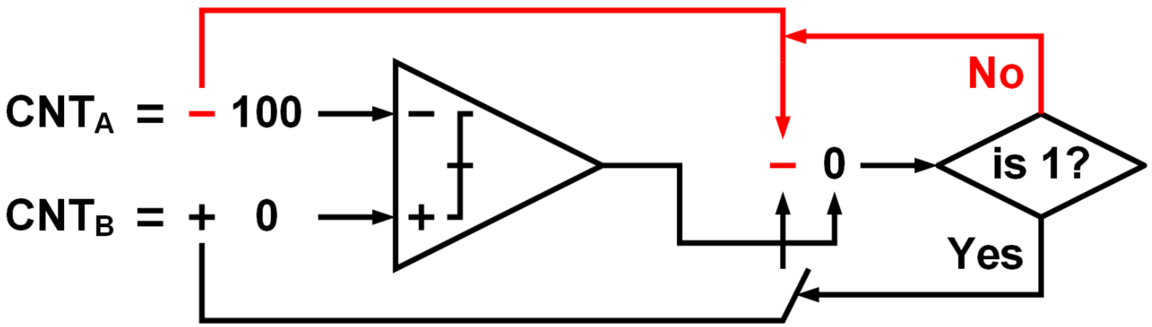


|CNT$_B$| > |CNT$_A$|? → Lower bit = 0

Sign of winner? → Upper bit

Quaternary Searching Algorithm [Step 1]

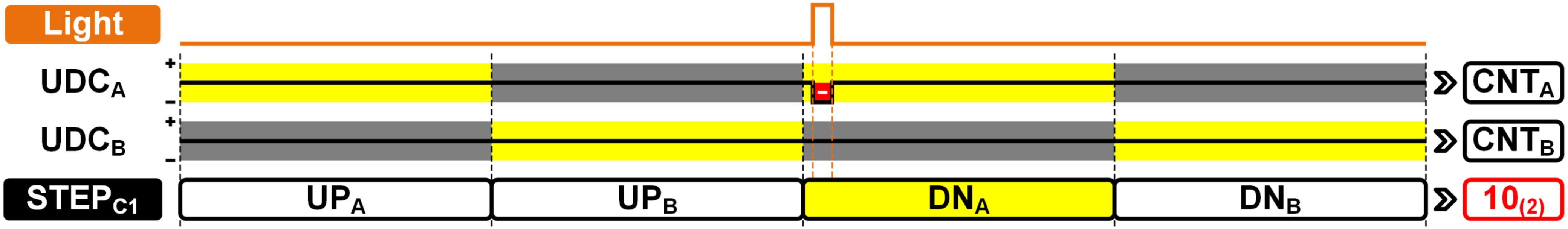


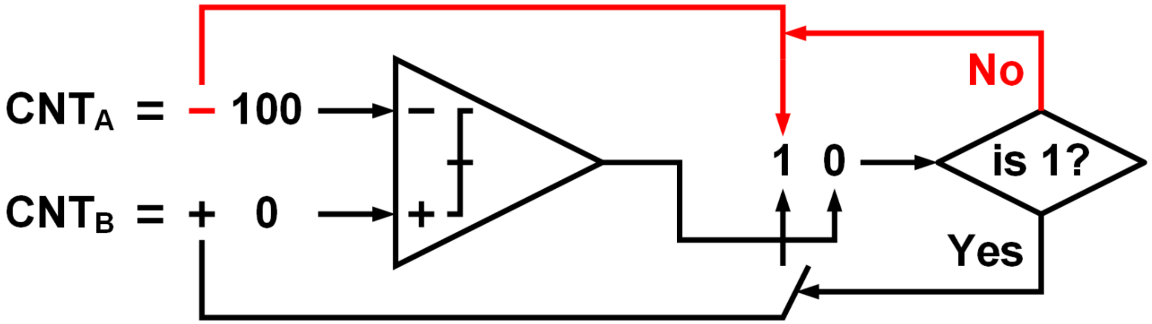


$|CNT_B| > |CNT_A|$? → Lower bit = 0

Sign of winner? → Upper bit

Quaternary Searching Algorithm [Step 1]

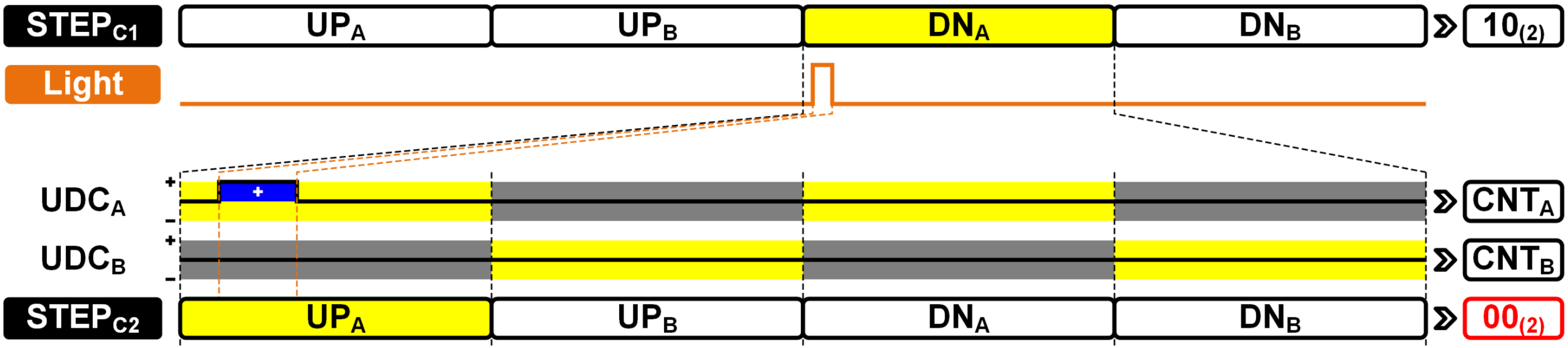


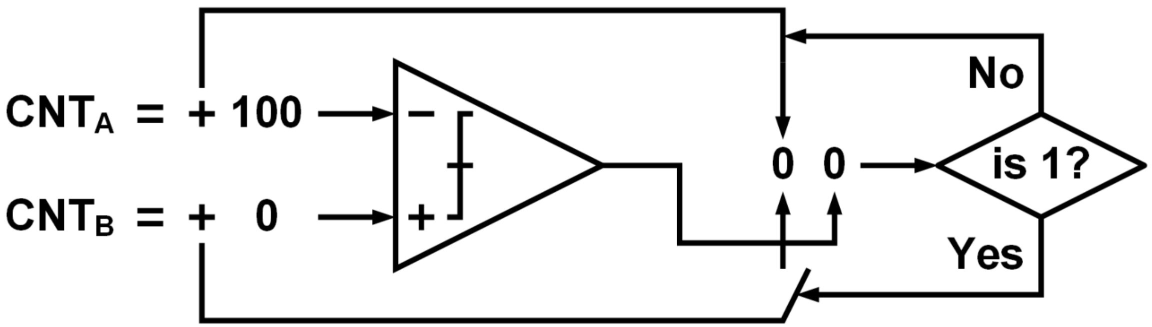


$|CNT_B| > |CNT_A|$? → Lower bit = 0

Sign of winner? → Upper bit = 1

Quaternary Searching Algorithm [Step 2]

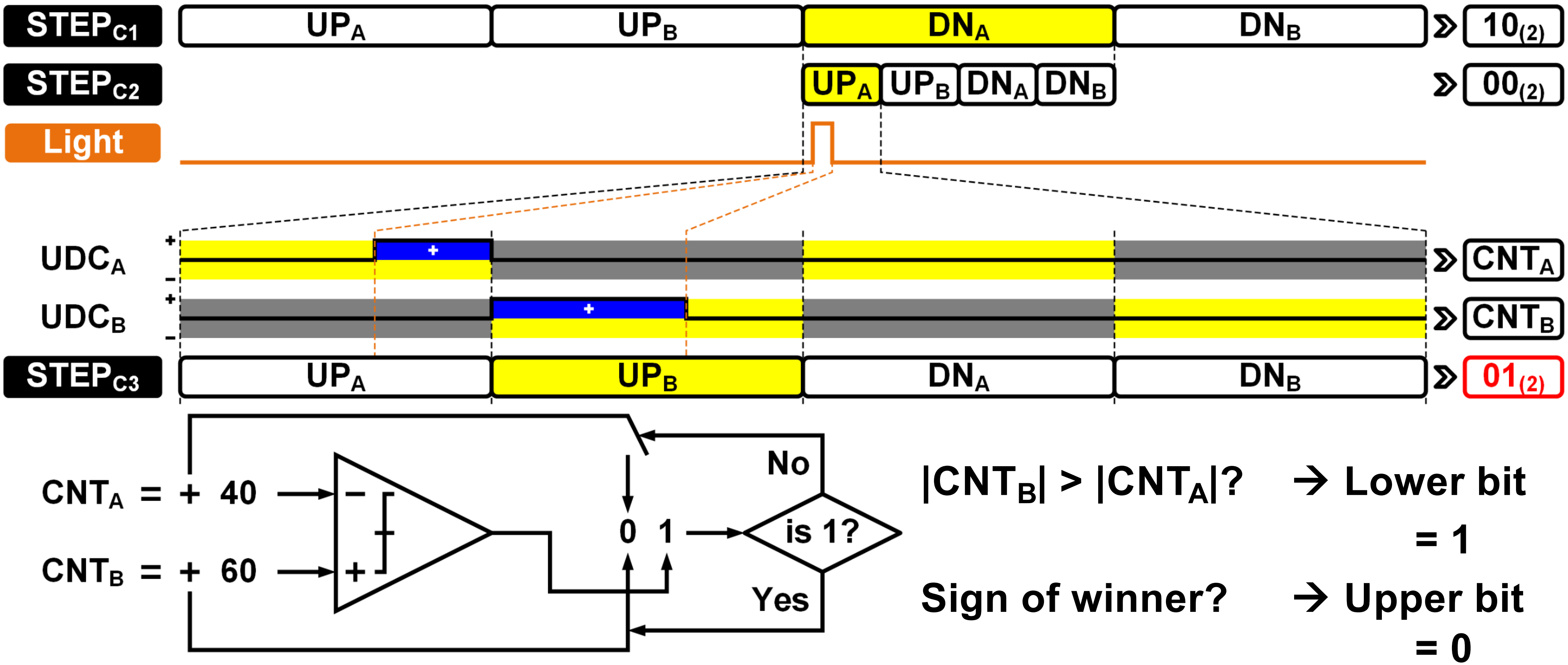




|CNT$_B$| > |CNT$_A$|? → Lower bit = 0

Sign of winner? → Upper bit = 0

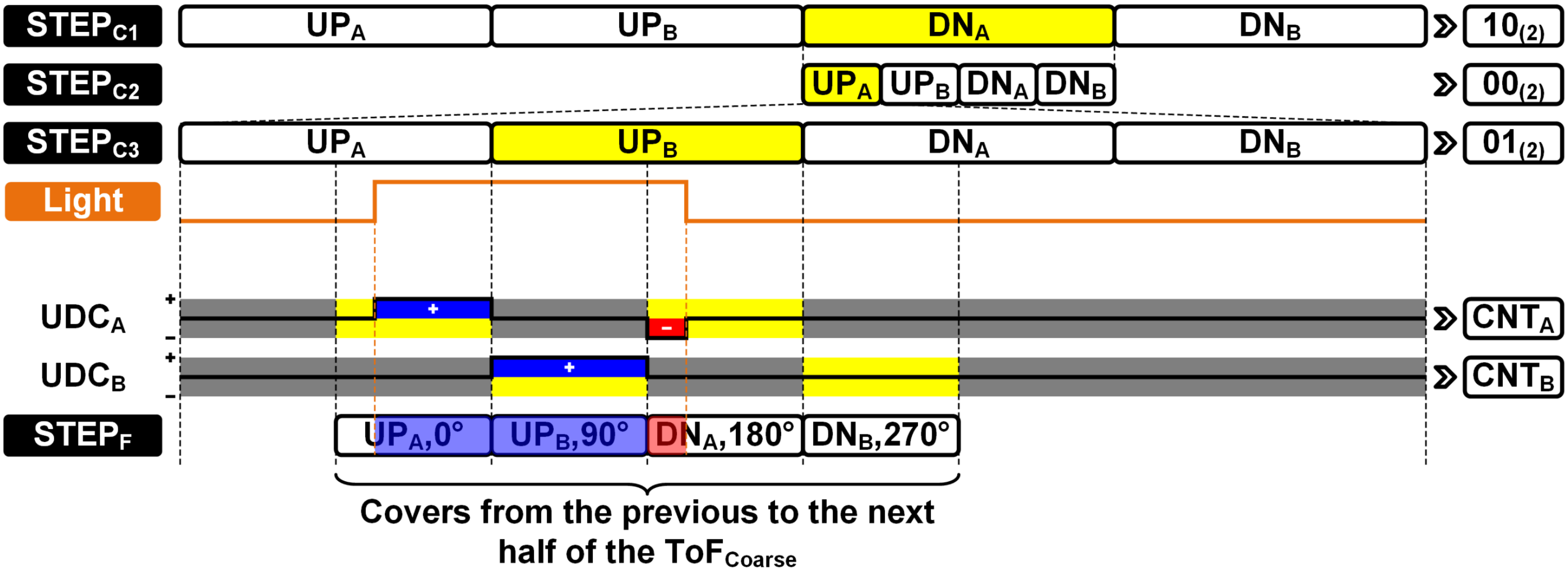
Quaternary Searching Algorithm [Step 3]



|CNTB| > |CNTA|? → Lower bit = 1

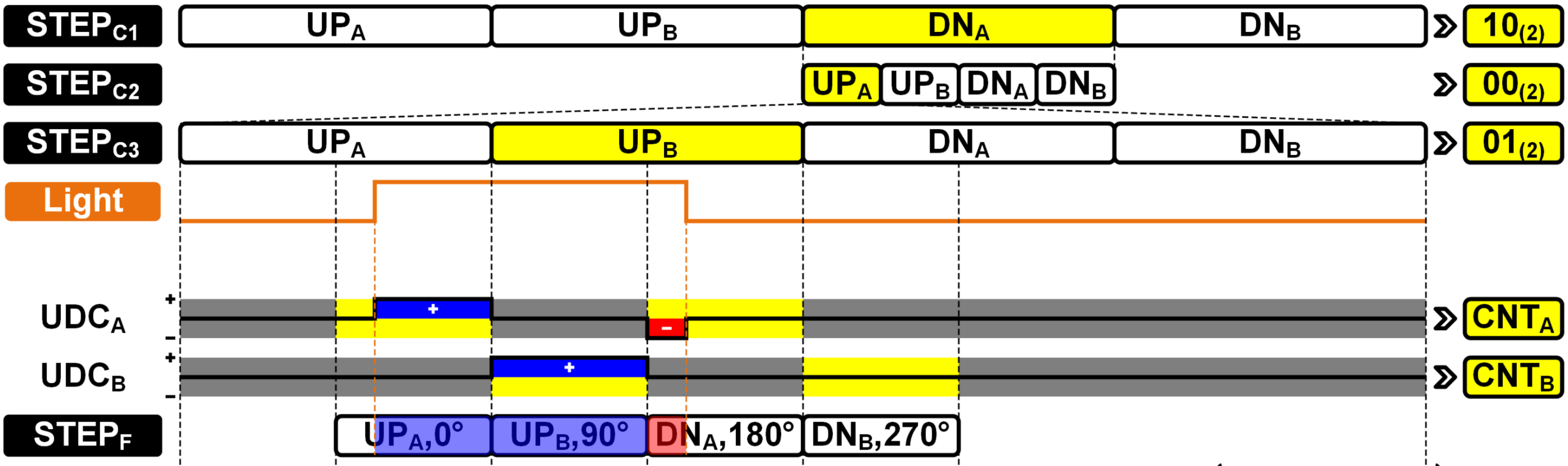
Sign of winner? → Upper bit = 0

Time-Gated Δ-Intensity Phase Detection



STEP$_F$ operates with 32-times higher SBR than STEP$_{C1}$ in the quaternary search ☺

Time-Gated Δ-Intensity Phase Detection



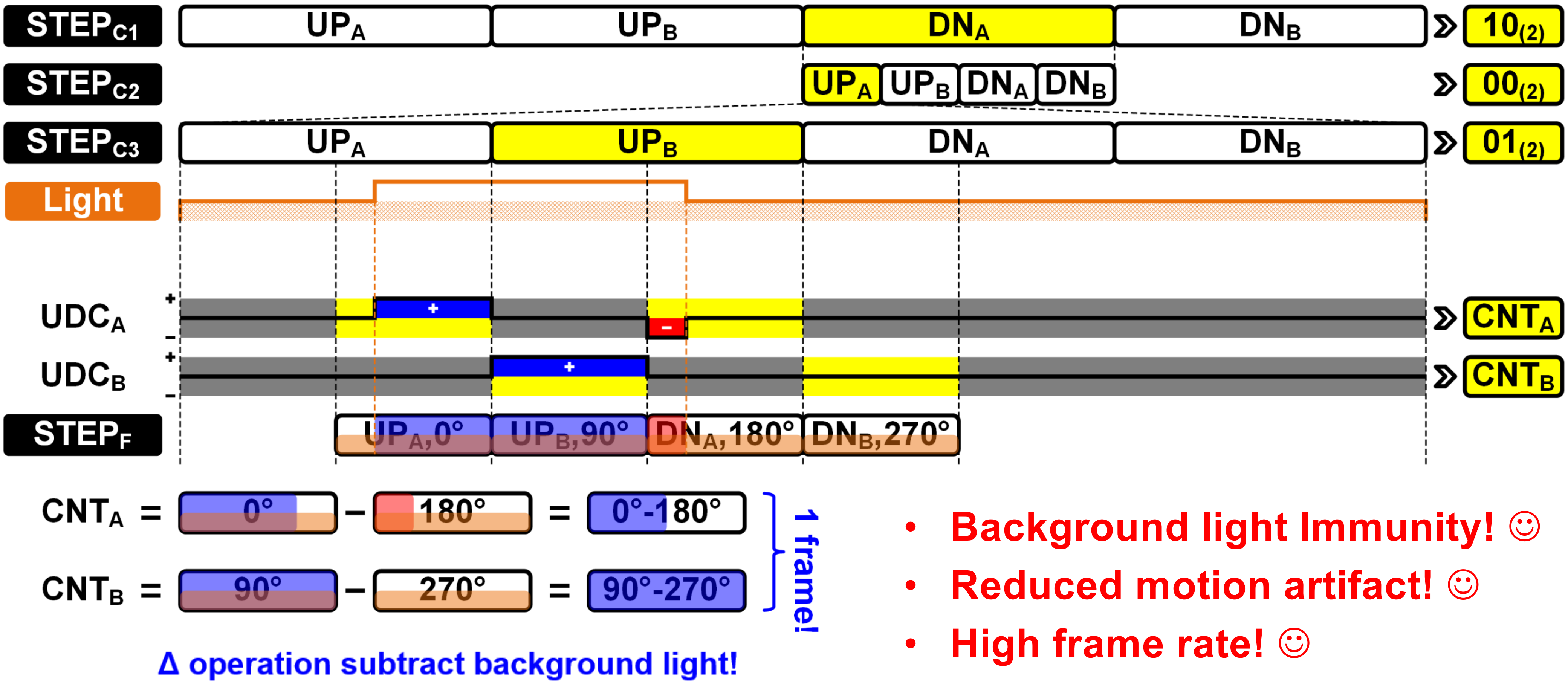
CNT_A = 0° − 180° = 0°-180°

CNT_B = 90° − 270° = 90°-270°

$$ToF_{Fine} = \frac{cT_{LSB}}{2\pi} \times \tan^{-1}\left(\frac{CNT_B - CNT_A}{CNT_B + CNT_A}\right)$$

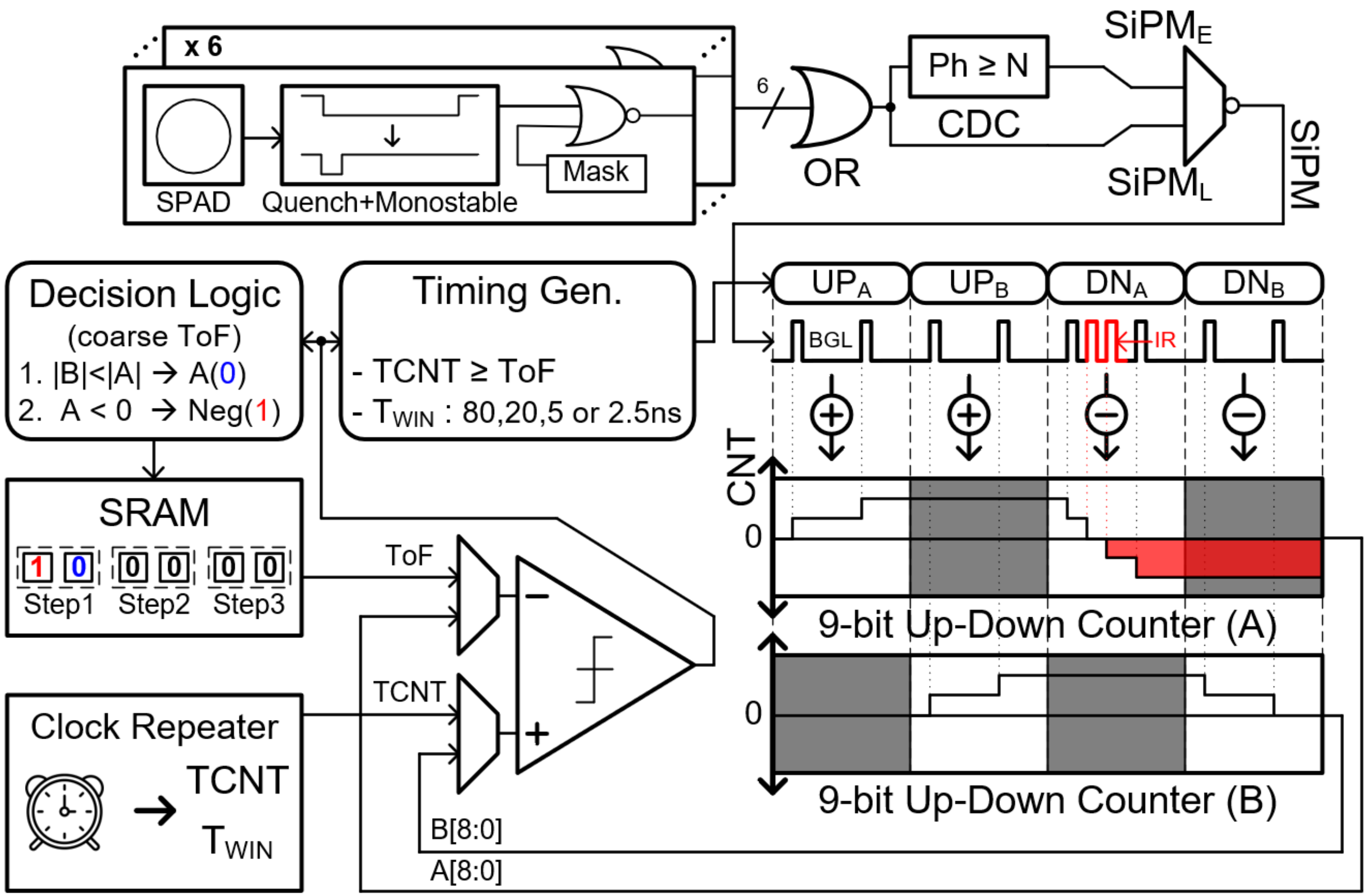
$$ToF = ToF_{Coarse} + ToF_{Fine}$$

Time-Gated Δ-Intensity Phase Detection



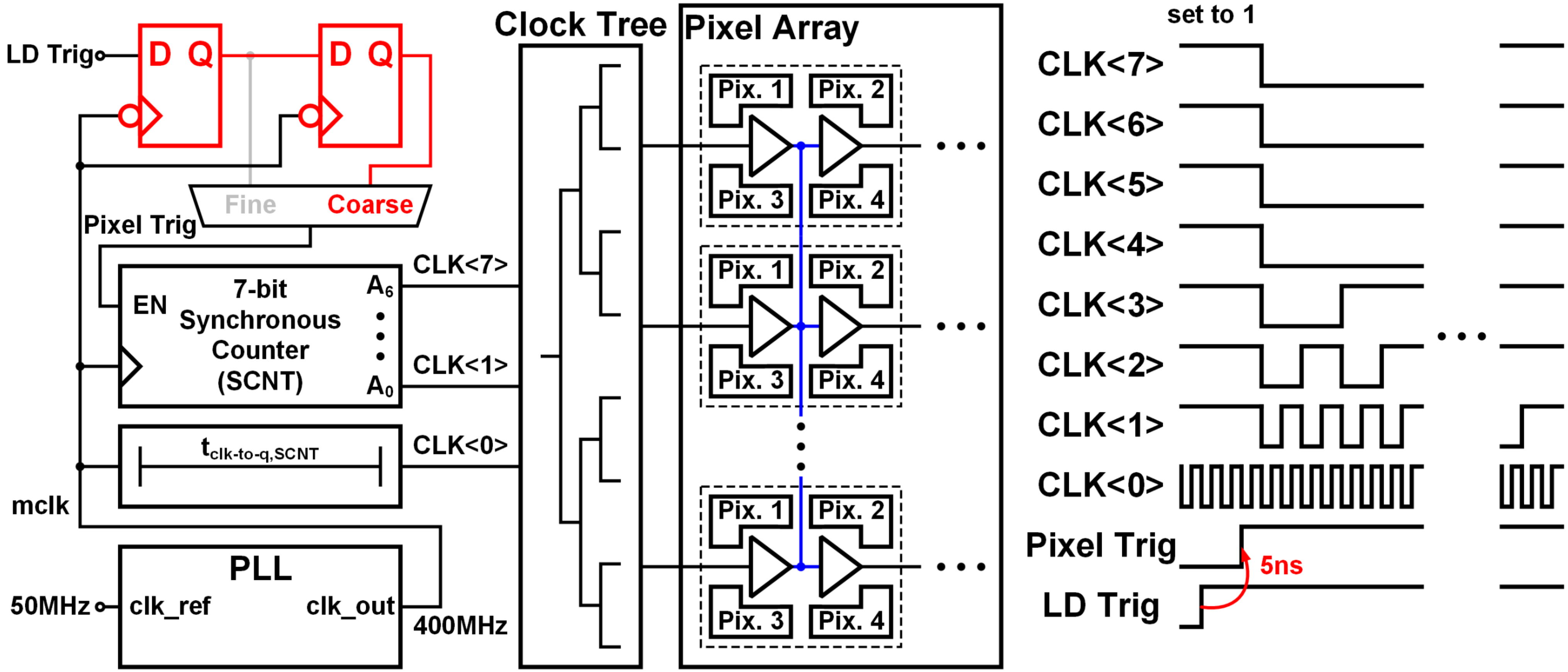
- **Background light Immunity! ☺**
- **Reduced motion artifact! ☺**
- **High frame rate! ☺**

Pixel Architecture

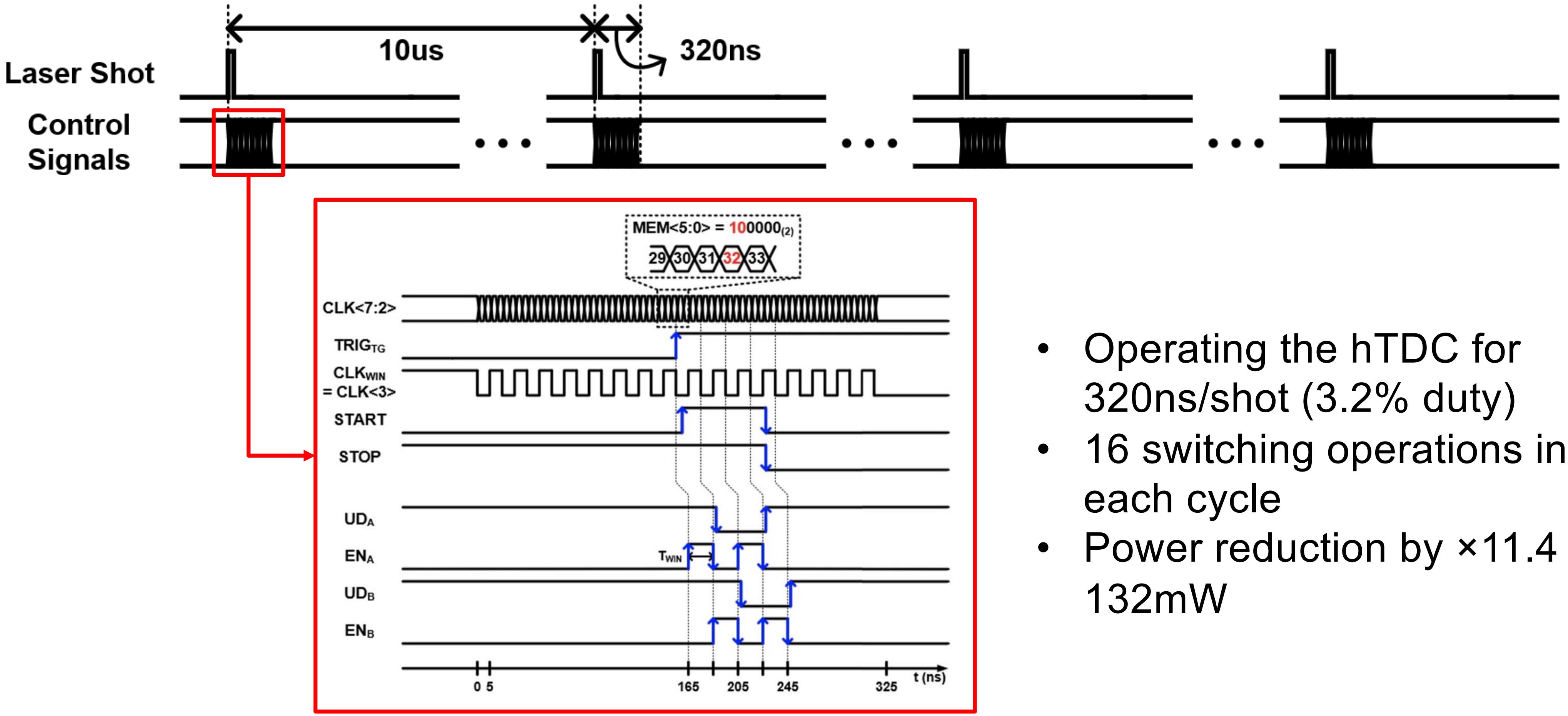


- 6 SPADs w/ AFE & masking mem
- Coincidence detection circuit
- Two 9-b UDC for quaternary search
- Timing generator for time bin management
- Clock repeater shared by four neighbor pixels

Clock Generator

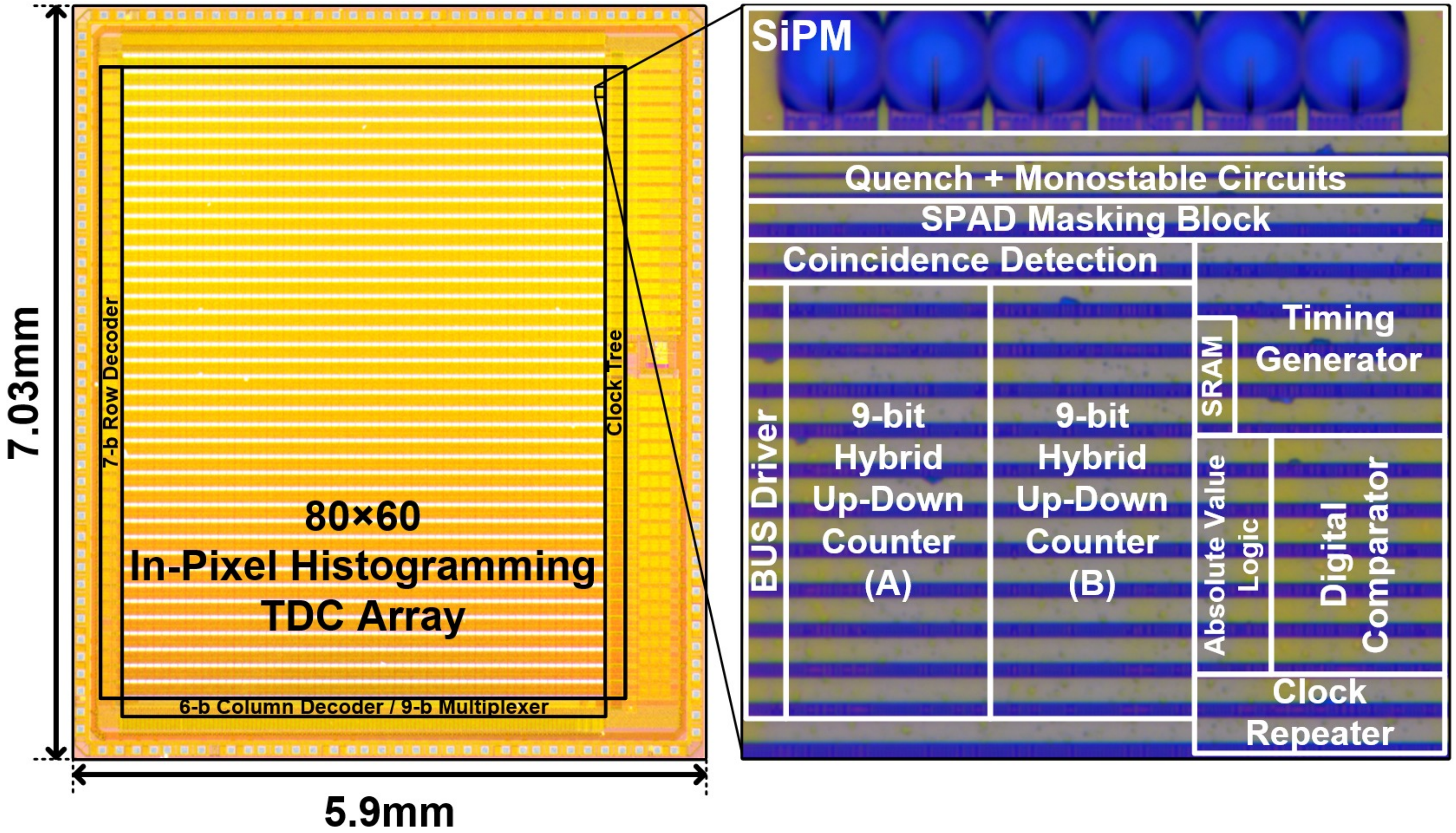


Duty-Cycling for Power Reduction



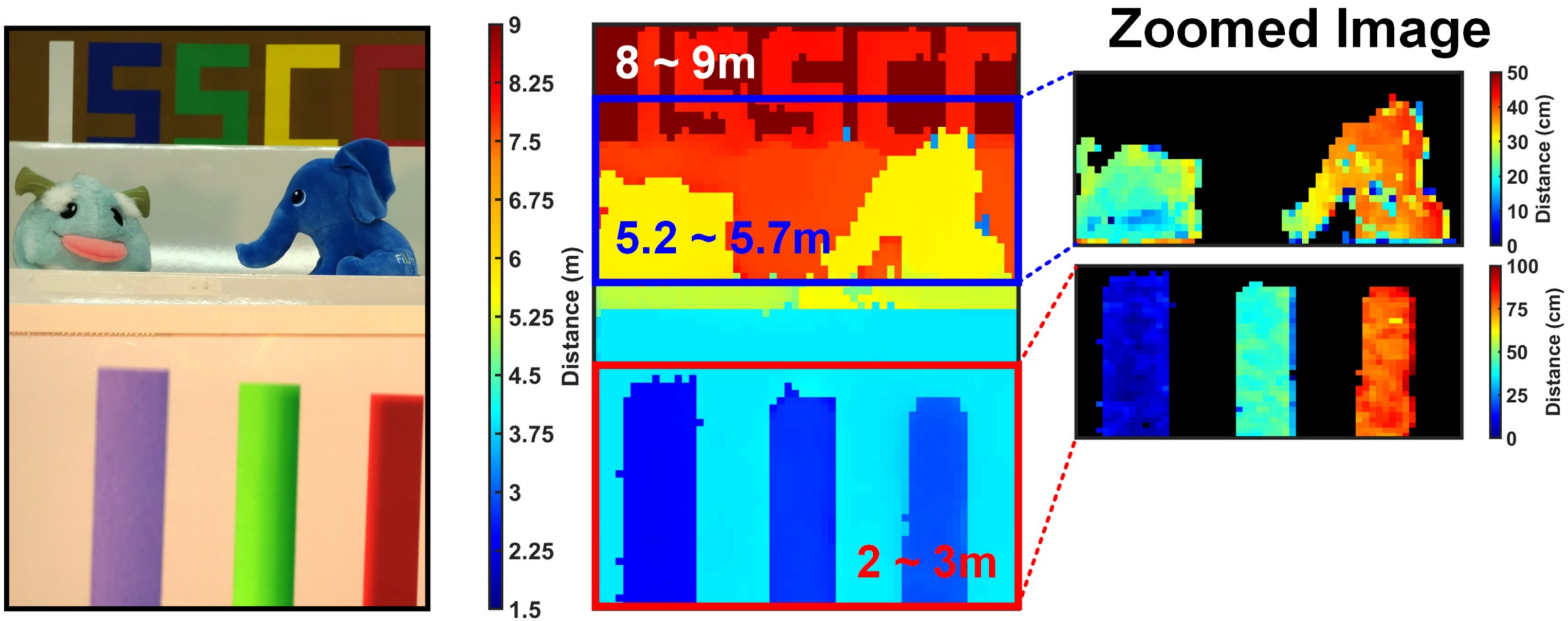
- Operating the hTDC for 320ns/shot (3.2% duty)
- 16 switching operations in each cycle
- Power reduction by ×11.4 to 132mW

Fabricated Prototype



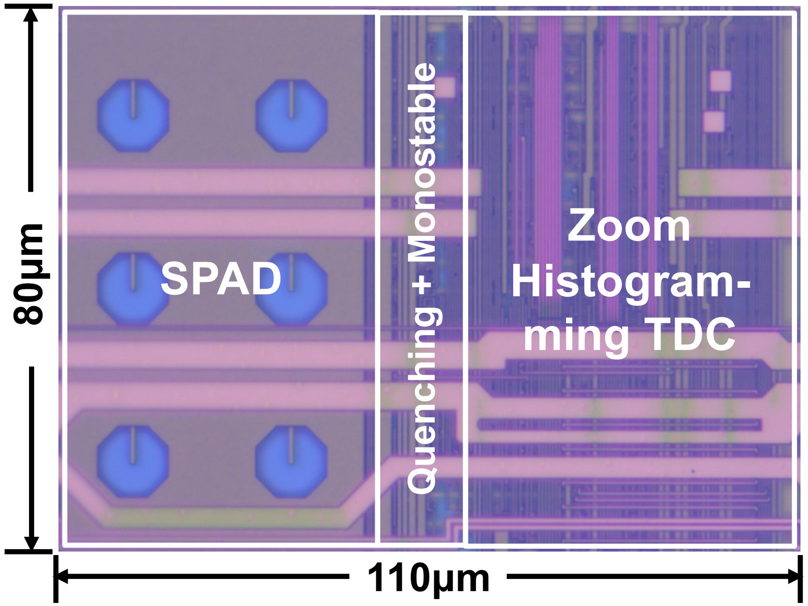
- Fabricated in 110nm FSI
- 6 SPADs per pixel
- Chip size: 7.03 × 5.9mm^2
- Pixel pitch: 75 μm
- Spatial resolution: 80 × 60
- TDC resolution: 5 ns / 100 ps

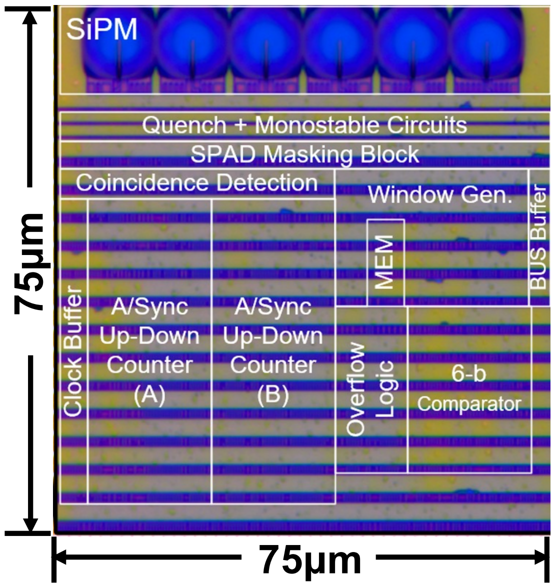
Depth Image

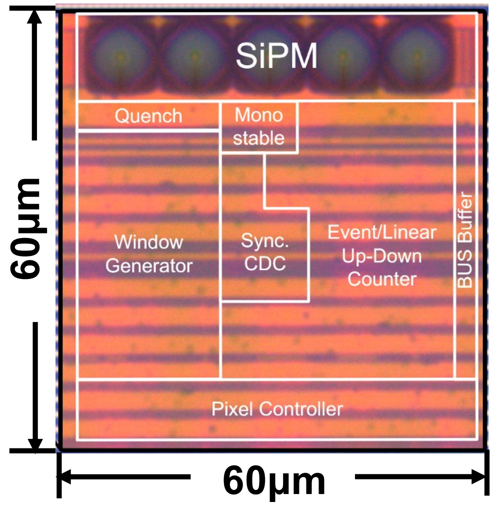


Captured in 30fps w/ 30klux background light

Other Issues in Previous hTDCs







Large pixel size

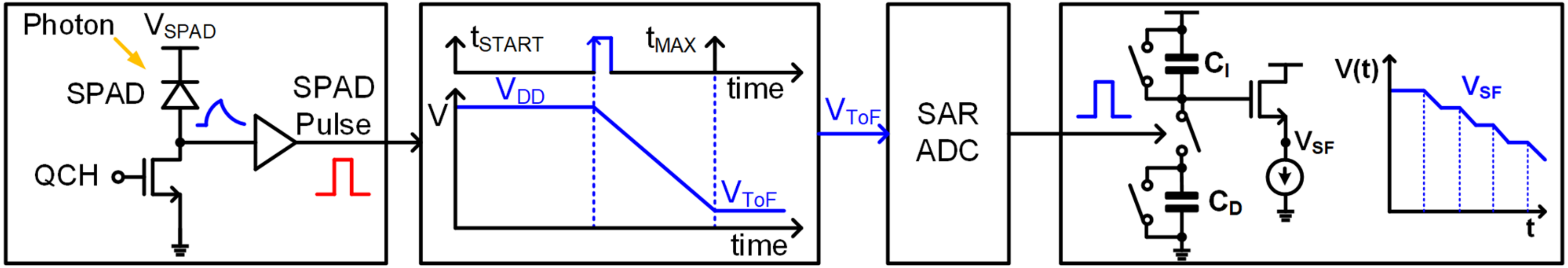
Large power consumption

⇩

Limited spatial resolution! ☹

⇨ Solution: Analog-assisted timing generator and counter replacing digital counterparts

Analog-Assisted Zoom hTDC



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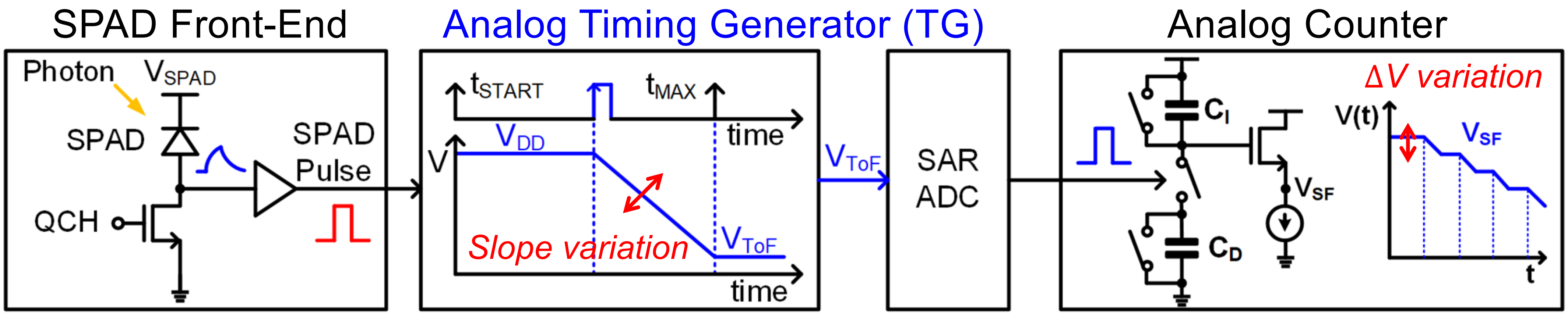
- **Challenges in reducing pixel size & power consumption**
  1. In-pixel SA hTDC operation in voltage domain ☺
  2. Digital counter-based TG → Analog-TG (TAC + SAR ADC) ☺
  3. Digital UP/DN Counter → Analog Counters ☺
- Capacitors are located under SPAD device thanks to BSI technology ☺

Challenges in Analog-Assisted Zoom hTDC

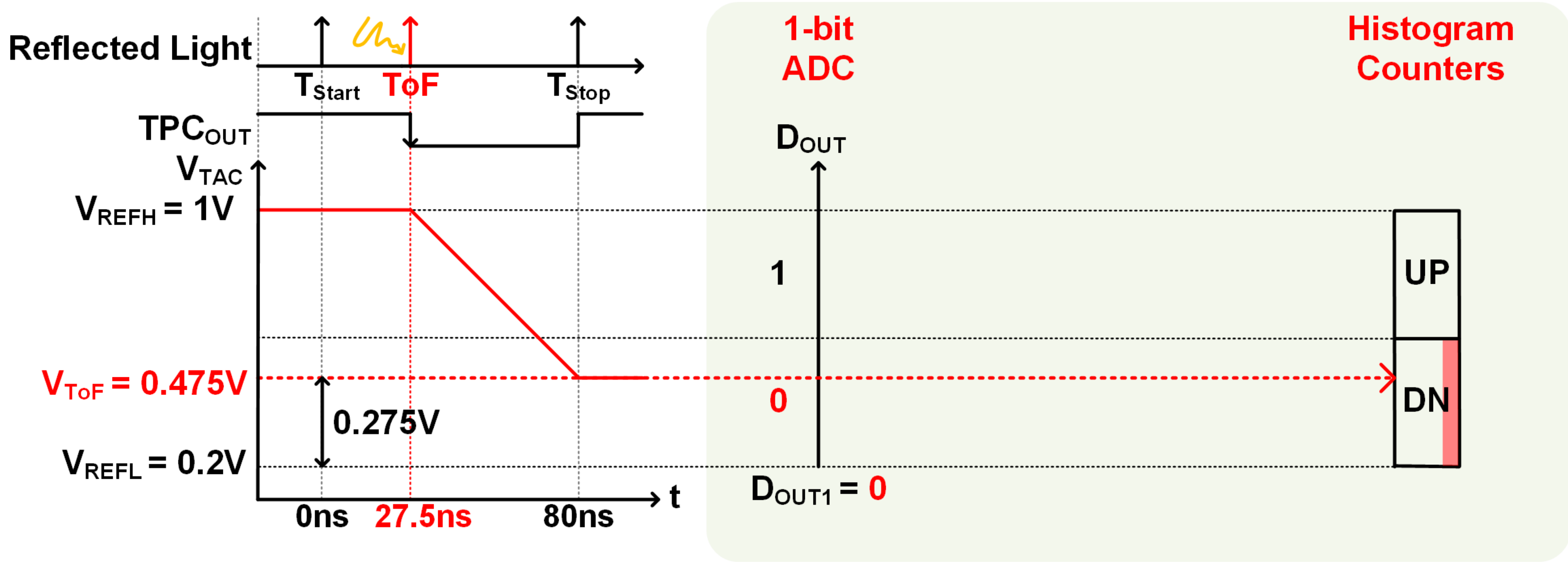


- **Challenges in pixel mismatch** in the analog-assisted circuits due to variations in capacitor size, current source, etc. ☹
- **Solutions: Self-calibration**
  - TAC + Self-Referenced SAR ADC ☺
  - Analog Counters + Self-Referenced SS ADC ☺

Conceptual Operation: Coarse Step 1

1. T/A Conversion

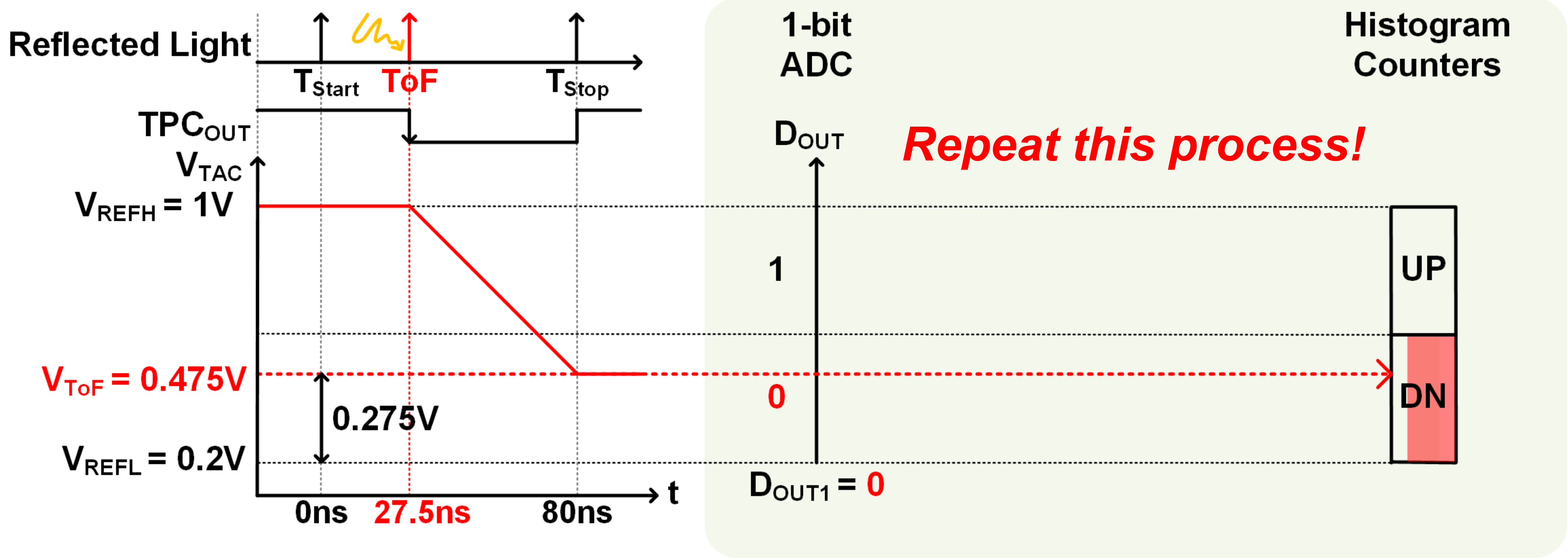
2. A/D Conversion & Histogram



Conceptual Operation: Coarse Step 1

1. T/A Conversion

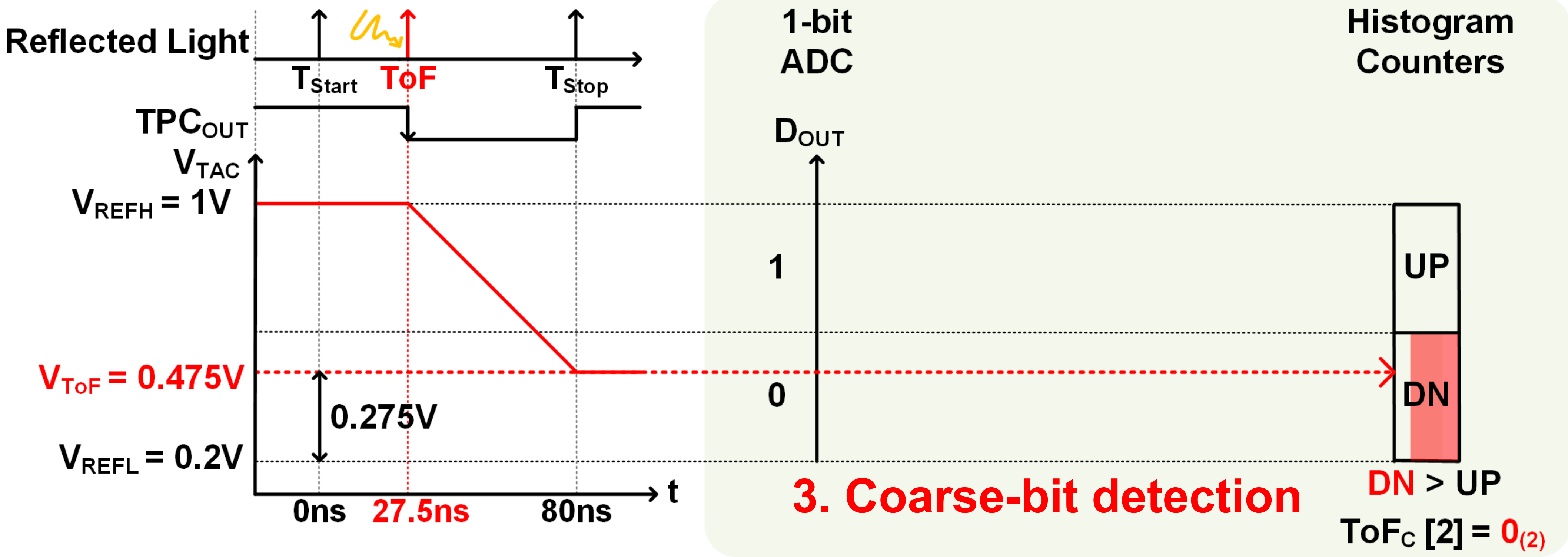
2. A/D Conversion & Histogram



Conceptual Operation: Coarse Step 1

1. T/A Conversion

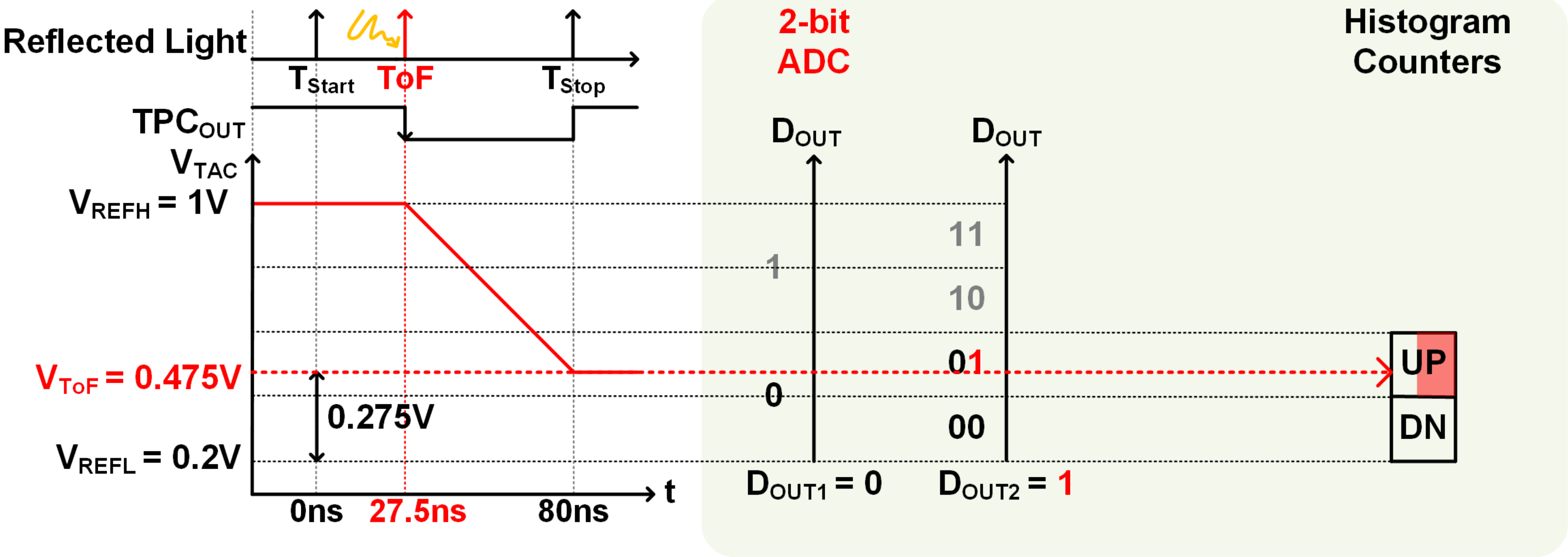
2. A/D Conversion & Histogram



Conceptual Operation: Coarse Step 2

1. T/A Conversion

2. A/D Conversion & Histogram

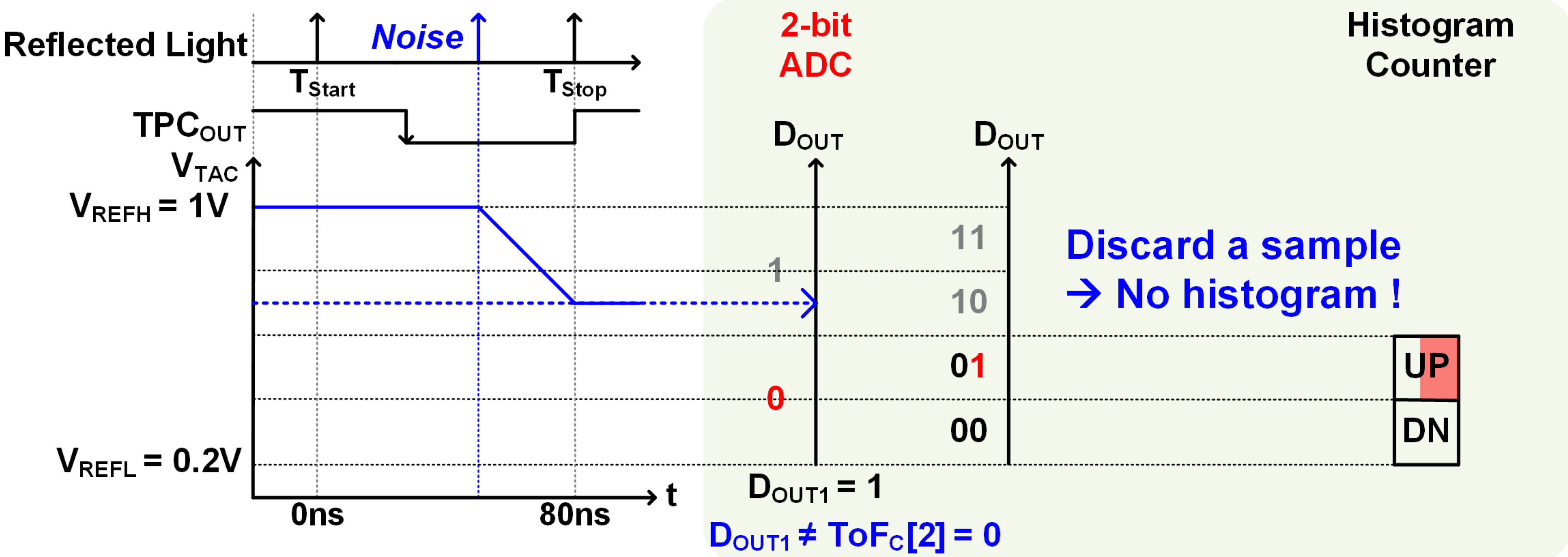


Zooming of the voltage range by ×2

Conceptual Operation: Error Prediction

1. T/A Conversion

2. A/D Conversion & Histogram

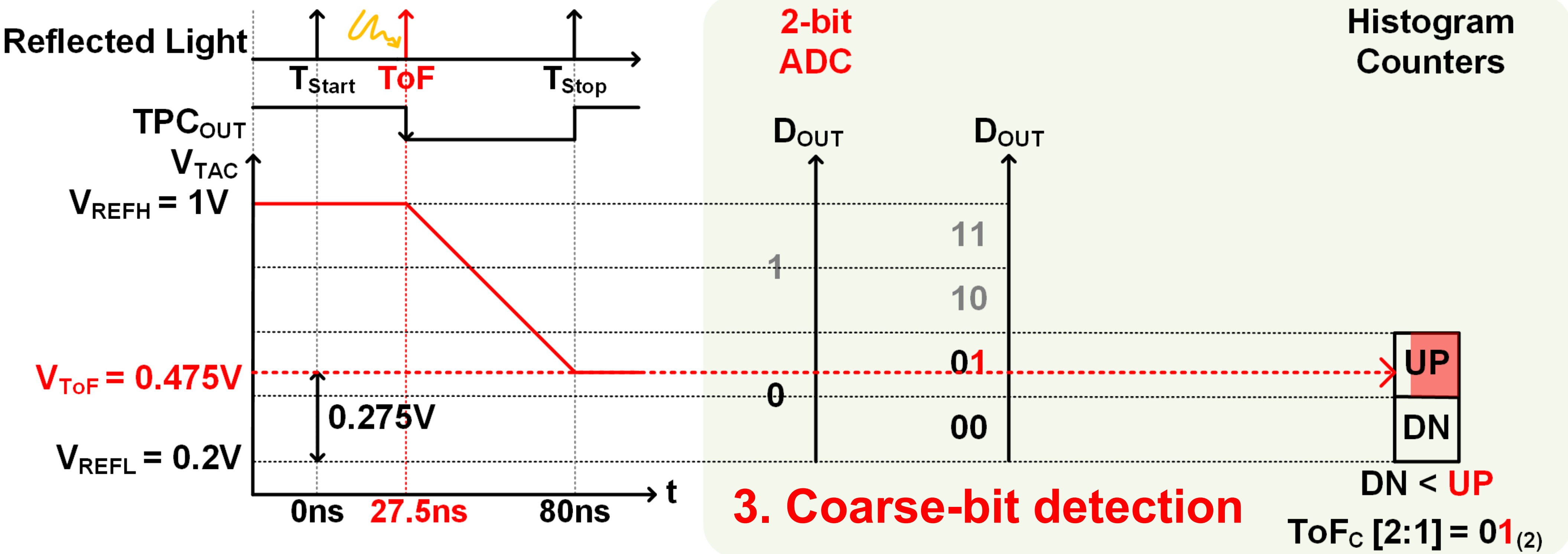


Error predictor performs the role in time gating.

Conceptual Operation: Coarse Step 2

1. T/A Conversion

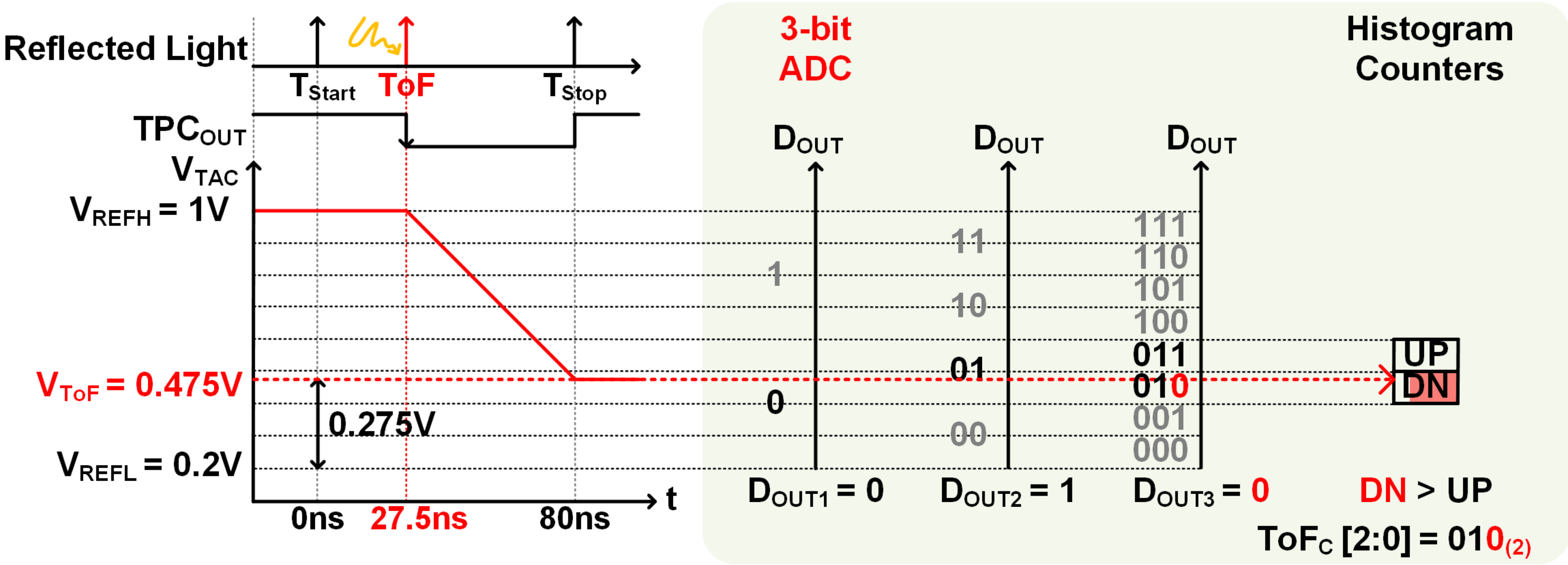
2. A/D Conversion & Histogram



Conceptual Operation: Coarse Step 3

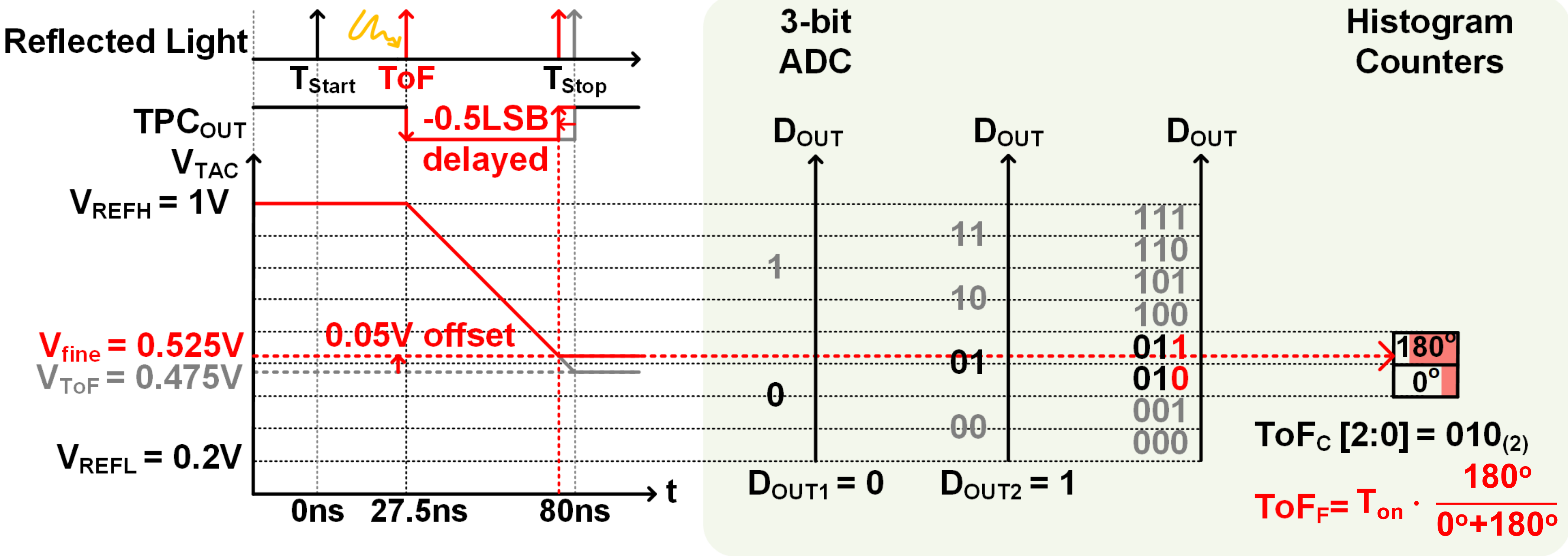
1. T/A Conversion

2. A/D Conversion & Histogram



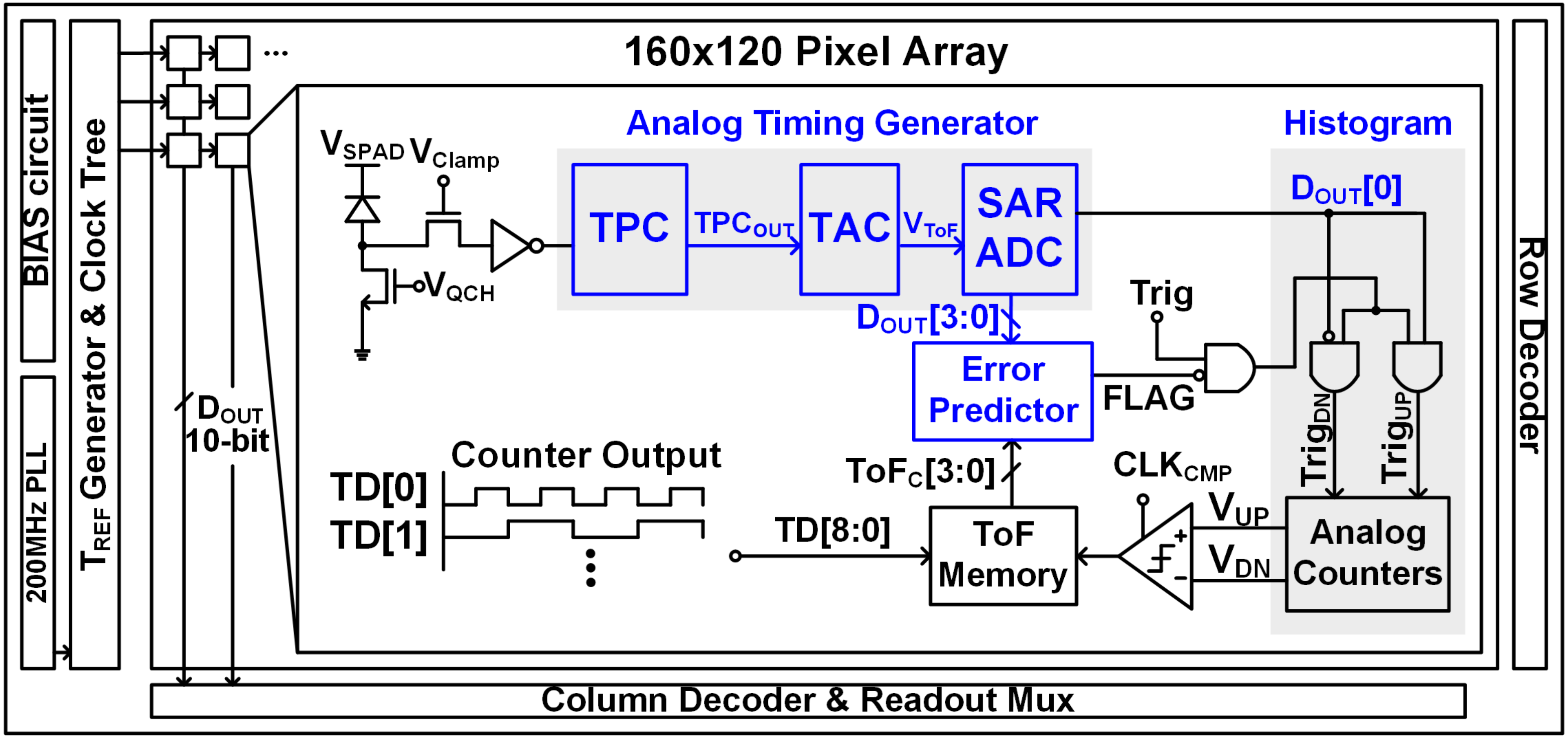
Conceptual Operation: Fine Step

Indirect ToF method

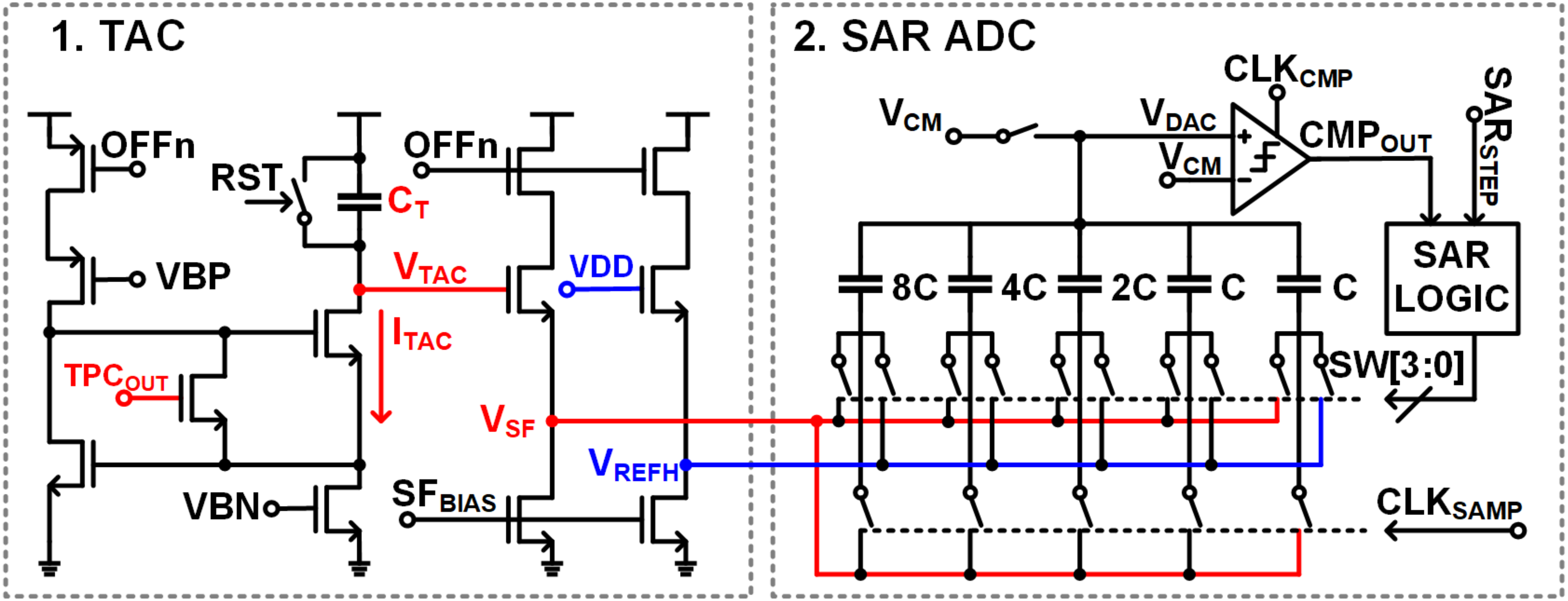


Phase shift of time bin → V_{ToF} offset generation based on $ToF_C[0]$ value

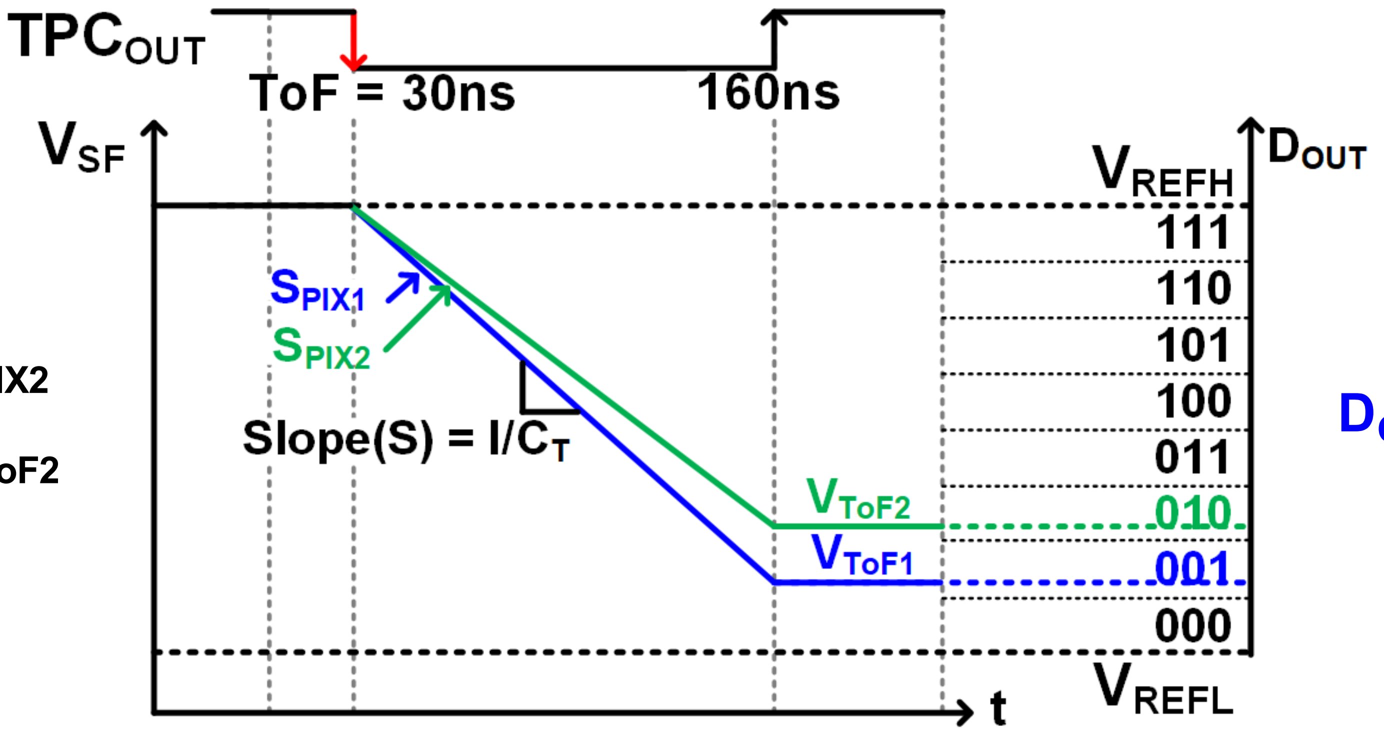
Block Diagram of Proposed Sensor



Schematic of Self-Referenced SAR ADC



Pixel Mismatch of TAC & SF



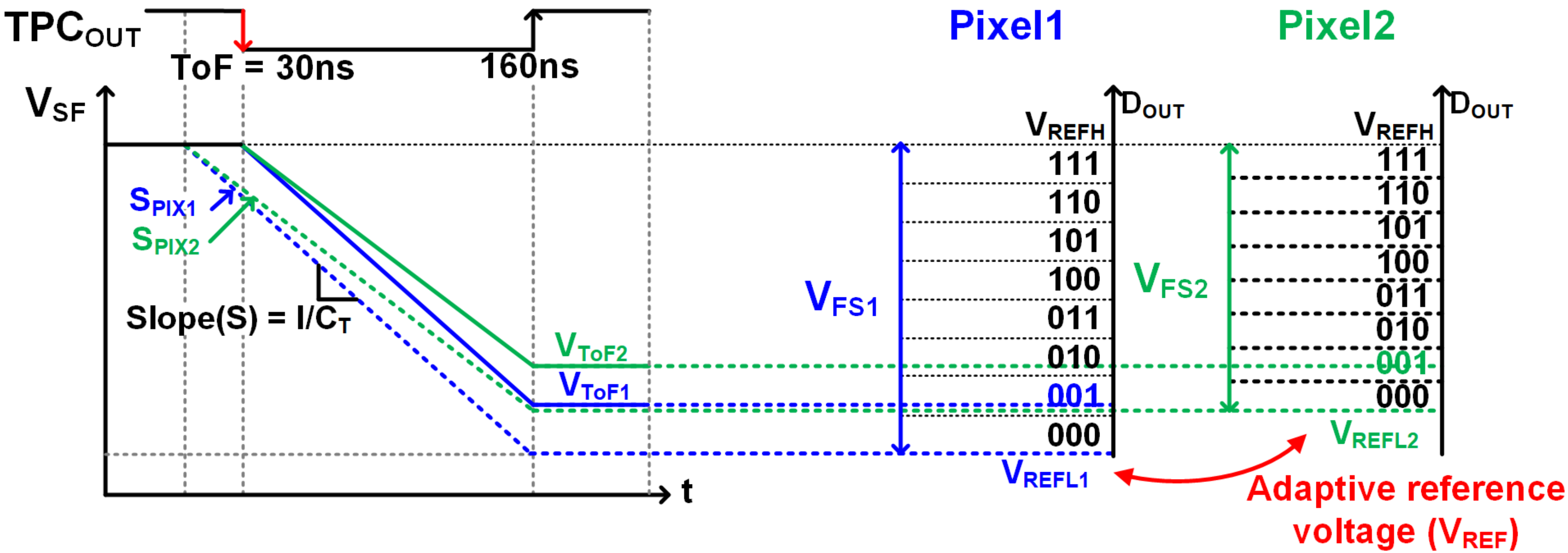
$S_{PIX1} \neq S_{PIX2}$

$V_{ToF1} \neq V_{ToF2}$

$D_{OUT1} \neq D_{OUT2}$

- Mismatches between pixels due to PVT variation ☹
- In MC simulation with a 100fF of C_T, $\sigma_{V_{TOF}}$ ~ 72mV > 1LSB (50mV)

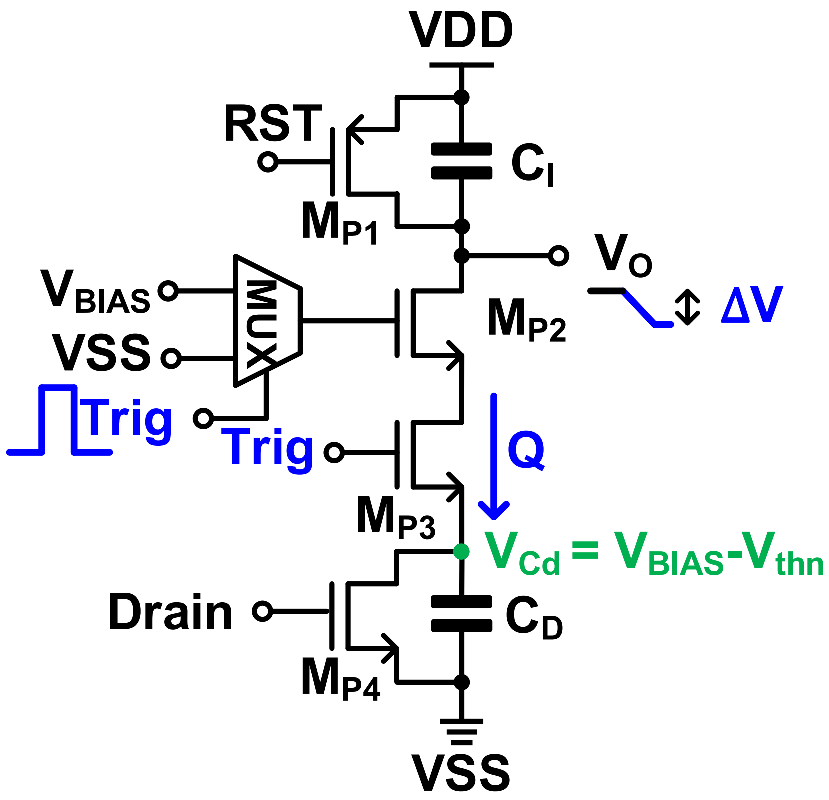
Automatic Calibration by Self-Reference

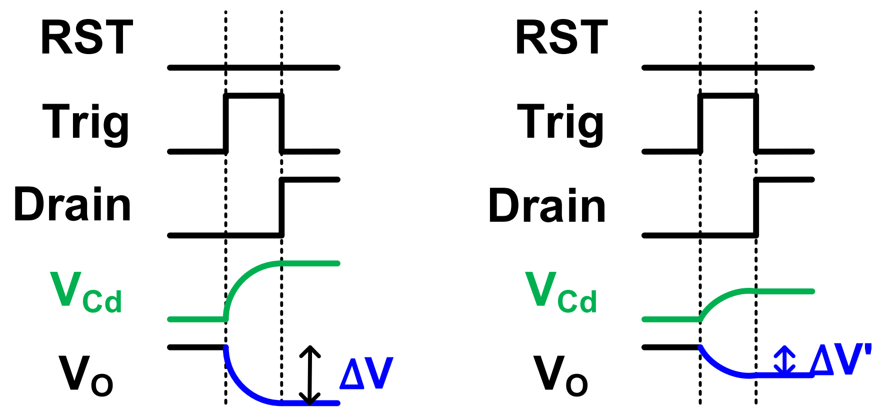


- Auto-Correction: generating both signal V_{ToF} and referenced voltage (V_{REFL}) in the same TAC. ☺

$D_{OUT1} = D_{OUT2}$

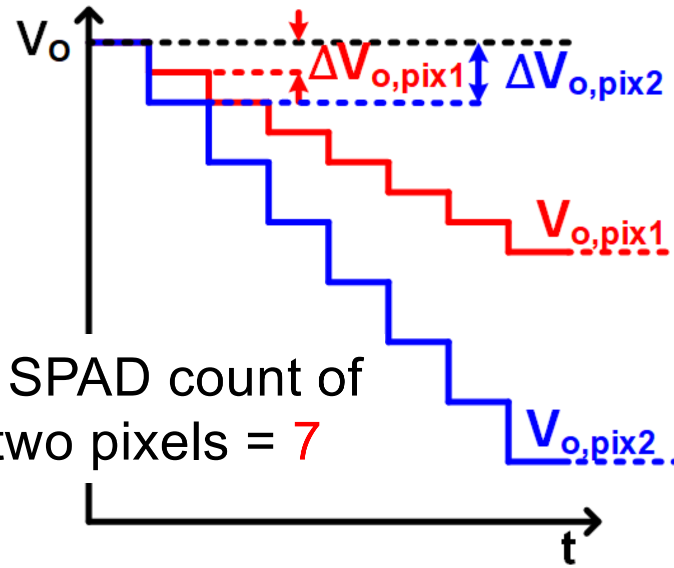
Mismatch in Analog Counter

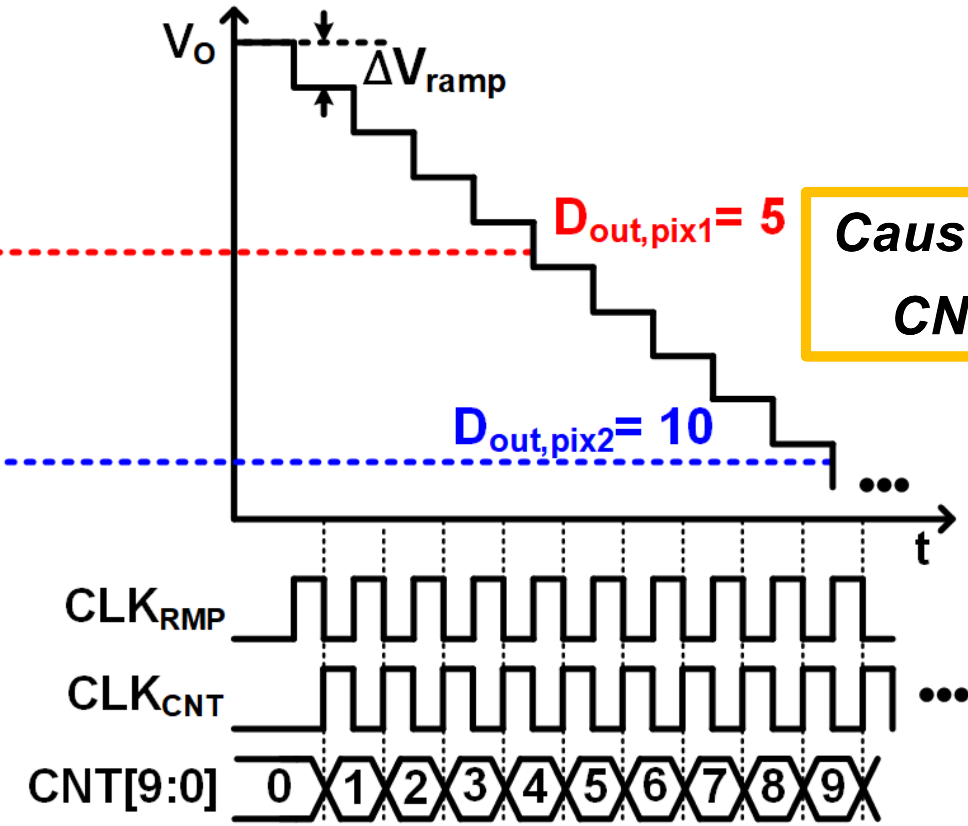




- A mismatch between pixels of step size due to V_{TH} & capacitor variation ☹
- It is important to accurately read out the phase intensity stored in analog counters to calculate ToF_{FINE}.

Conventional Single-Slope ADC



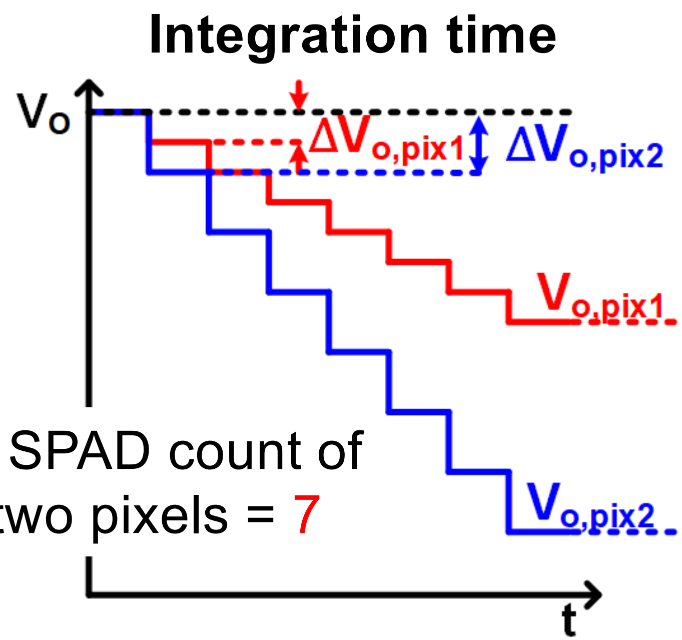


Cause Error!!

CNT ≠ 7

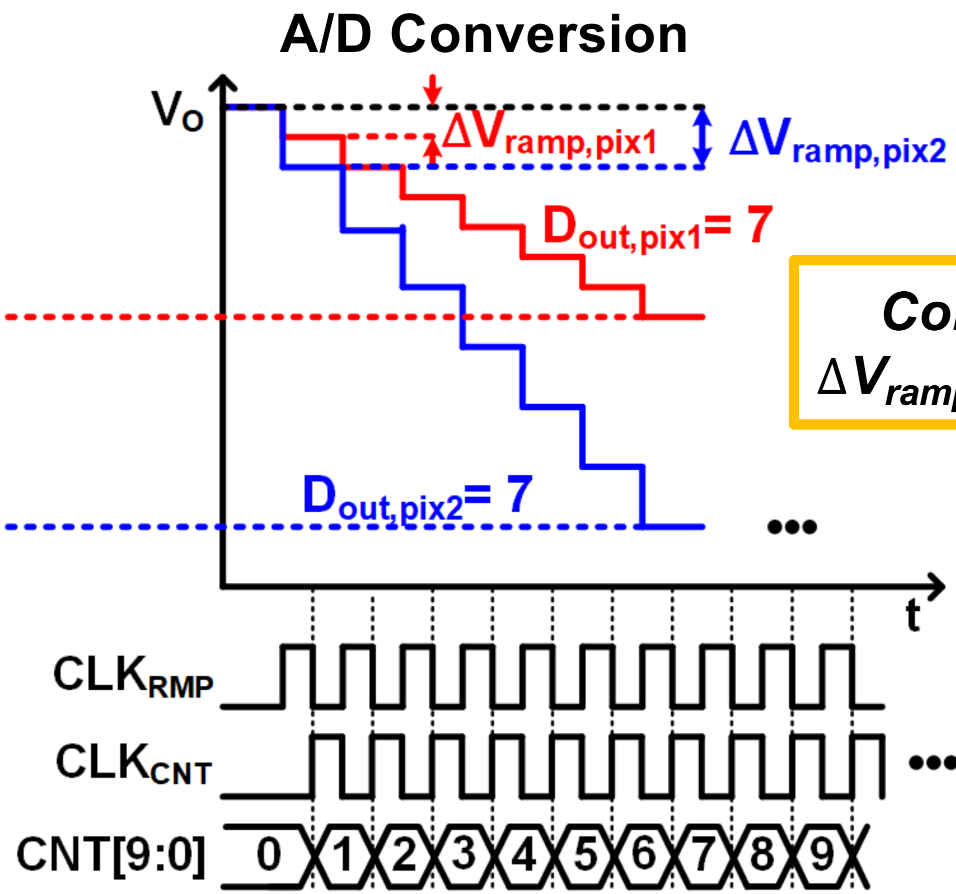
- The SPAD count of the two pixels = 7
- Capacitor & V_{TH} mismatch causes ΔV_O variation between pixels.

Self-Referenced SS ADC



- The SPAD count of the two pixels = 7

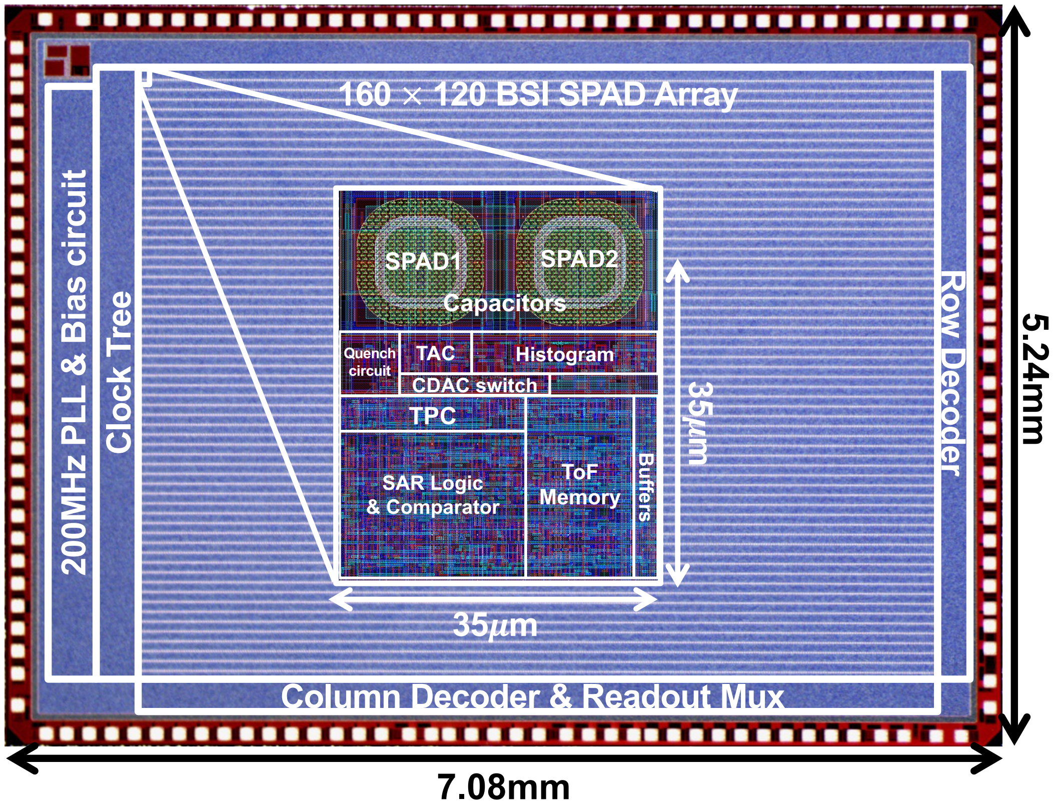
- The ramp signal is also generated by an in-pixel analog counter.



Correct!!
$\Delta V_{ramp} = \Delta V_{o,pix}$

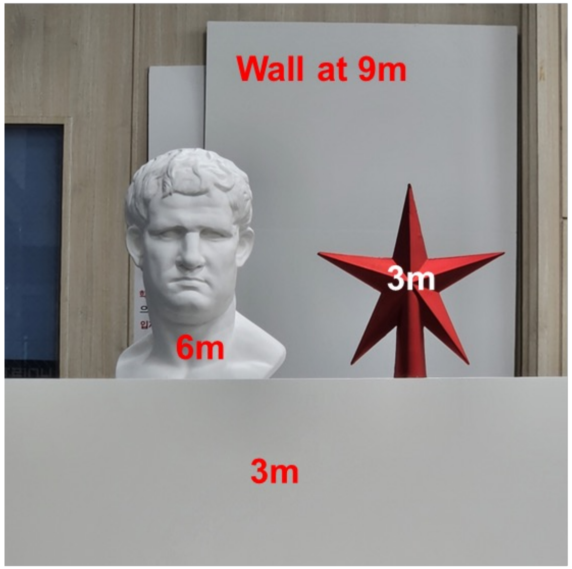
S.-H. Han, VLSI 2022

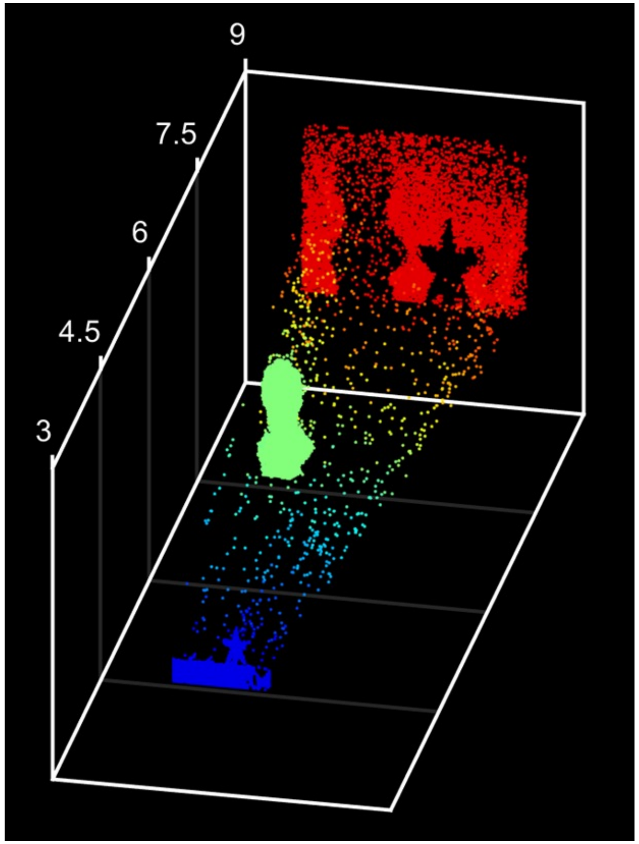
Chip Micrograph



- Fabricated in 110nm BSI
- A single SPAD per pixel
- Chip size: 7.08 × 5.24mm^2
- Pixel pitch: 35 μm
- Spatial resolution: 160 × 120
- TDC resolution: 10 ns / 230 ps

Indoor Depth Image





Depth image taken at a 10fps under indoor condition

Comparison of Three hTDCs

	SA hTDC w/ Digital Counter	QS hTDC w/ Digltal Counter	Analog Assisted SA hTDC
Technology	110nm BSI	110nm FSI	110nm BSI
Pixel array	100 × 76	80 × 60	160 × 120
Chip size	7.0 × 5.9mm^2	7.0 × 5.9mm^2	5.9 × 5.2mm^2
hTDC area	2700μm^2	3600μm^2	520μm^2
TDC resolution	Coarse 10ns [1]Fine 300ps	Coarse 5ns [1]Fine 100ps	Coarse 10ns [1]Fine 230ps
Maximum distance	50m (designed: 96m)	45m	24m
Depth precision	10.5cm	1.5cm@2m	2.8cm@7m
Depth nonlinearity	4.5cm	2.5cm@2m	4.8cm@7m
Power consumption	104mW@40klux	132mW	60mW
Frame rate	10fps@10m, 40klux	30fps@10m, 30klux	10fps@10m, 6klux
# of TDCs	7600	4800	19200

[1]Estimated equivalent value from measurement results

Thank you for your attention!

Any questions?