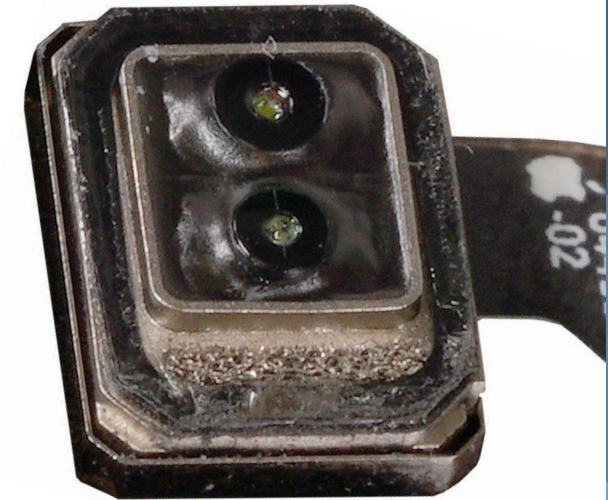
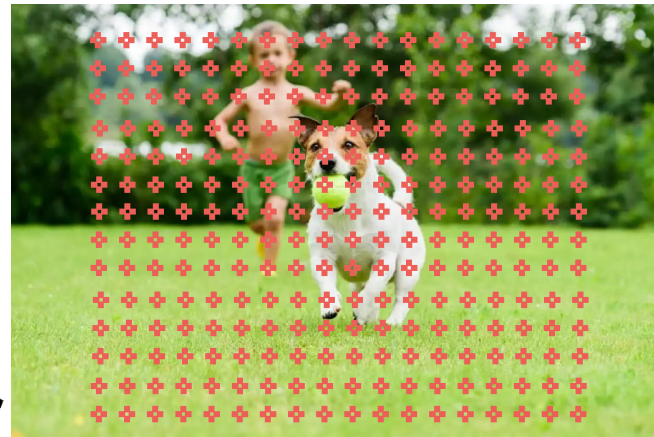




Physical and Cost Comparison of Smartphone Laser Autofocus Solutions

presented by P.L. Bonanno



SONY

We provide industrial companies, financial investors and R&D organizations, with market research and marketing analysis, technology, supply chain and cost analysis, as well as performance evaluation, to help our customers in their decision-making about their future business and manufacturing strategy in the semiconductor, photonic and electronic sectors.

3 CORE ACTIVITIES BASED ON DEEP SYNERGIES

Market & Technology

- Market, technology, and strategy consulting
- M&A, Due Diligence and evaluation of companies

Teardown Reverse engineering and costing

- Technology, process & cost analysis
- Teardown and reverse engineering
- Comparative analysis

Performance analysis

- Test of electric and electro-optical performance of devices
- Comparison of performances and related technical choice

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LASER AUTOFOCUS REVERSE COSTING

Presentation Outline

1. Smartphone 3D Imaging and Laser Autofocus
2. 3 systems
 - iPhone 15 Pro LiDAR module by Sony
 - VL53L5 by STMicroelectronics
 - TMF8821 by ams AG
3. Reverse Costing Methodology
4. Approximative Model
5. Results & Discussion

LASER AUTOFOCUS REVERSE COSTING










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SMARTPHONE 3D IMAGING AND LASER AUTOFOCUS

Smartphone 3D Imaging use cases

Use-cases and opportunities for the **front** 3D camera

Easy unlocking		
Morphing Augmented reality		
Payment Face recognition		
Gaming Avatar		
Enhanced video call		
Holographic displays		


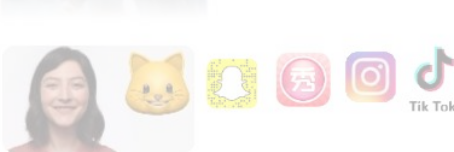
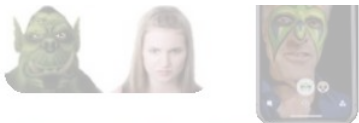


Use-cases and opportunities for the **rear** 3D camera

Better photography		
Augmented reality		
Gaming		
Commercial		
3D printing		
Others?		

SMARTPHONE 3D IMAGING AND LASER AUTOFOCUS





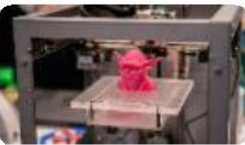

Smartphone 3D Imaging use cases

Use-cases and opportunities for the front 3D camera

Easy unlocking		✓
Morphing Augmented reality		✓
Payment Face recognition		✓
Gaming Avatar		
Enhanced video call		
Holographic displays		

Interesting, but out of scope

Use-cases and opportunities for the rear 3D camera

Better photography		✓
Augmented reality		✓
Gaming		✓
Commercial		
3D printing		
Others?		

SMARTPHONE 3D IMAGING AND LASER AUTOFOCUS

Smartphone 3D Imaging use cases

Photography
(space-resolved
laser autofocus)



selective
focus &
bokeh



Continuous
mode autofocus

SMARTPHONE 3D IMAGING AND LASER AUTOFOCUS

Smartphone 3D Imaging use cases

Mixed Reality Gaming



SMARTPHONE 3D IMAGING AND LASER AUTOFOCUS

Smartphone 3D Imaging use cases

Commercial / Shopping



Virtual mall



Fitting clothes



AR Advertisement



Reality curation

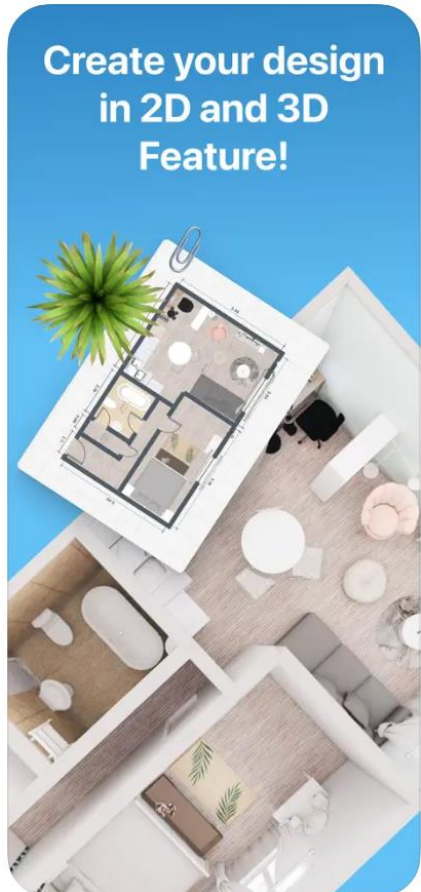


Interior decorating

SMARTPHONE 3D IMAGING AND LASER AUTOFOCUS

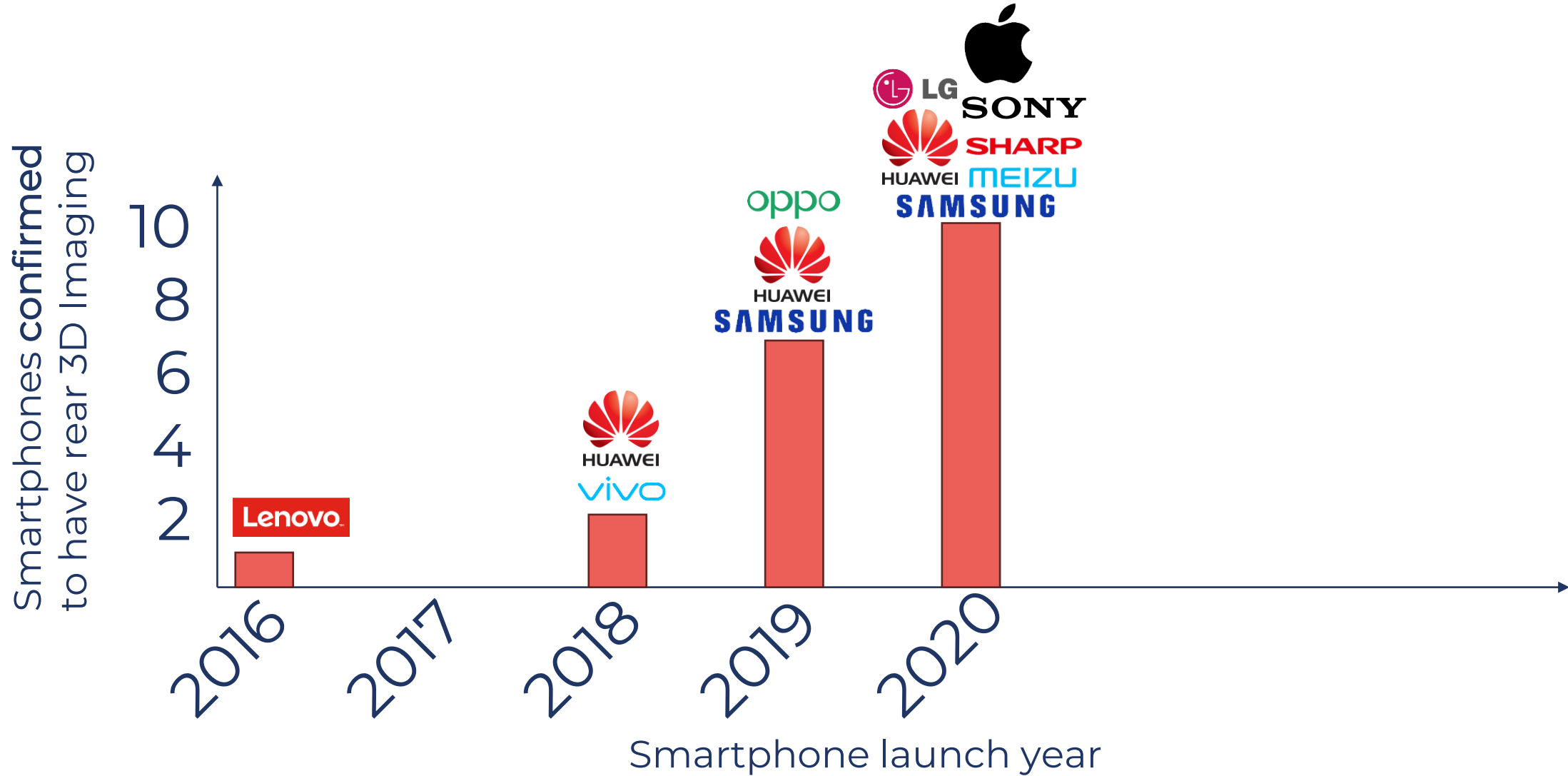
Smartphone 3D Imaging use cases

and more...



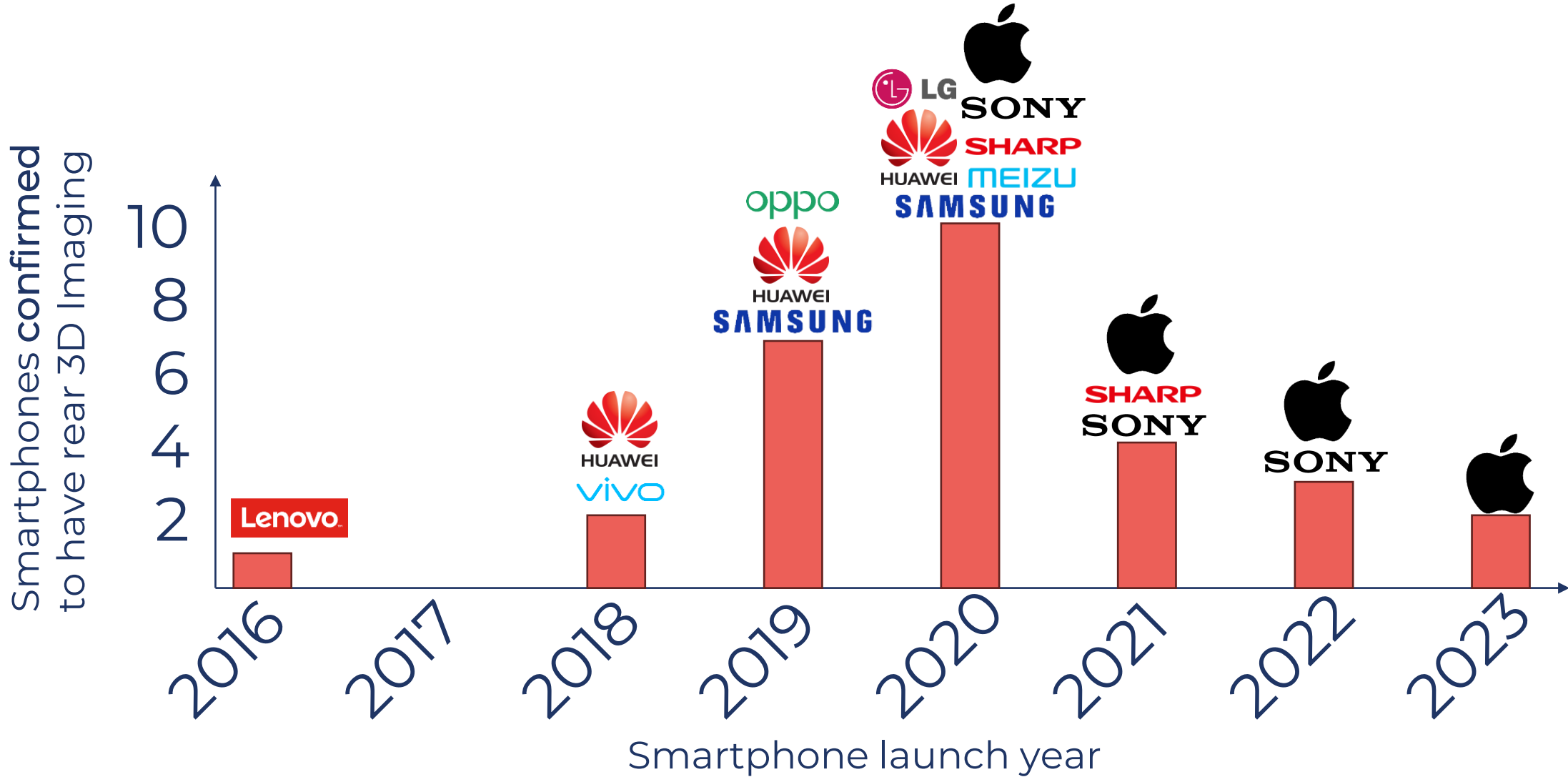
SMARTPHONE 3D IMAGING AND LASER AUTOFOCUS

Incidence of Rear-facing 3D Imaging



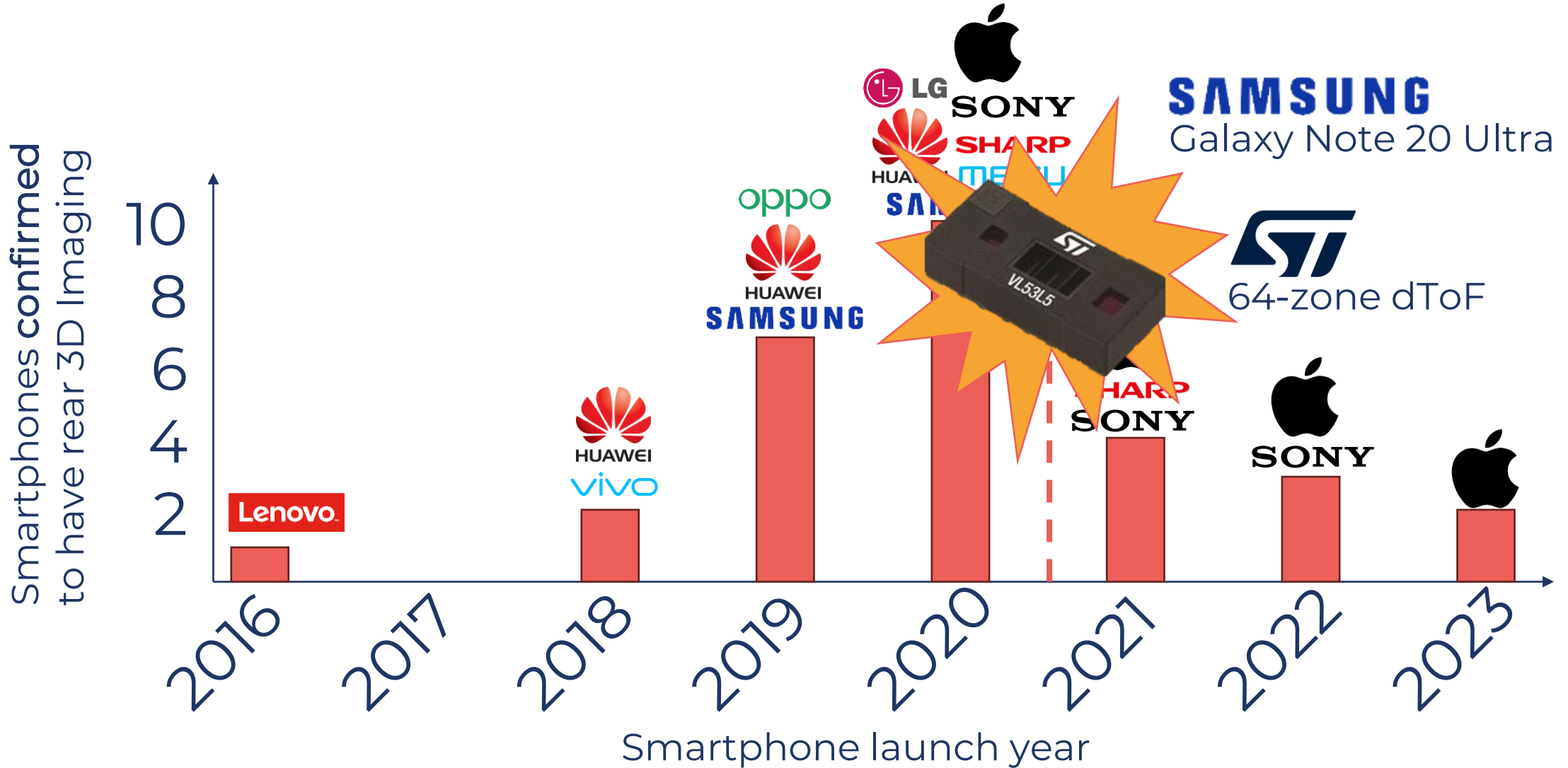
SMARTPHONE 3D IMAGING AND LASER AUTOFOCUS

Incidence of Rear-facing 3D Imaging



SMARTPHONE 3D IMAGING AND LASER AUTOFOCUS



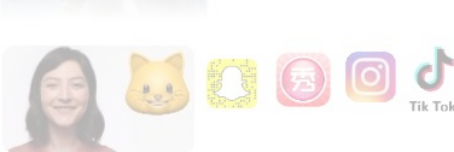









Incidence of Rear-facing 3D Imaging



SMARTPHONE 3D IMAGING AND LASER AUTOFOCUS



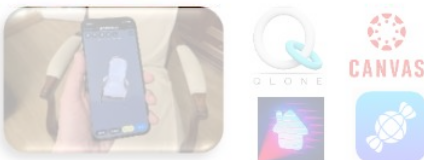



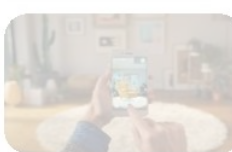



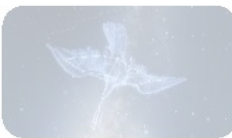

Multizone dToF use cases

Use-cases and opportunities for the **front** 3D camera

Easy unlocking		
Morphing Augmented reality		
Payment Face recognition		
Gaming Avatar		
Enhanced video call		
Holographic displays		

Interesting, but out of scope

Use-cases and opportunities for the **rear** 3D camera

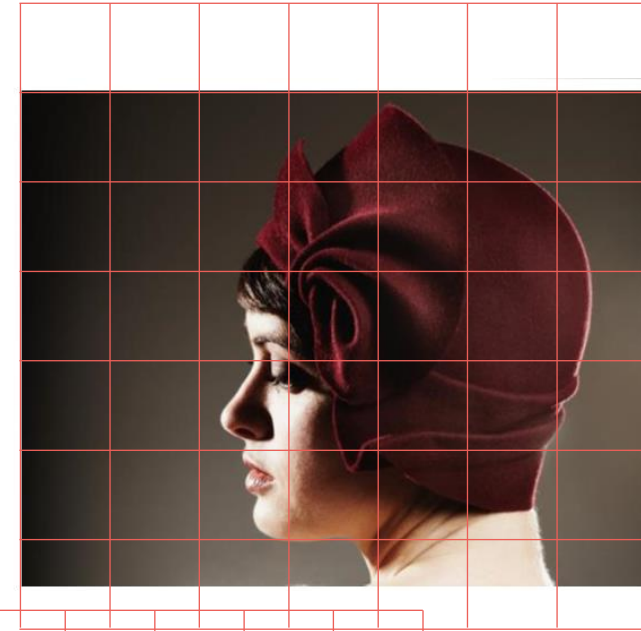
Better photography		
Augmented reality		
Gaming		
Commercial		
3D printing		
Others?		

SMARTPHONE 3D IMAGING AND LASER AUTOFOCUS

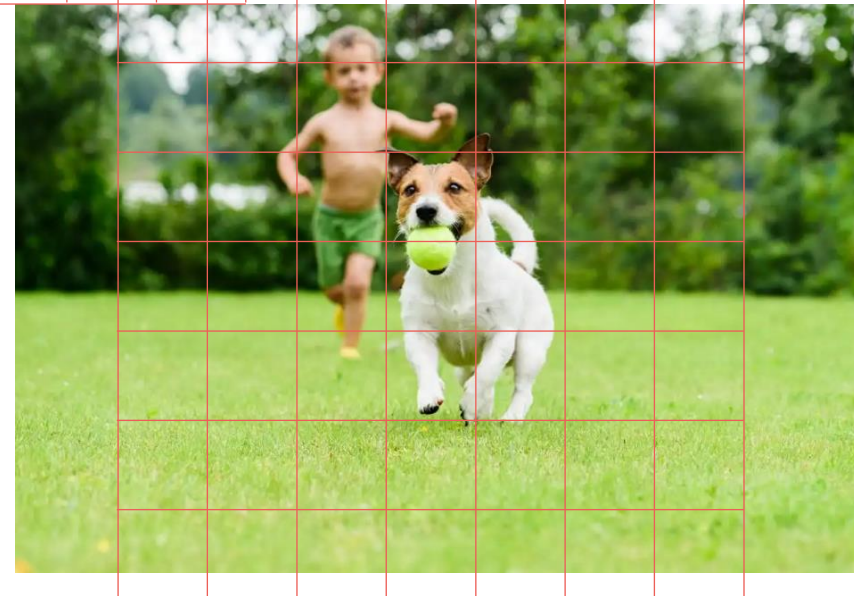
Multi-zone Laser Autofocus

Photography
(space-resolved
laser autofocus)

“Multi-zone”
Laser Autofocus



selective
focus &
bokeh



Continuous
mode autofocus

SMARTPHONE 3D IMAGING AND LASER AUTOFOCUS

Ultra-premium Smartphone Autofocusing Strategies

Passive Autofocus



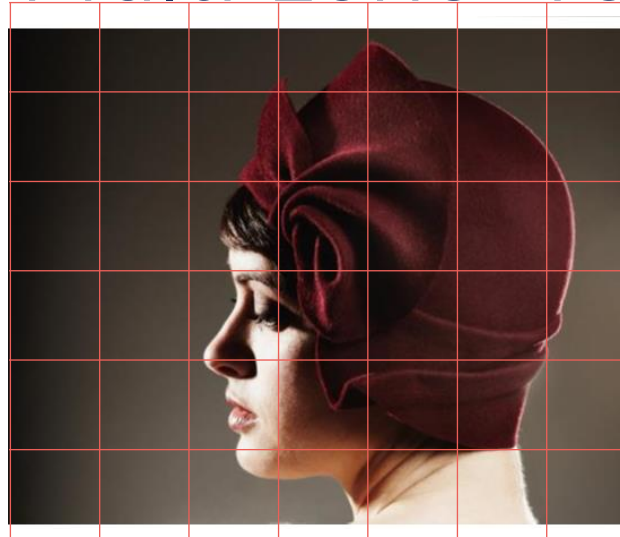
Uses special pixels in the CIS

- Very Inexpensive
- Needs bright, high contrast scene

used by all smartphones

Active Autofocus

“Multi-zone” ToF



- Moderate cost
- Low resolution

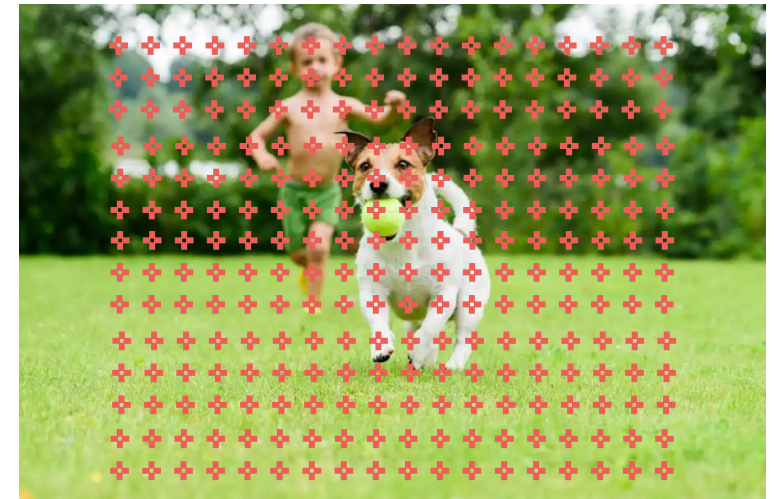


HONOR

SAMSUNG

MEIZU

3D Imaging



- High cost
- High resolution

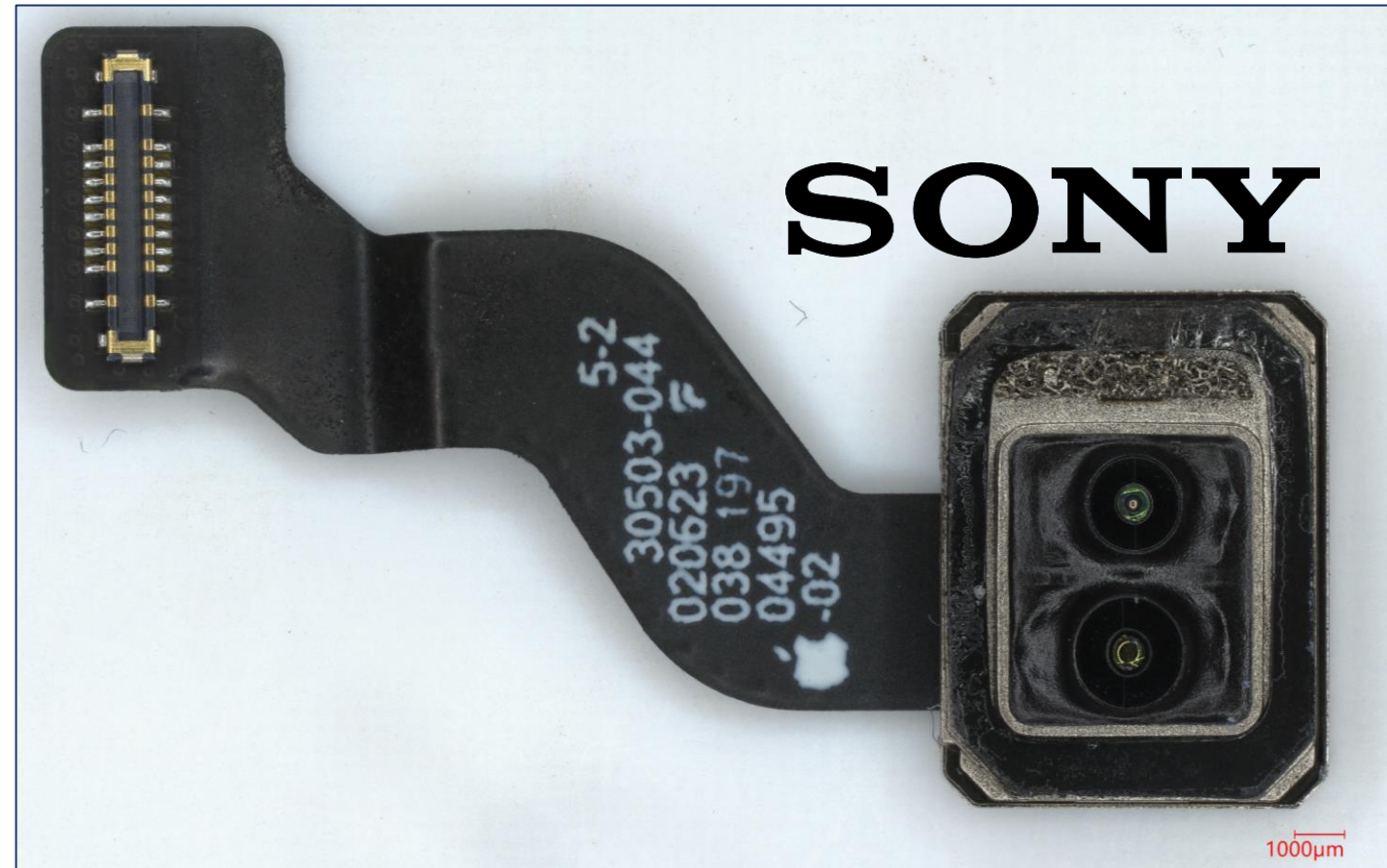
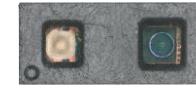


LASER AUTOFOCUS REVERSE COSTING

Presentation Outline

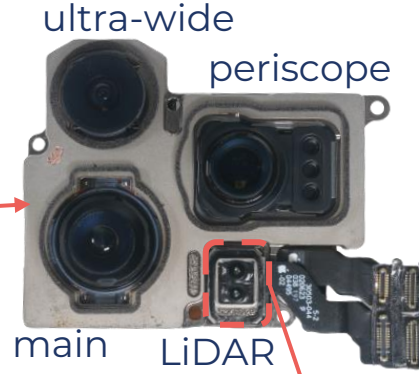
1. Smartphone 3D Imaging and Laser Autofocus
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ams



IPHONE 15 PRO LIDAR MODULE

iPhone 15 Pro Max Teardown



*iPhone 15 Pro Max
Rear Camera
©2024 Yole SystemPlus*

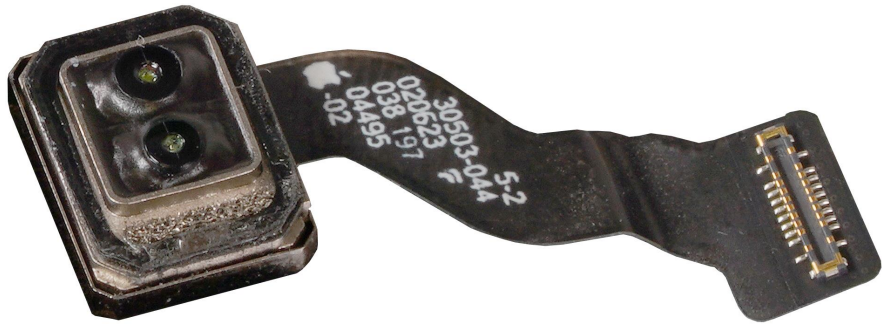
The LiDAR module is part of the rear camera.



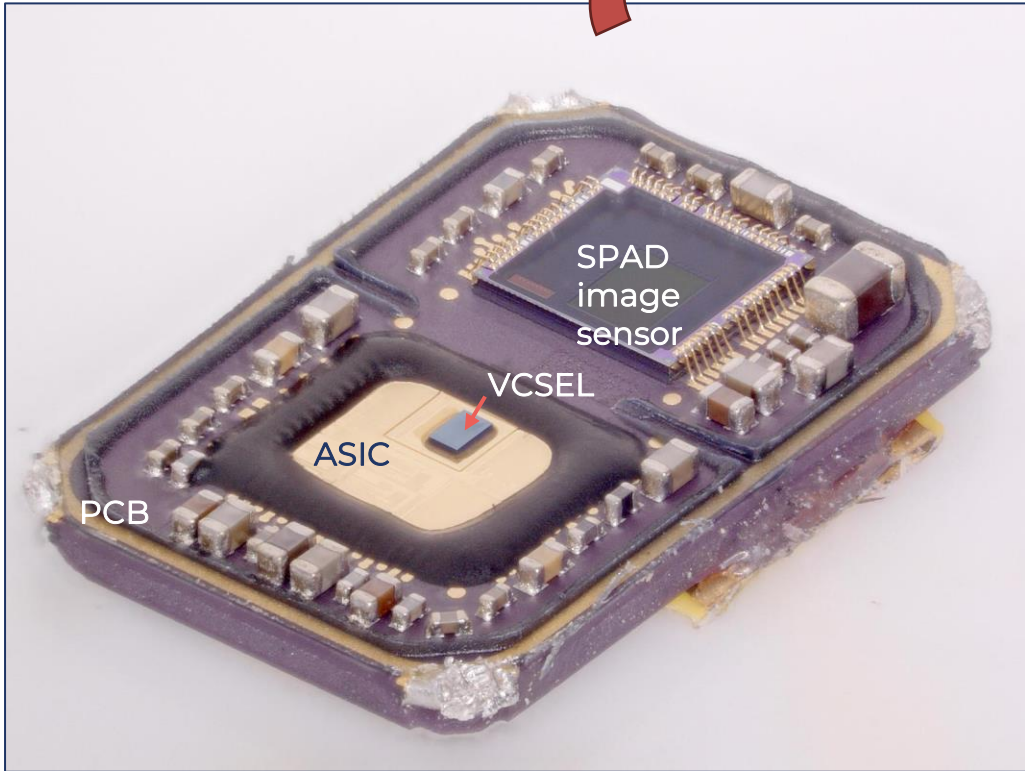
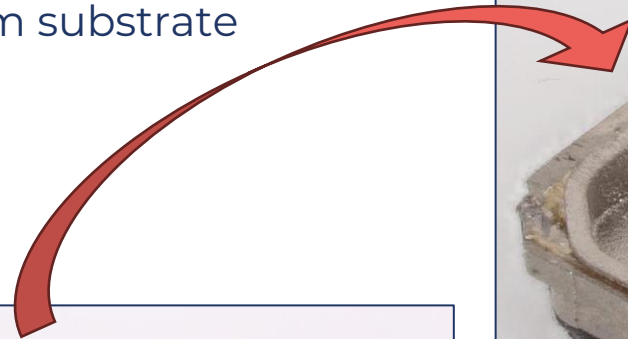
*LiDAR Module
©2024 Yole SystemPlus*

IPHONE 15 PRO LIDAR MODULE

Module Teardown

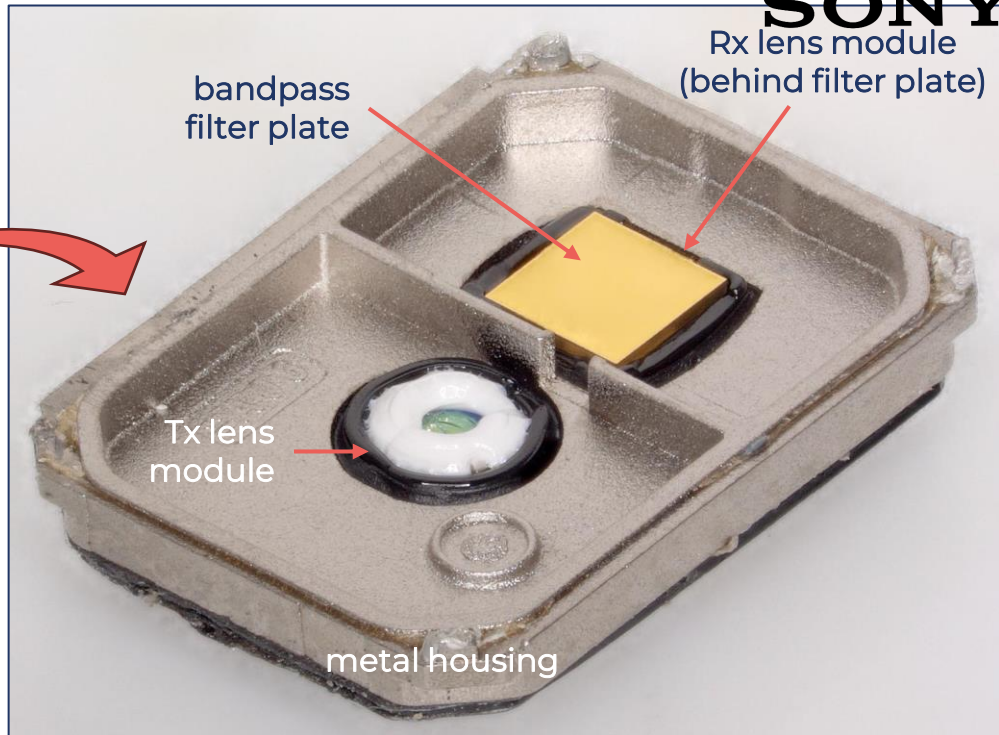


separate optics assembly
from substrate



LidAR Module /with optics removed - Perspective View

©2024 Yole SystemPlus



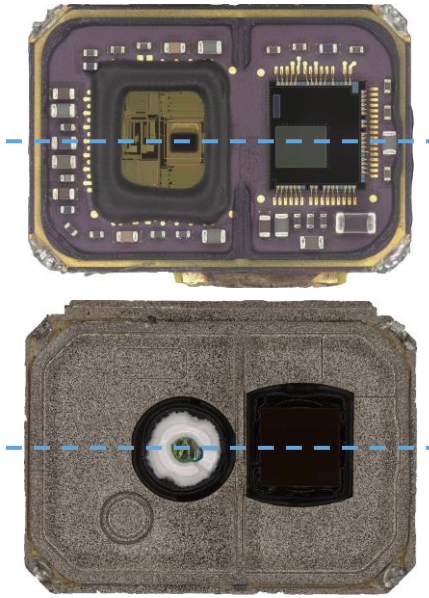
LidAR Module Optics Assembly - Perspective View

©2024 Yole SystemPlus

SONY

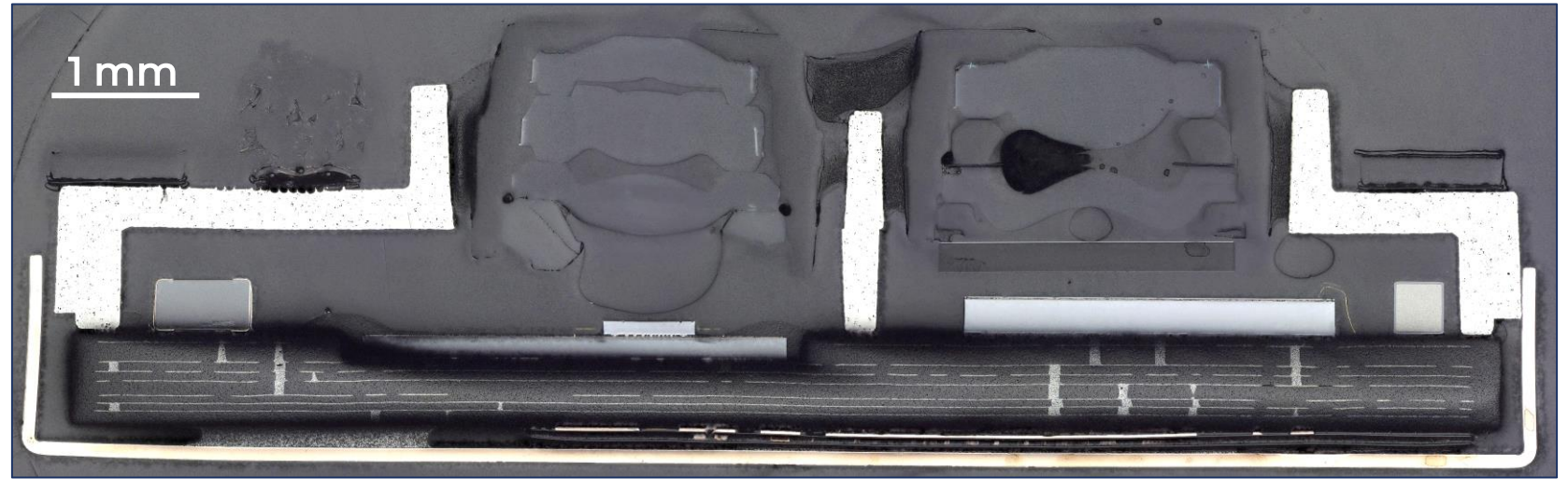
IPHONE 15 PRO LIDAR MODULE

Cross Section

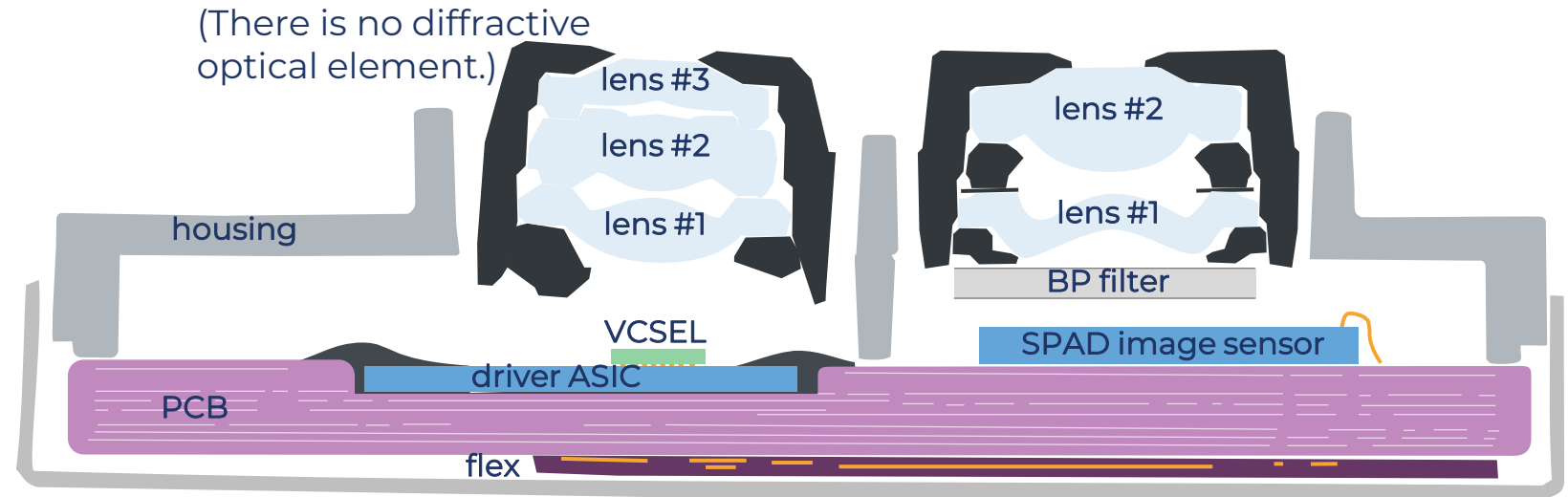


Opened LiDAR Module w/ cross-sectional plane indicated - Optical Views ©2024 Yole SystemPlus

The 3 active dies, the driver ASIC, SPAD image sensor and VCSEL, are all supplied by Sony.



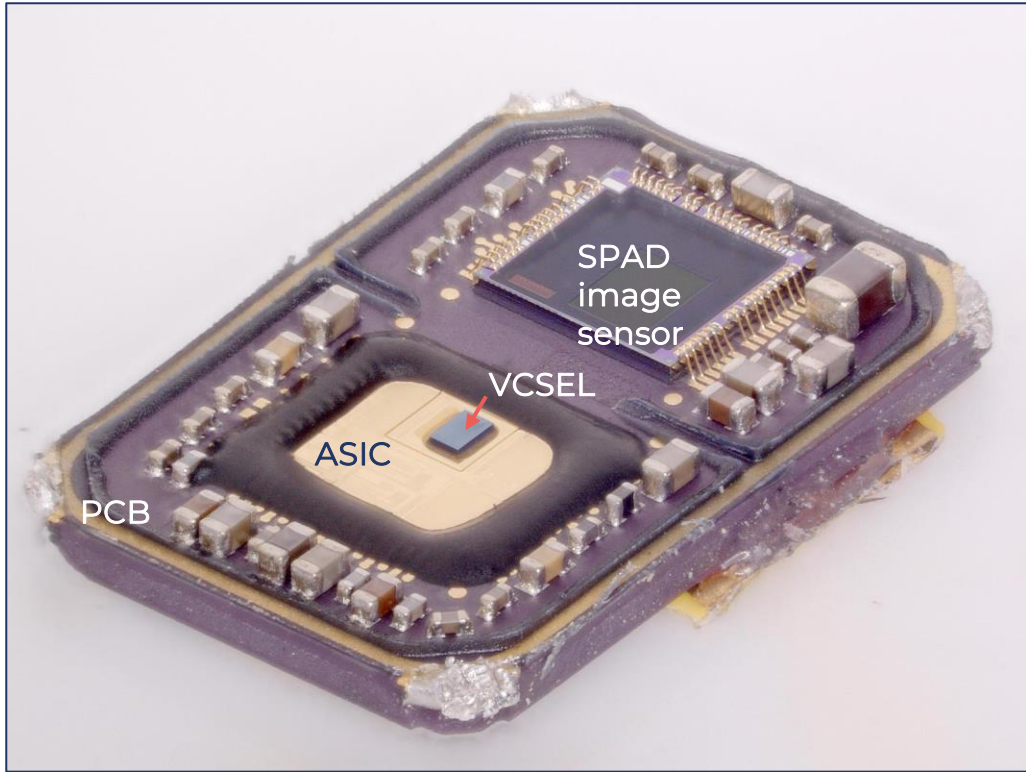
LiDAR Module Cross Section - Optical View ©2024 Yole SystemPlus



(There is no diffractive optical element.)

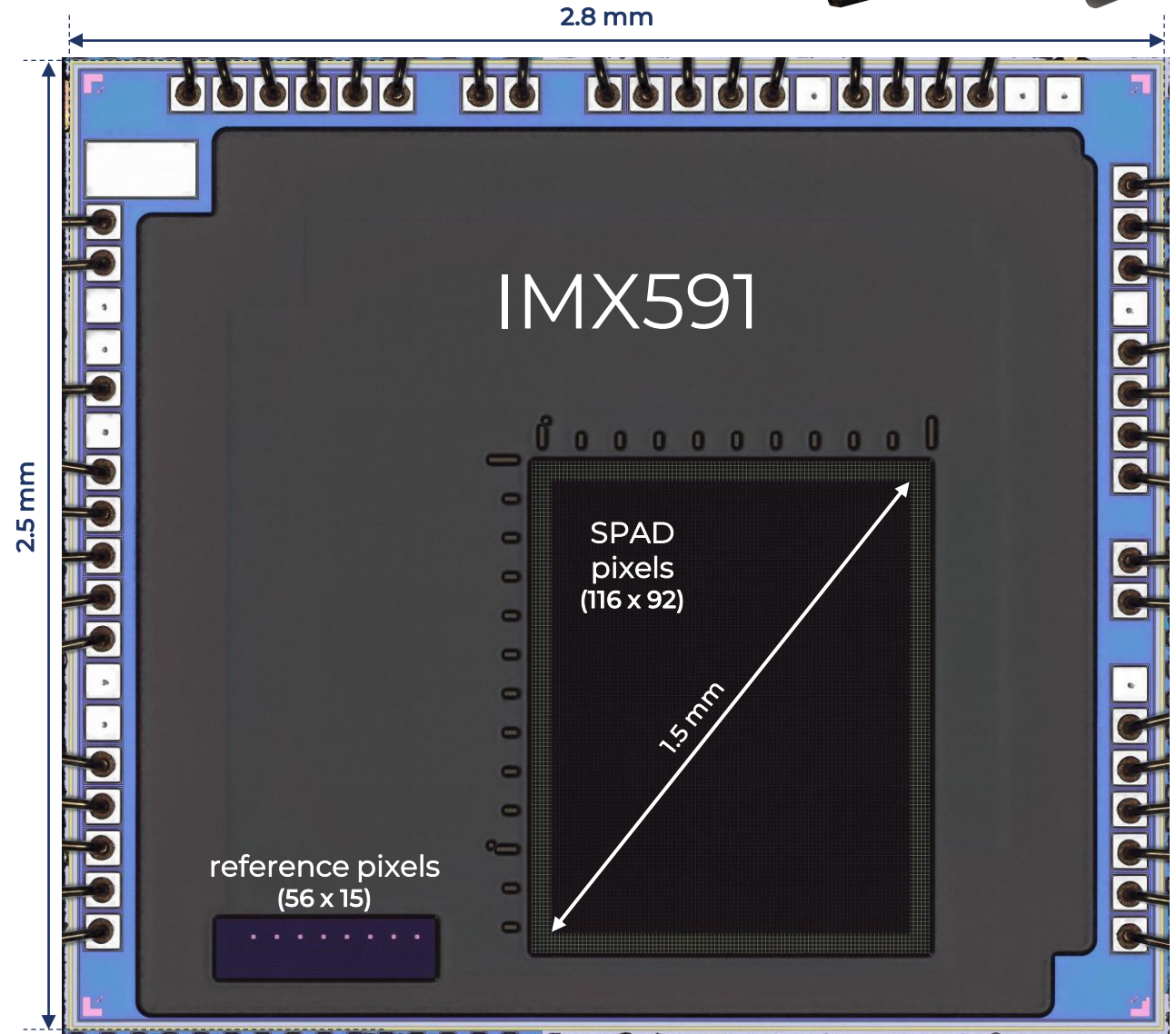
LiDAR Module in Profile - Schematic View ©2024 Yole SystemPlus

IPHONE 15 PRO LIDAR MODULE SPAD CIS Overview



LiDAR Module /with optics removed - Perspective View
©2024 Yole SystemPlus

0.01 Mp SPAD CIS
10 μm SPAD pixel

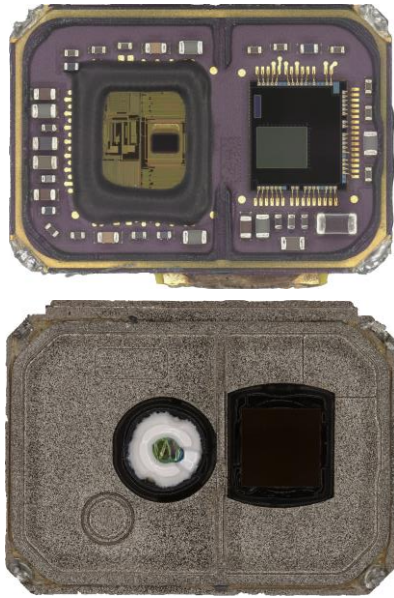


SPAD image Sensor Die Overview - Optical View
©2024 Yole SystemPlus

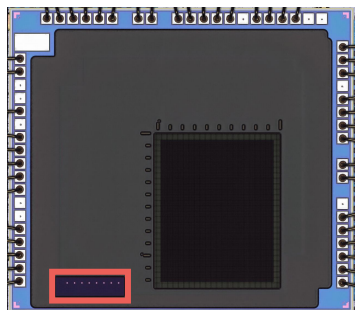


IPHONE 15 PRO LIDAR MODULE

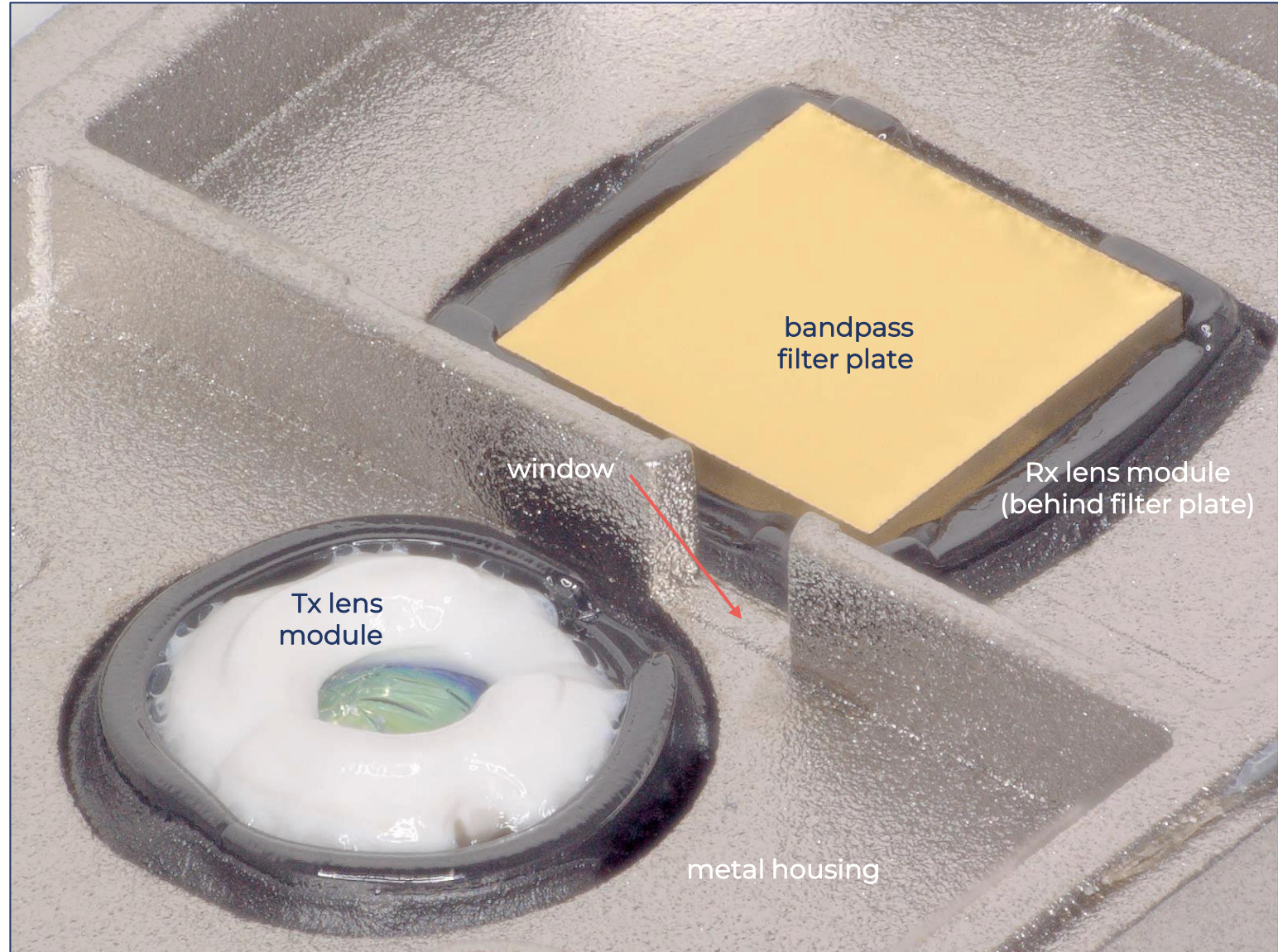
Window



Opened LiDAR Module -
Optical Views
©2024 Yole SystemPlus

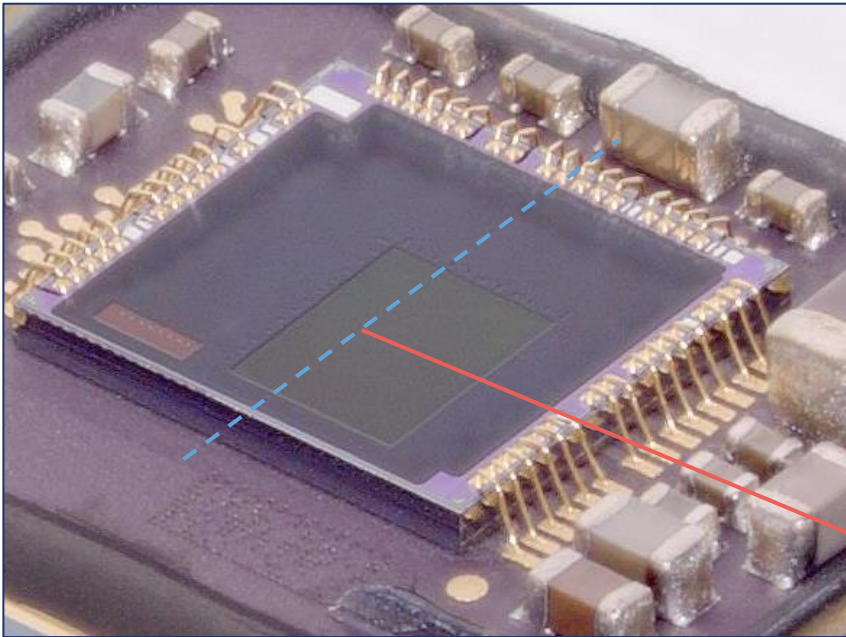


A window in the light-blocking wall transmits a small portion of the emission to give a $t=0$ signal for dToF. We hypothesize that all histogramming is handled by the CIS.

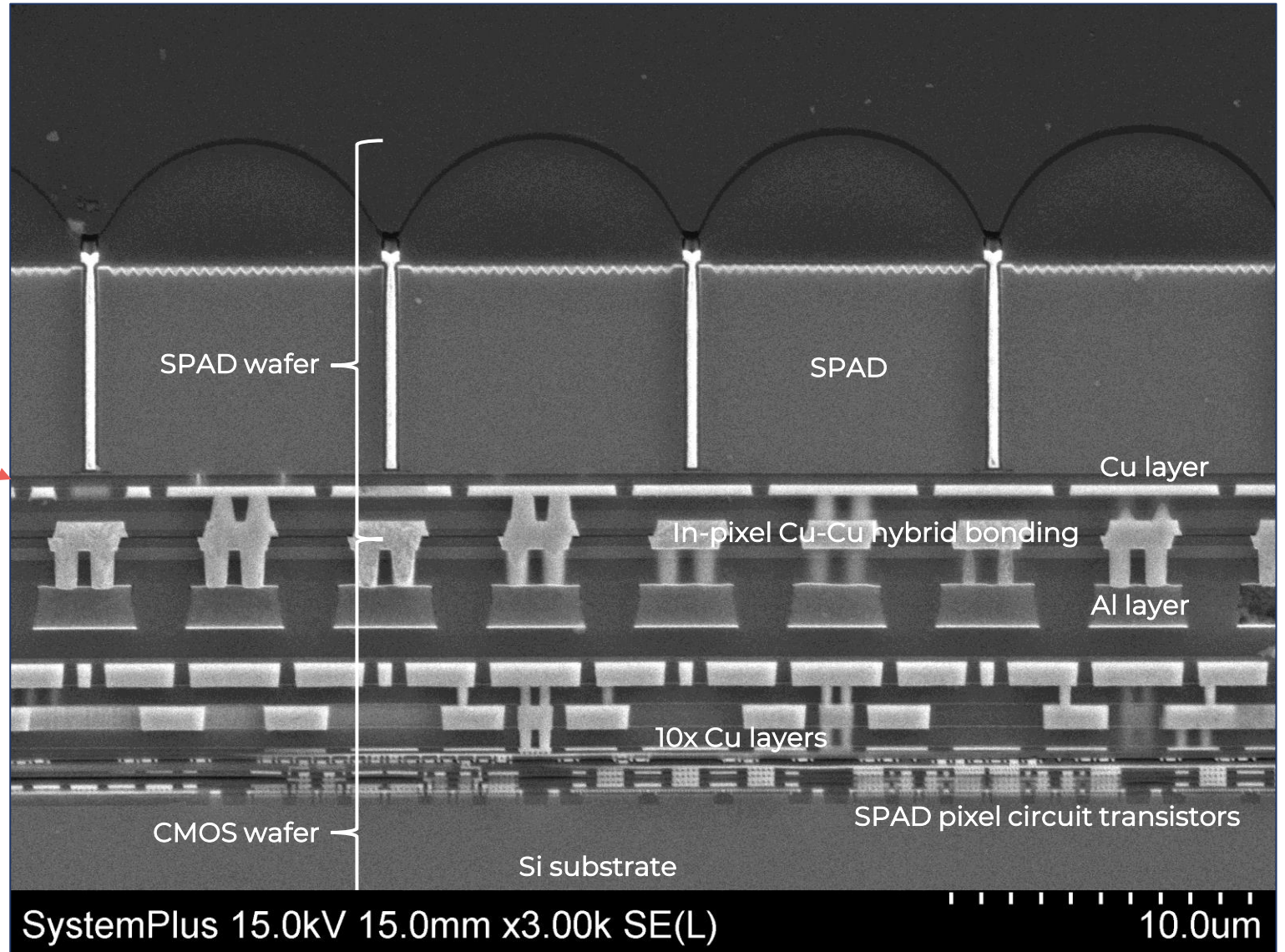


IPHONE 15 PRO LIDAR MODULE

SPAD CIS Overview



Opened LiDAR Module w/ cross-sectional plane indicated - Optical View ©2024 Yole SystemPlus



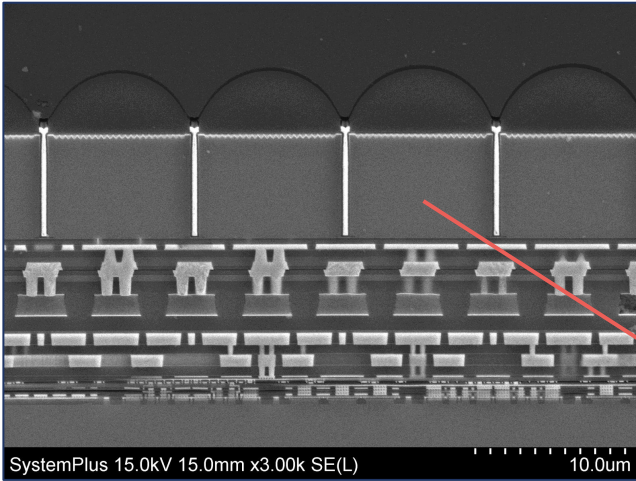
Cross Section through the SPAD Pixel Array - SEM View ©2024 Yole SystemPlus

3D integrated BSI

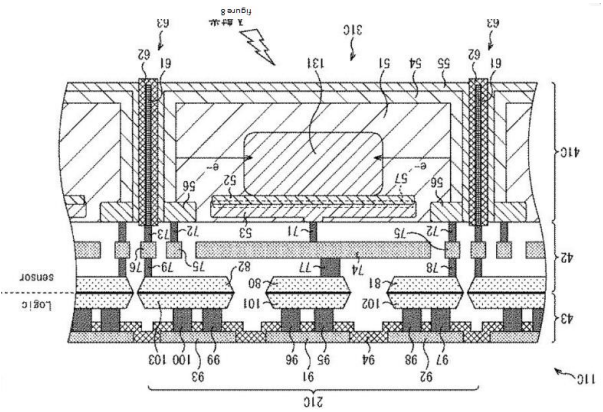


IPHONE 15 PRO LIDAR MODULE

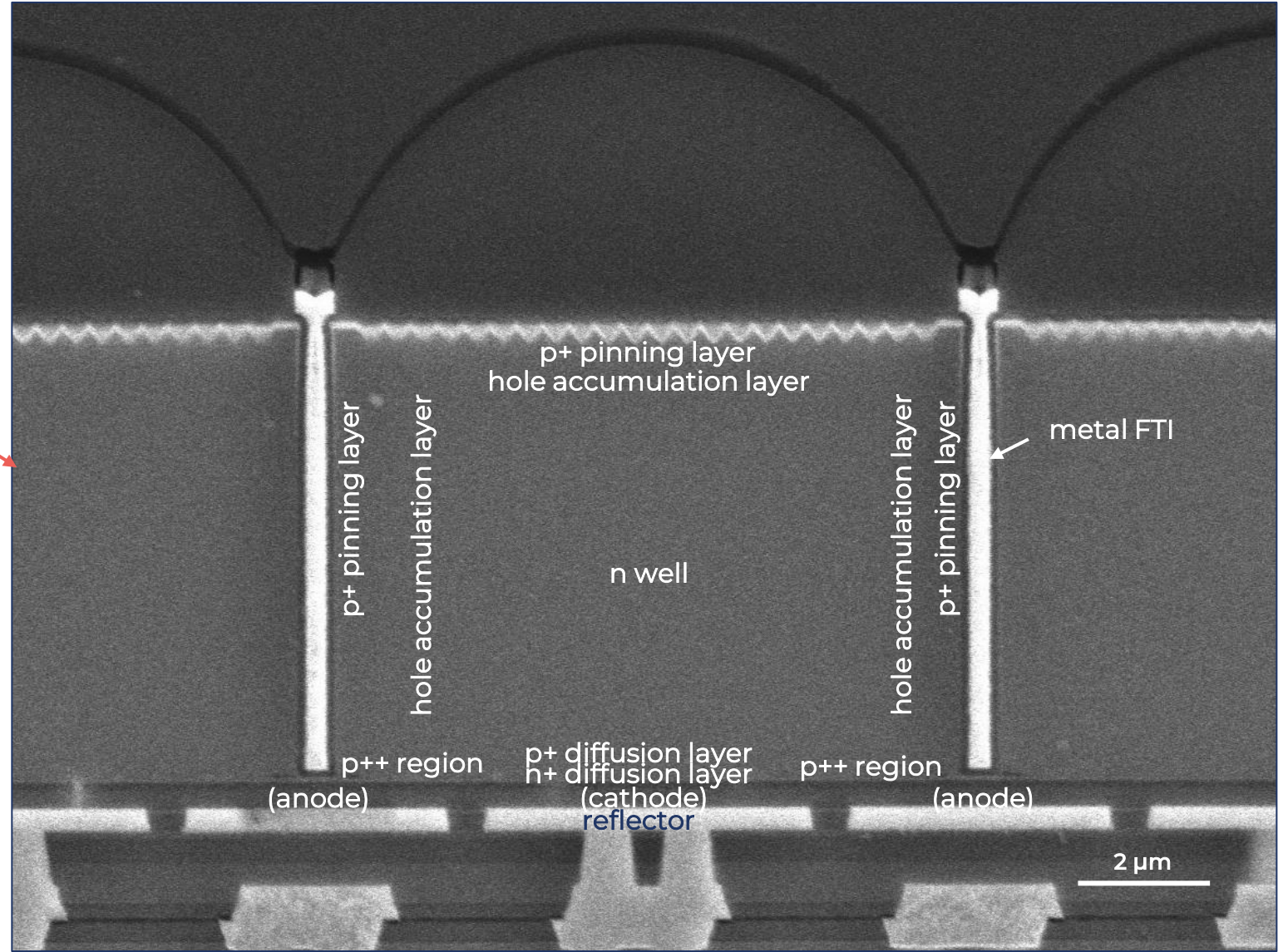
SPAD CIS Overview



Cross Section through the SPAD Pixel Array
- SEM View ©2024 Yole SystemPlus



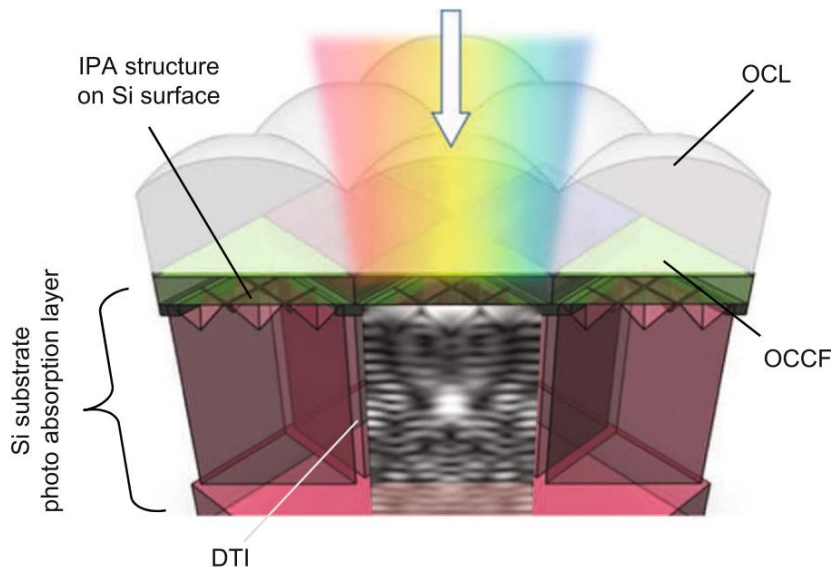
[1] Sony semiconductor patent
Publication number JP,2018-088488A



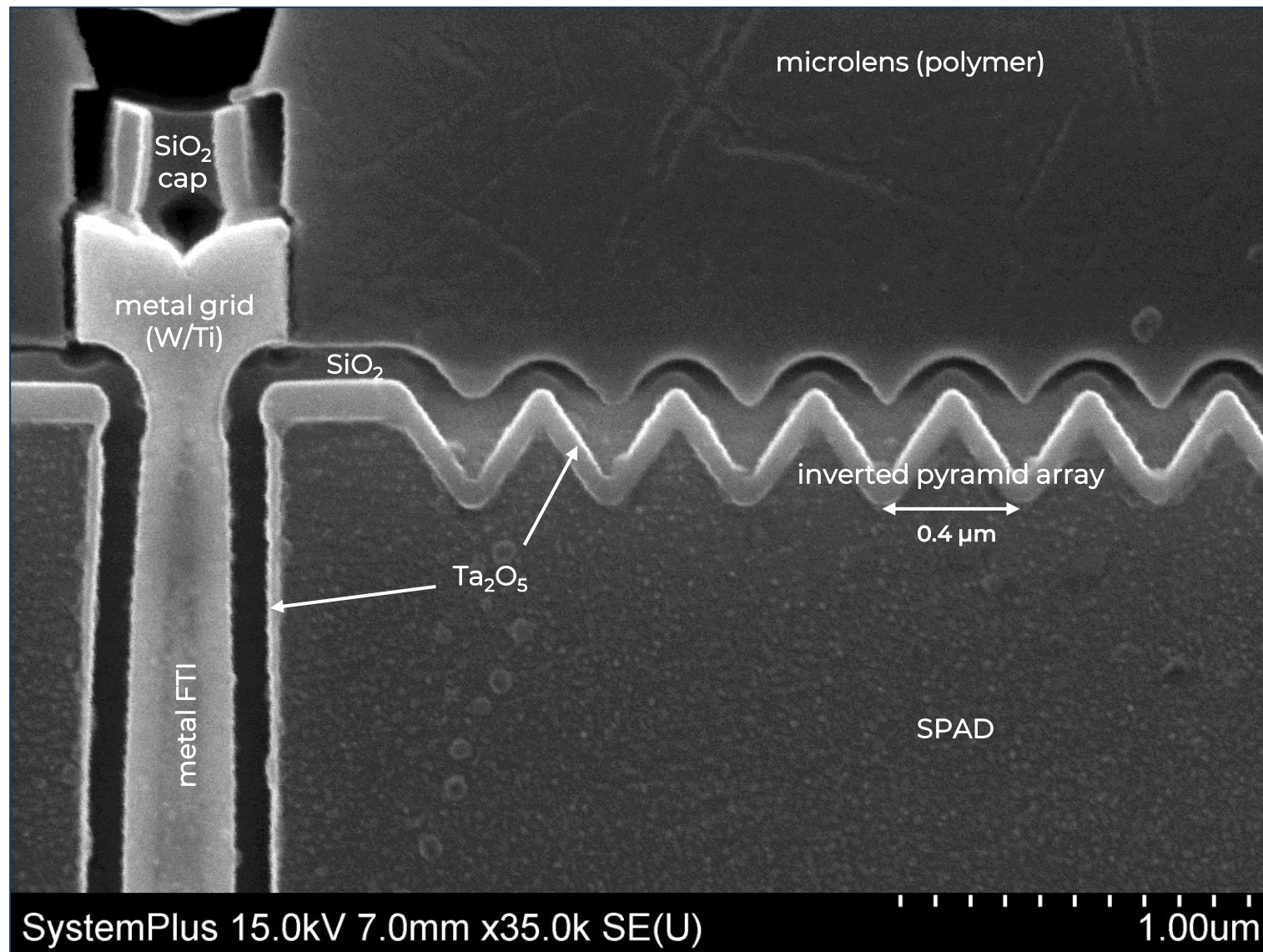
Cross Section of BSI SPAD with 3D Integration - SEM View ©2024 Yole SystemPlus

IPHONE 15 PRO LIDAR MODULE

SPAD CIS Overview



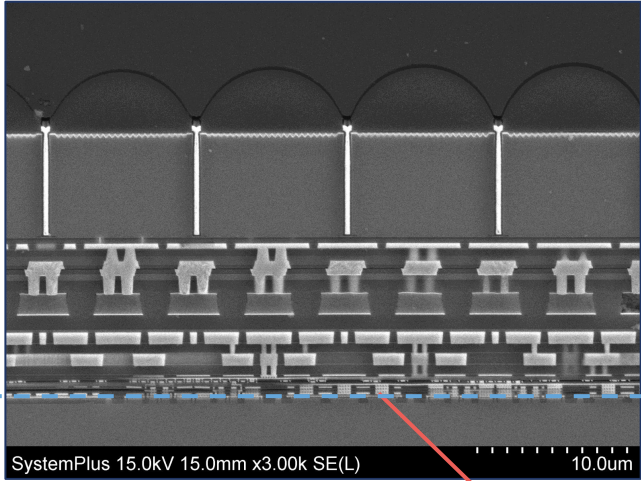
Yokogawa, S., Oshiyama, I., Ikeda, H. *et al.* IR sensitivity enhancement of CMOS Image Sensor with diffractive light trapping pixels. *Sci Rep* **7**, 3832 (2017).
<https://doi.org/10.1038/s41598-017-04200-y>



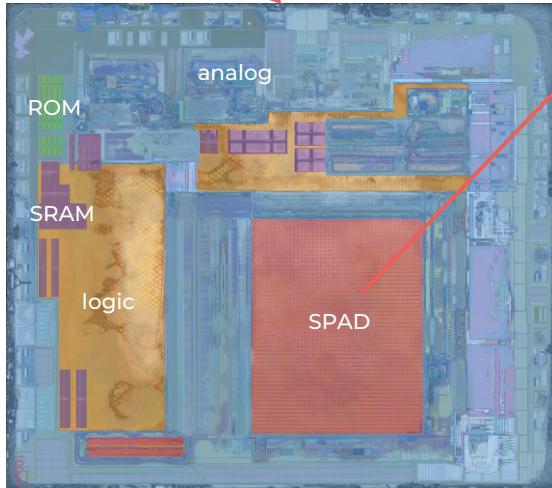
Cross Section through of Inverted Pyramid Array and Metal Grid - SEM View ©2024 Yole SystemPlus

IPHONE 15 PRO LIDAR MODULE

SPAD CIS Overview

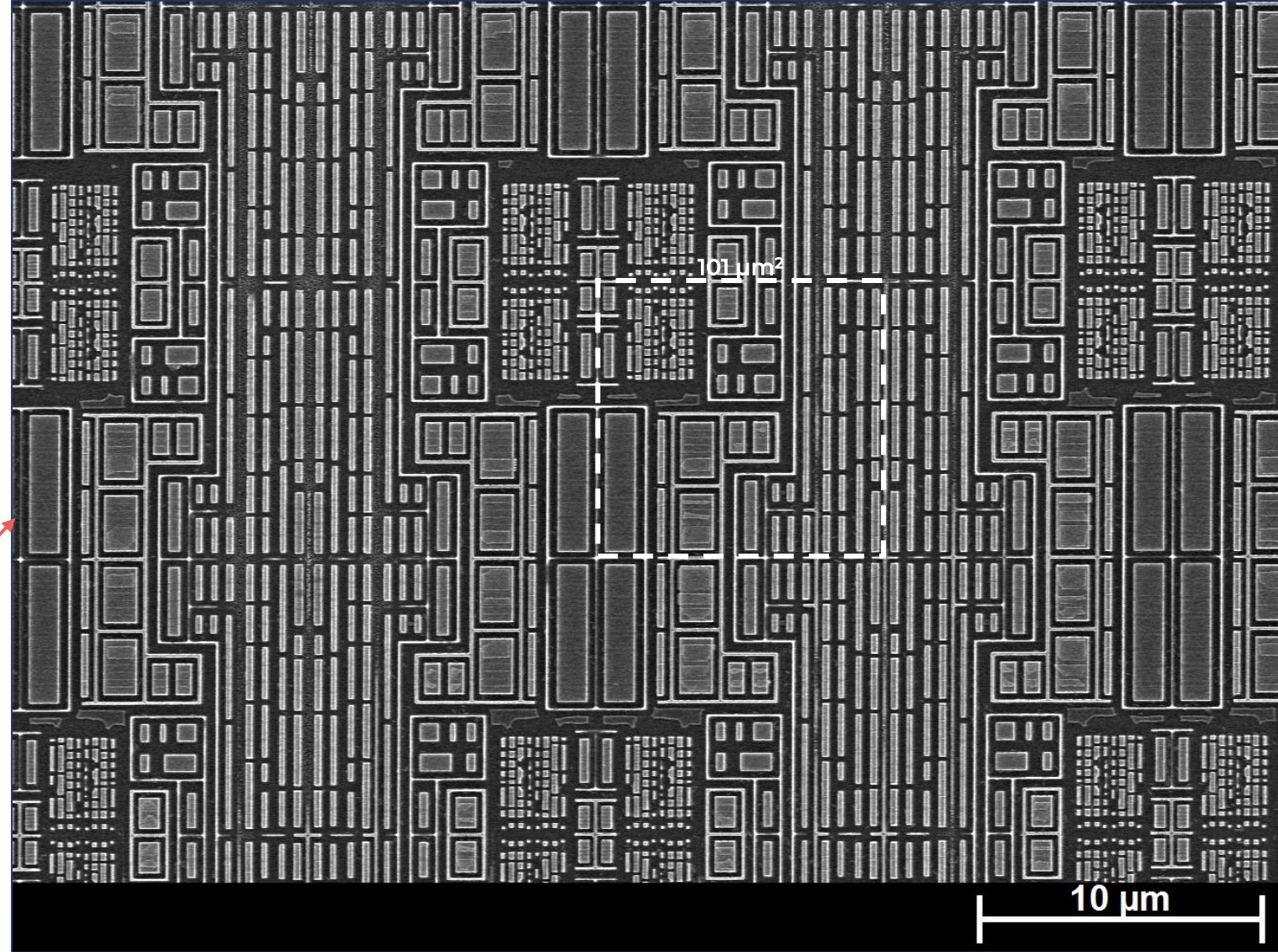


Cross Section through the SPAD Pixel Array - SEM View
©2024 Yole SystemPlus



Die Overview w/ Main Blocks

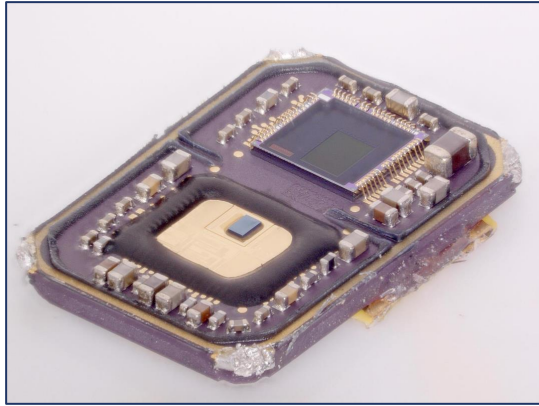
©2024 Yole SystemPlus



SPAD circuit transistors in the SPAD Block - SEM View ©2024 Yole SystemPlus

IPHONE 15 PRO LIDAR

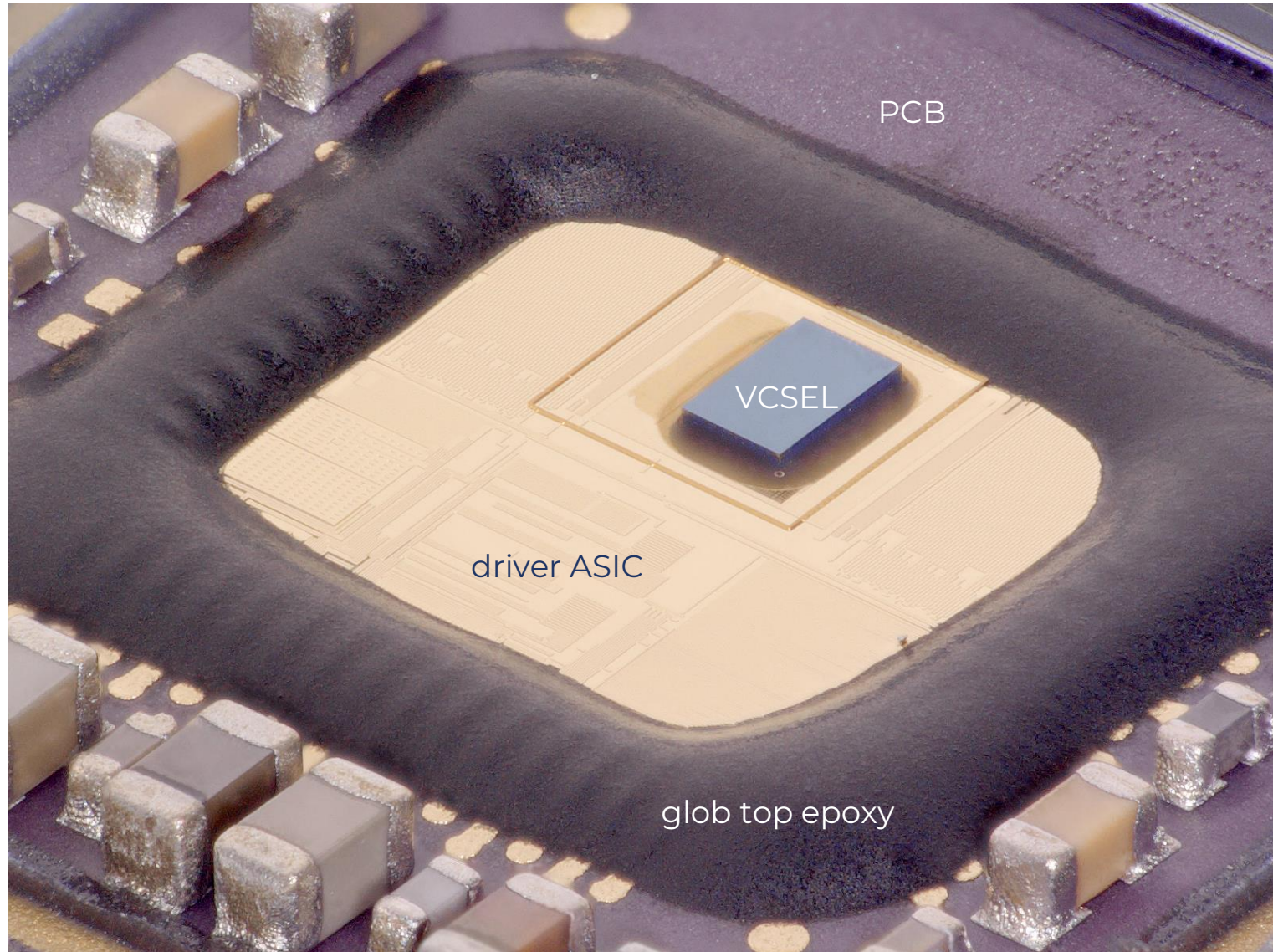
VCSEL+Driver Overview



*LiDAR Module /with optics removed
- Perspective View ©2024 Yole SystemPlus*

The VCSEL is flip-chip bumped directly onto the driver ASIC.

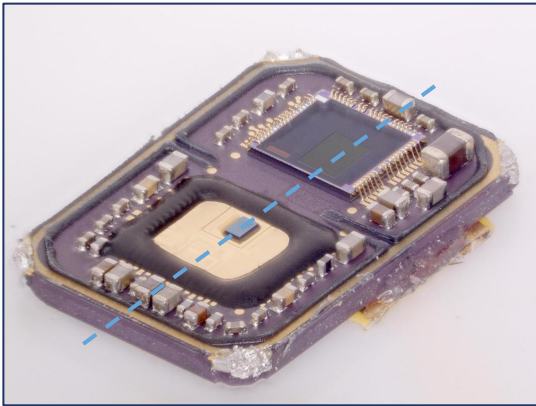
Wirebonds are covered by glob top epoxy.



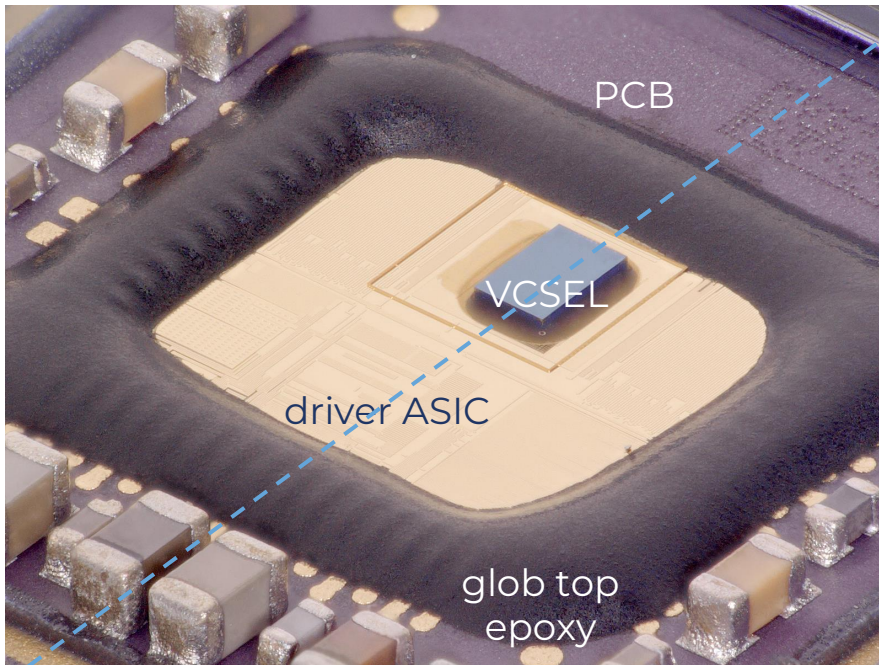
Driver ASIC Overview - Perspective View ©2024 Yole SystemPlus

REVERSE COSTING METHODOLOGY

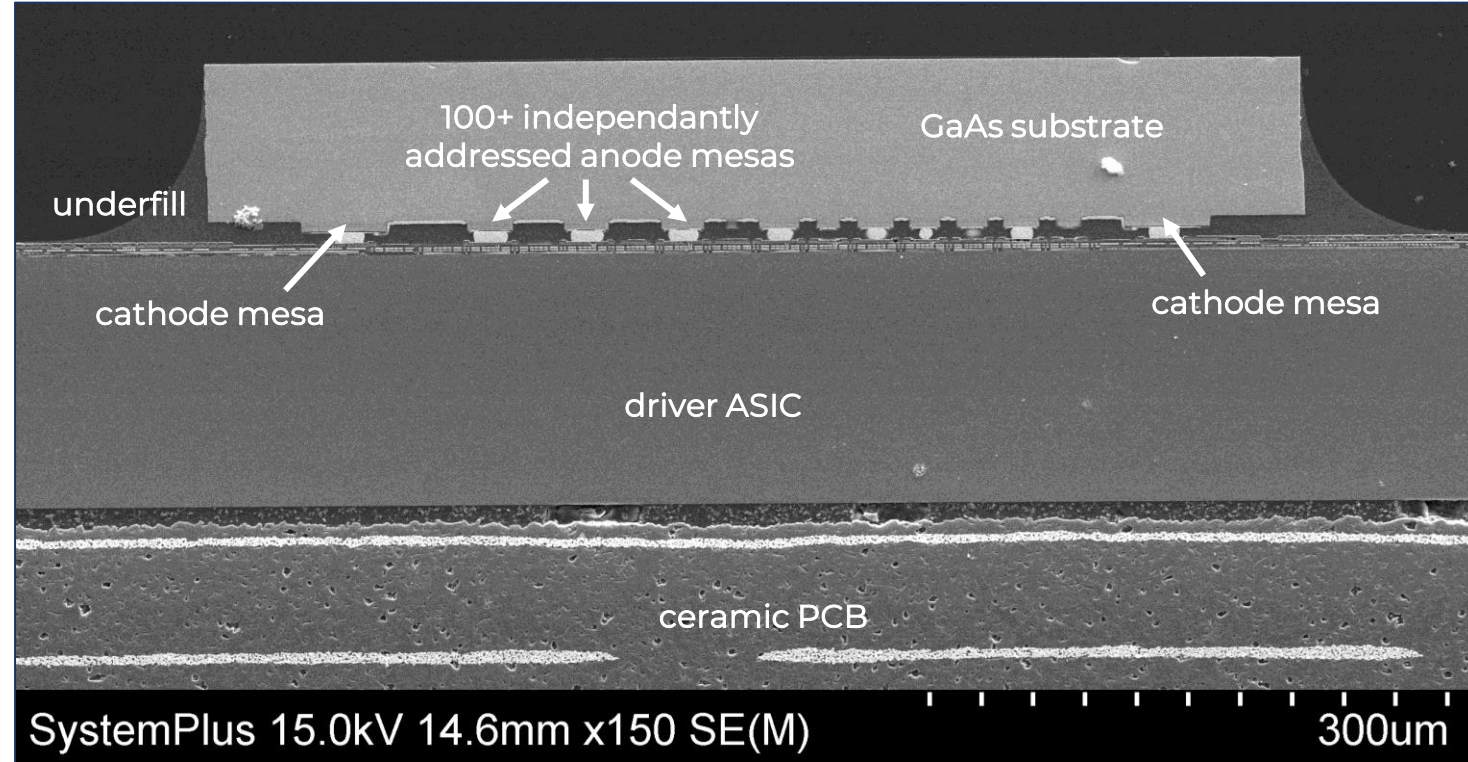
VCSEL+Driver Overview



*LiDAR Module /with optics removed
- Perspective View ©2024 Yole SystemPlus*



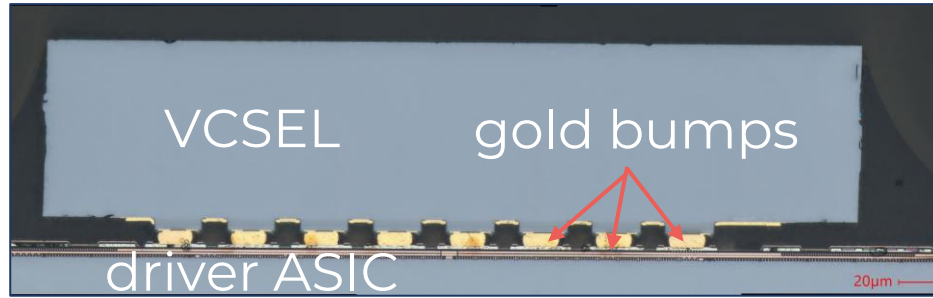
*Driver ASIC Overview - Perspective View
©2024 Yole SystemPlus*



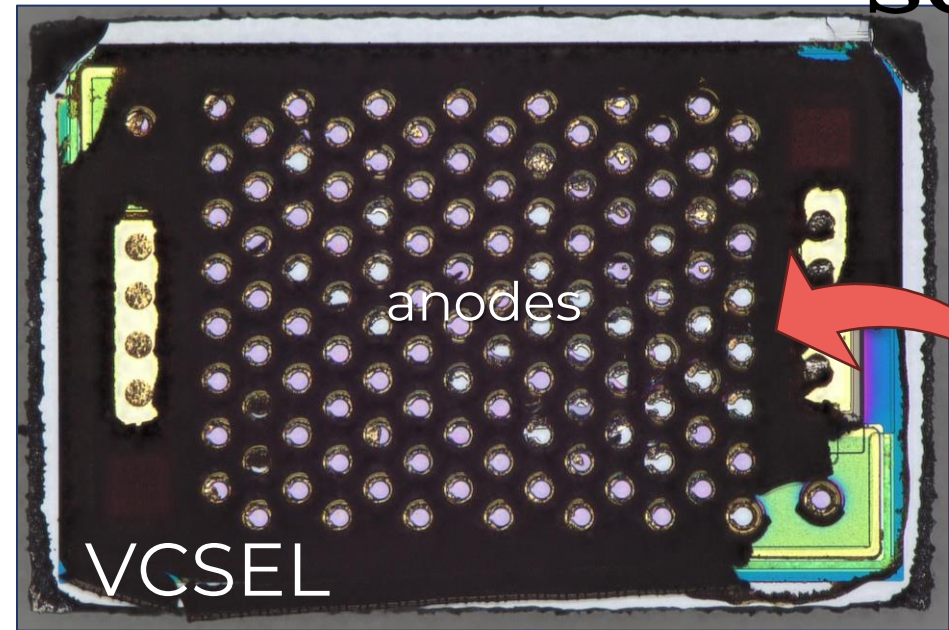
VCSEL Cross Section - Optical Overview ©2024 Yole SystemPlus

REVERSE COSTING METHODOLOGY

VCSEL+Driver Overview



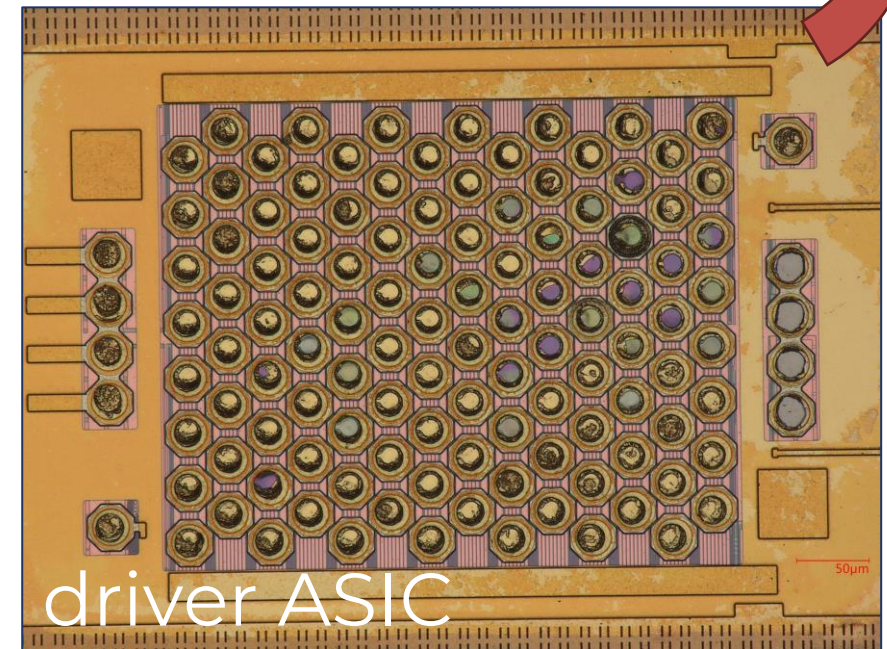
Cross-Section of VCSEL showing gold-bump connections to the driver ASIC - Optical View ©2024 Yole SystemPlus



Bottom View of VCSEL with underfill partially removed - Optical View ©2024 Yole SystemPlus

The VCSEL is gold bumped to the driver ASIC such that **every anode is independently addressed**. The cathode is shared. There are a total of 122 bumps.

This is a cost-saving strategy as it removes the need for the diffractive optic.



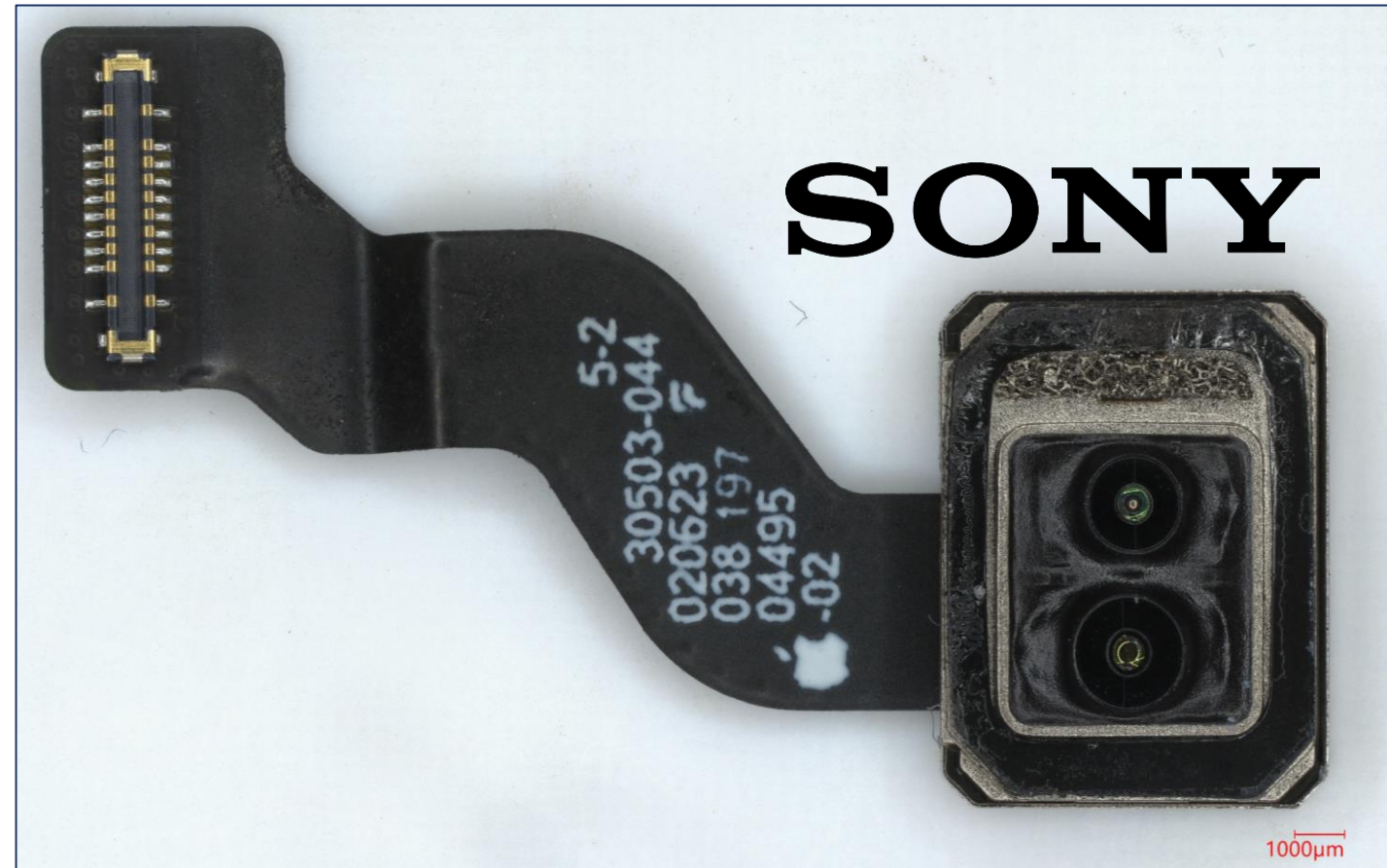
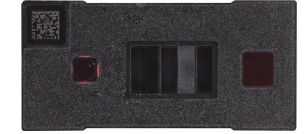
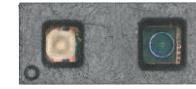
Top View of Driver ASIC where it connects to the VCSEL - Optical View ©2024 Yole SystemPlus

LASER AUTOFOCUS REVERSE COSTING

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 - TMF8821 by ams AG
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5. Results & Discussion

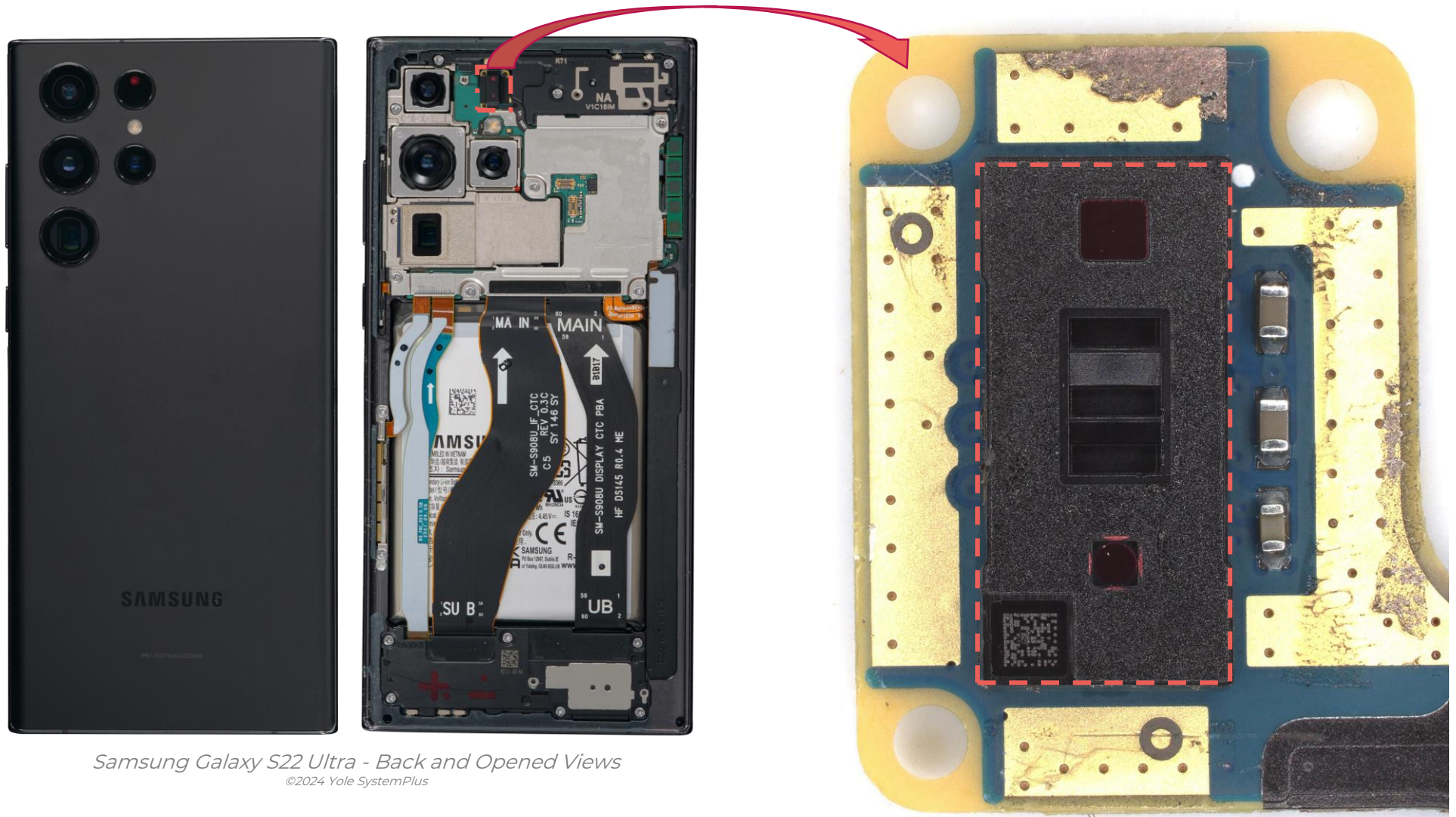
ams



VL53L5

Galaxy S22 Ultra Teardown

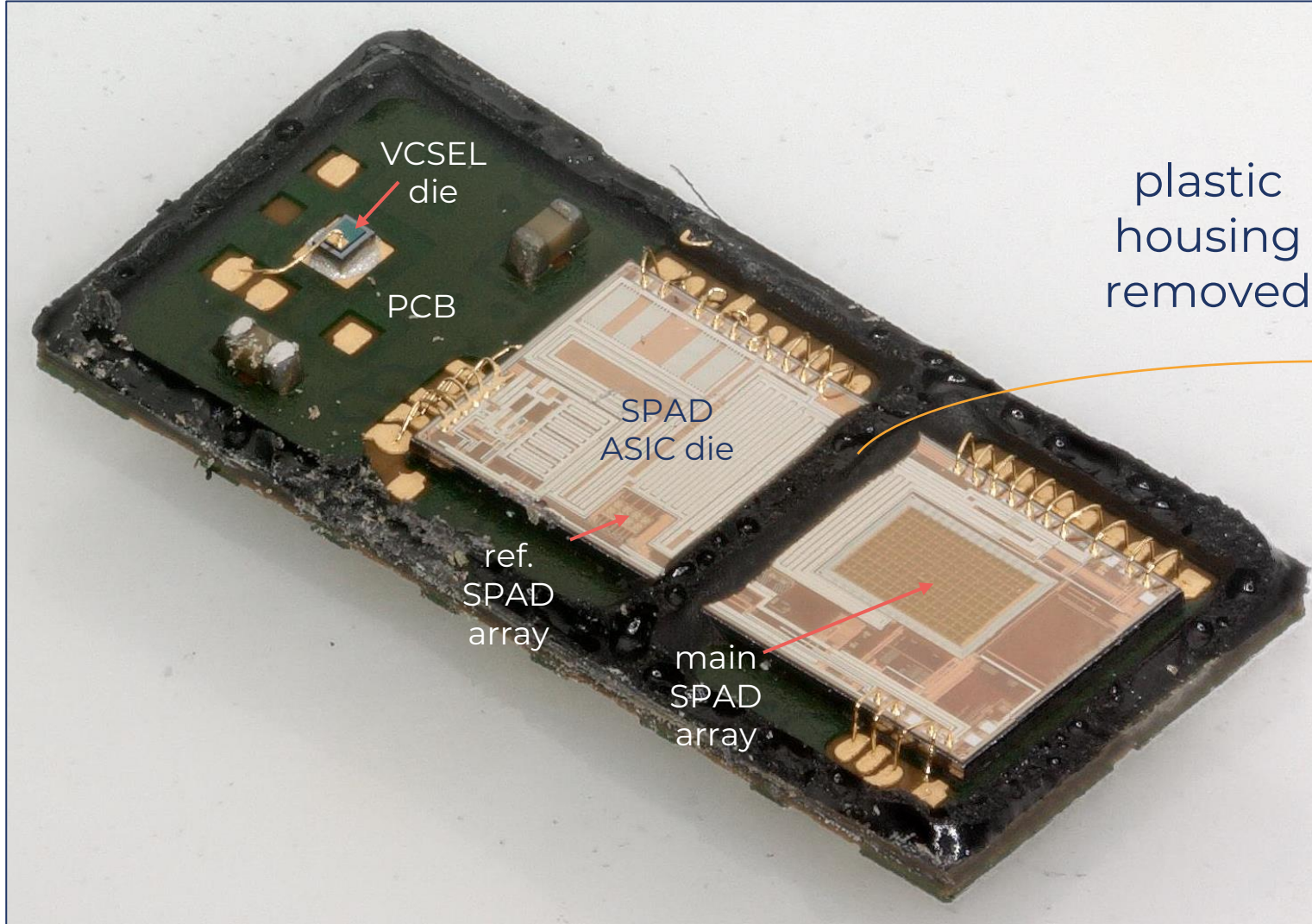
- We've also found the VL53L5 in the
- Galaxy S21 Ultra,
 - Galaxy Note20 Ultra,
 - Xiaomi 12S Ultra,
 - Xiaomi Mi 11 Ultra, and
 - Meizu 20 INF



Samsung Galaxy S22 Ultra - Back and Opened Views
©2024 Yole SystemPlus

STMicrollectronics VL53L5 Depth Ranger Module on Smartphone PCB
©2024 Yole SystemPlus

VL53L5 Module Teardown



(not to scale) 



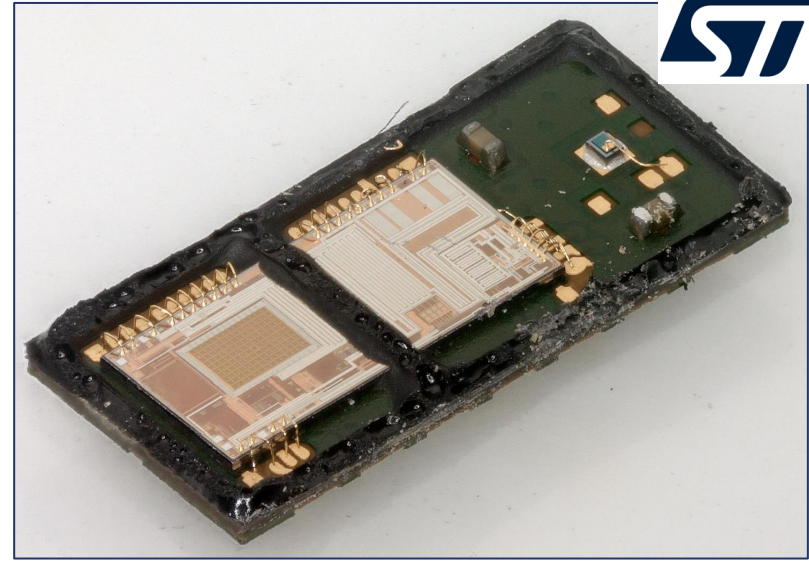
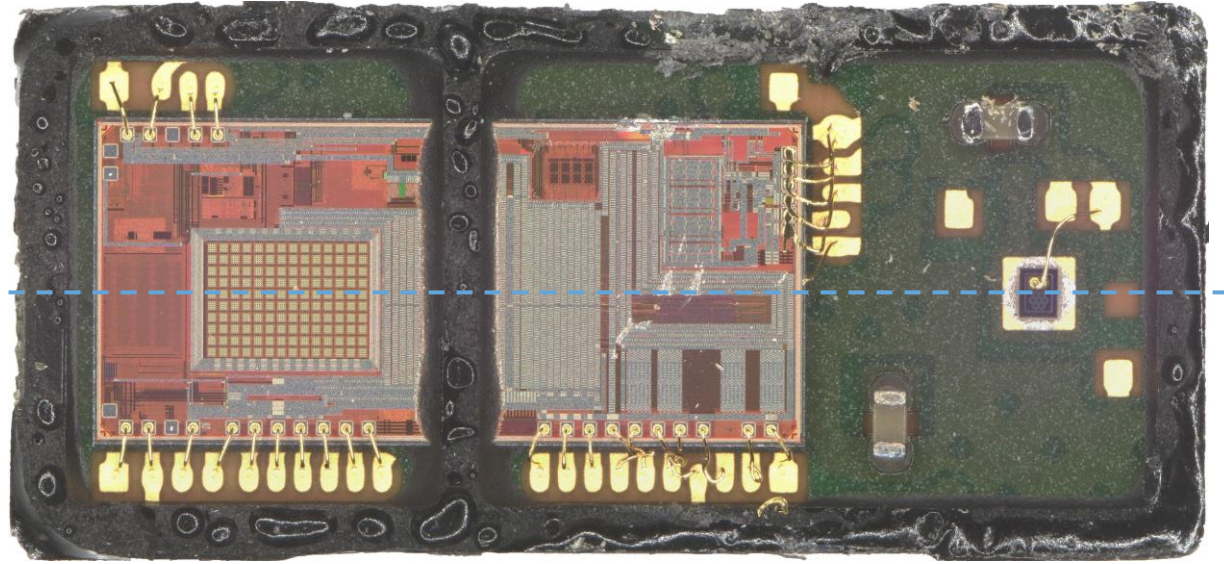
Plastic Housing w/ Diffuser and Fresnel Lens - Bottom View
©2024 Yole SystemPlus

The diffuser and Fresnel-like lens are glued into the plastic housing.

VL53L5 Module with Plastic Housing Removed - Tilted View
©2024 Yole SystemPlus

VL53L5

Cross Section

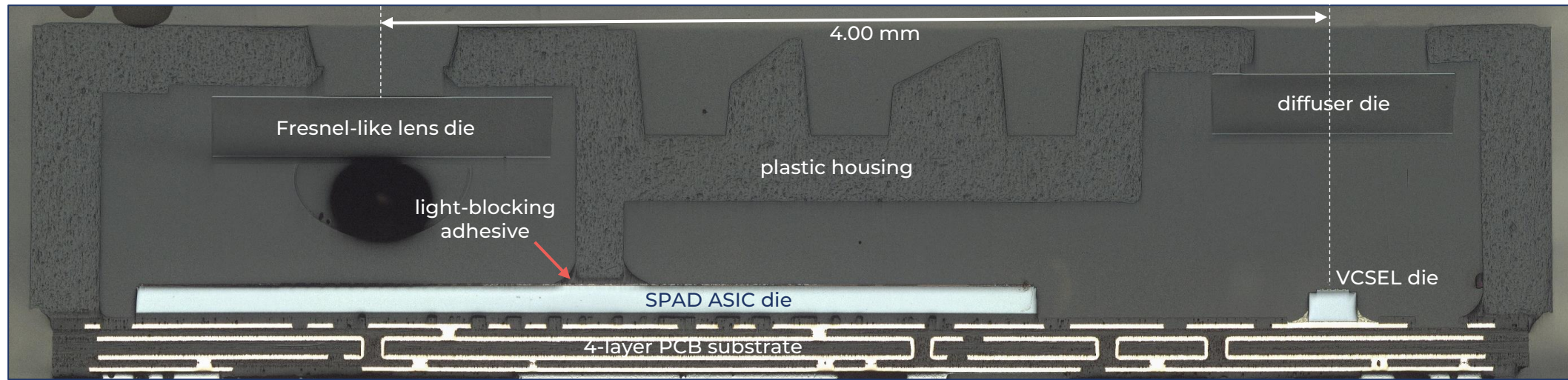


Tilted Top View of Opened Module
(image mirrored left-right)

©2024 Yole SystemPlus

Top View of Opened Module
showing the Cross-Sectional Plane

©2024 Yole SystemPlus



Module Cross Section - Optical View ©2024 Yole SystemPlus

ISSW24 | Laser Autofocus Reverse Costing | all images ©2024 Yole Group

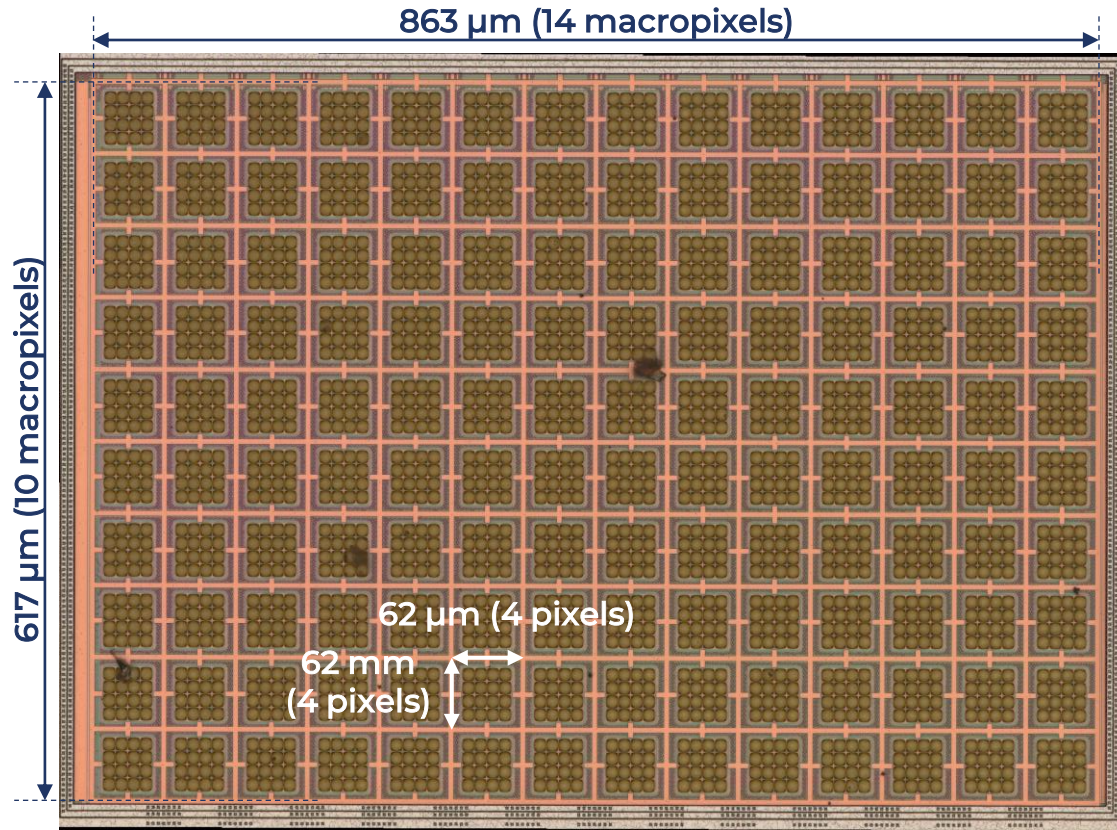
VL53L5

Optics & VCSEL

- Diffractive optics are embossed polymer on glass
- Microlenses on SPAD pixels



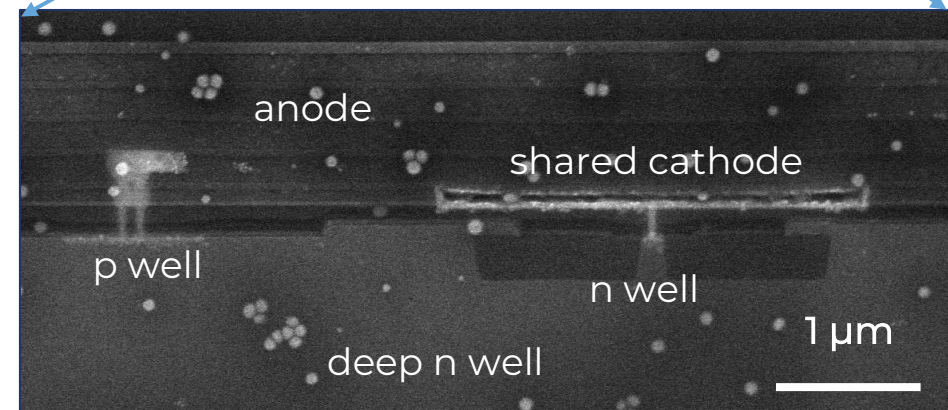
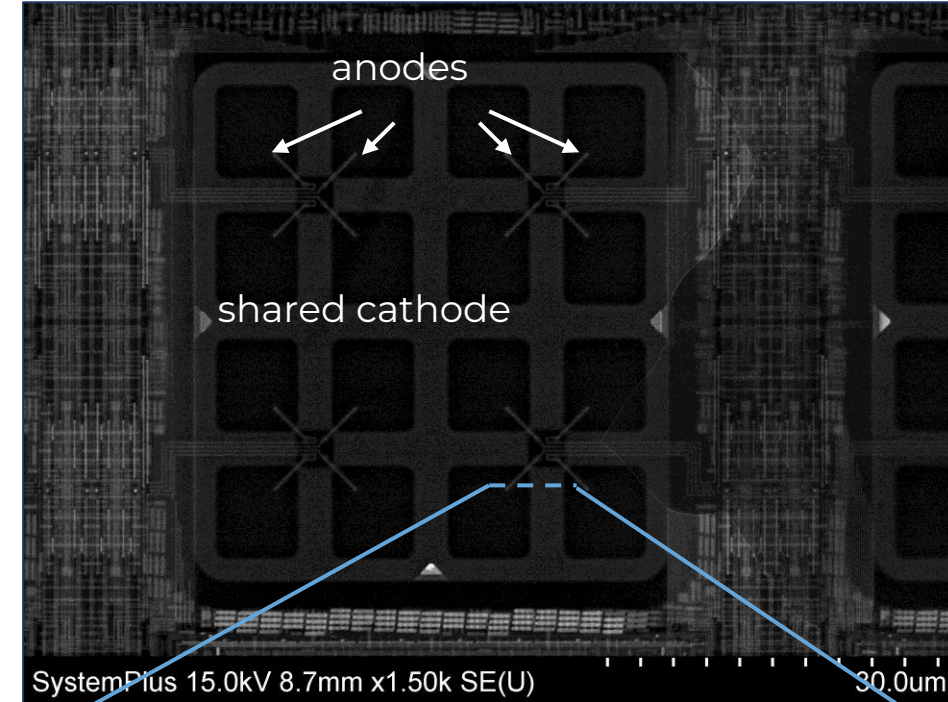
VL53L5 SPAD Array



SPAD ASIC Die Overview - Optical View ©2024 Yole SystemPlus

3. S. Pellegrini et al., "Industrialised SPAD in 40 nm technology," IEEE International Electron Devices Meeting (IEDM) 2017, doi: 10.1109/IEDM.2017.8268404.
4. S. Pellegrini. "Industrialized SPADs in deep-submicron CMOS technology." ISSW 2018.
5. Bruce Rae and Pascal Mellot, "A SPAD-based, Direct Time of Flight, 64 Zone, 15fps, Parallel Ranging Device Based on 40nm CMOS SPAD Technology." ISSW 2018.

SPAD Overview – SEM View ©2024 Yole SystemPlus



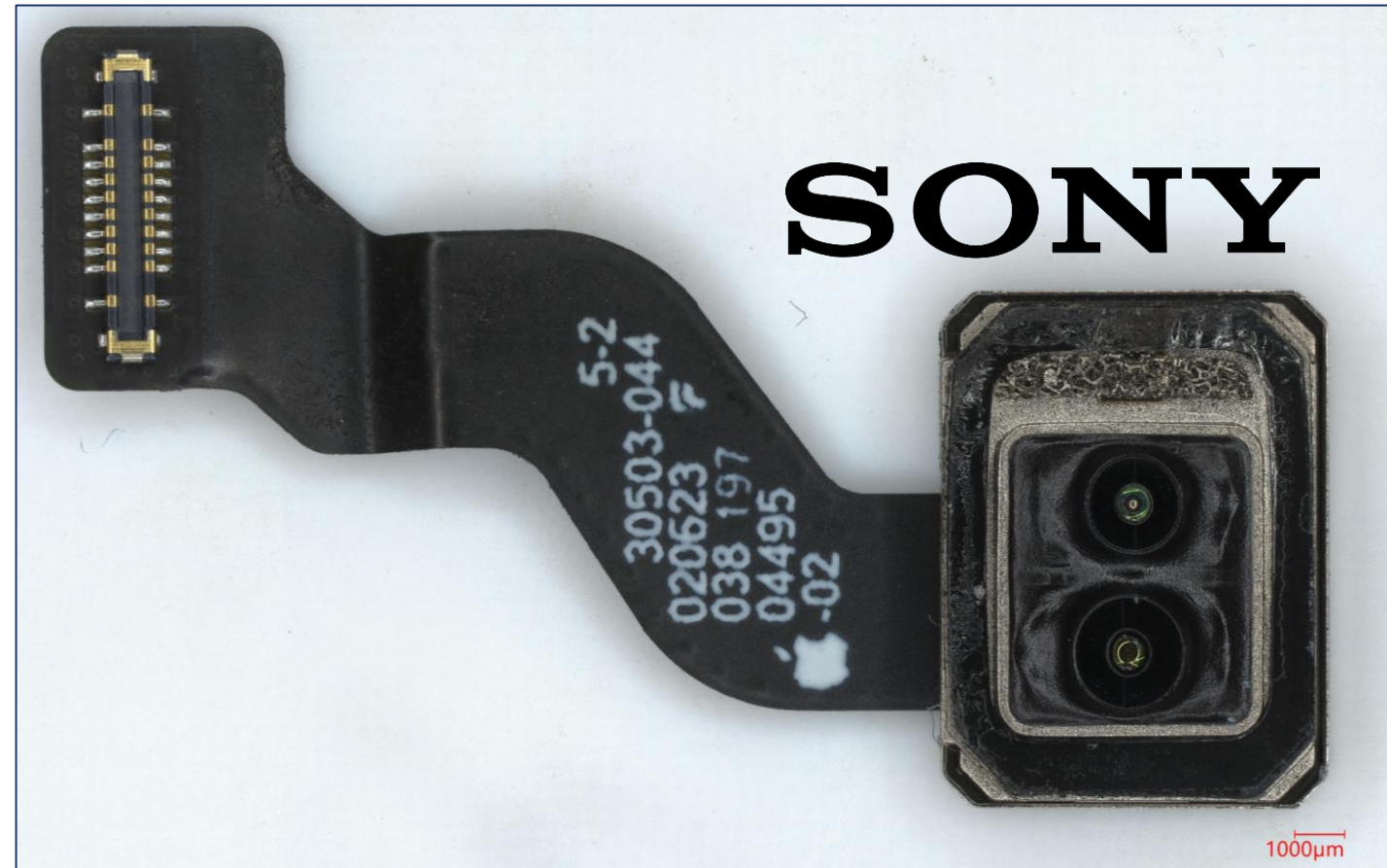
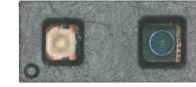
SPAD Section – SEM View ©2024 Yole SystemPlus

LASER AUTOFOCUS REVERSE COSTING

Presentation Outline

1. Smartphone 3D Imaging and Laser Autofocus
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 - VL53L5 by STMicroelectronics
 - TMF8821 by ams AG
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ams



TMF8821

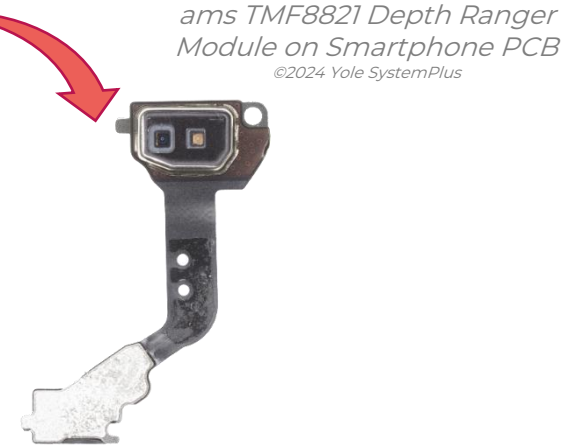
Magic3 Pro Teardown

We've also found the TMF8821 in the

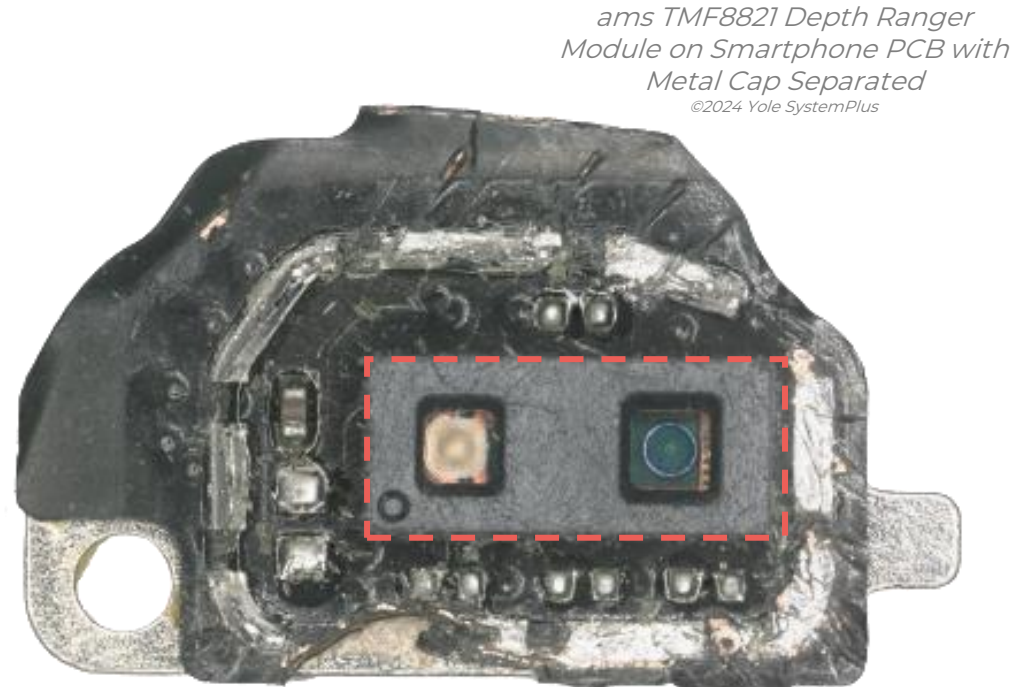
- Honor Magic 5 Pro
- Honor Magic V2



Honor Magic3 Pro - Back and Opened Views
©2024 Yole SystemPlus



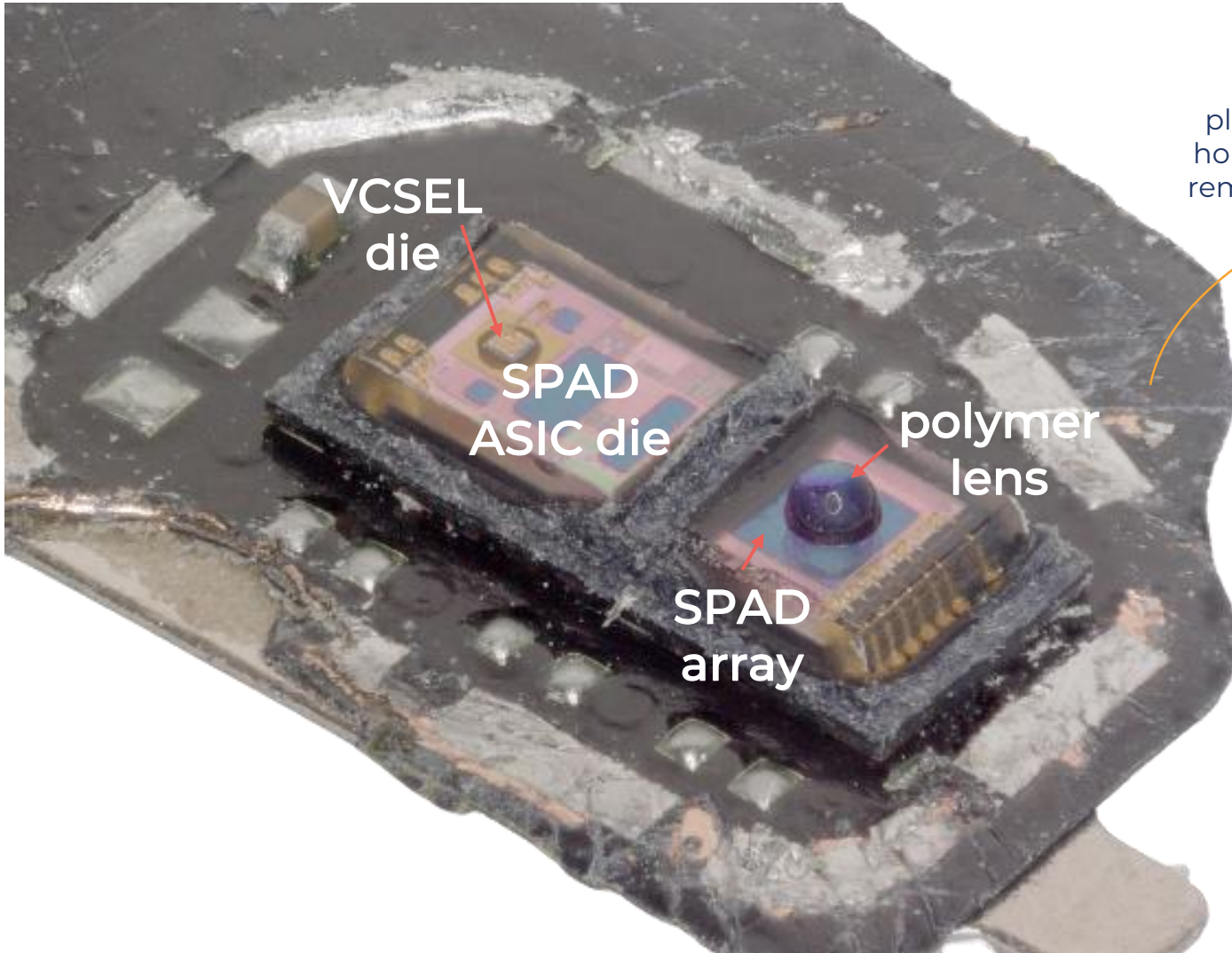
*ams TMF8821 Depth Ranger
Module on Smartphone PCB*
©2024 Yole SystemPlus



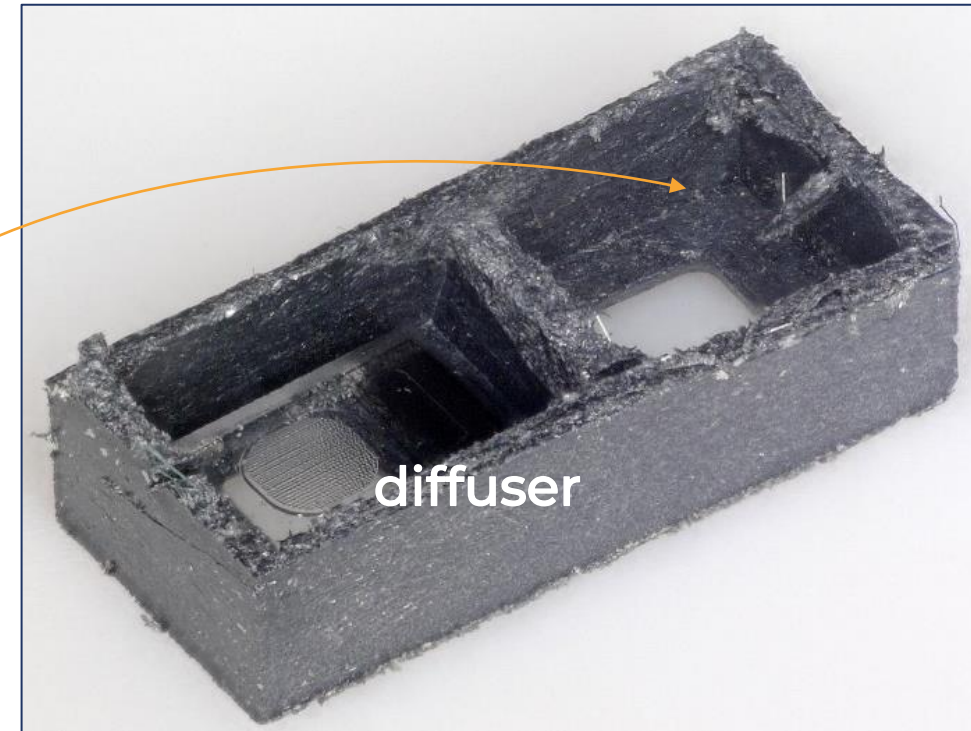
*ams TMF8821 Depth Ranger
Module on Smartphone PCB with
Metal Cap Separated*
©2024 Yole SystemPlus

TMF8821

Module Teardown



plastic housing removed



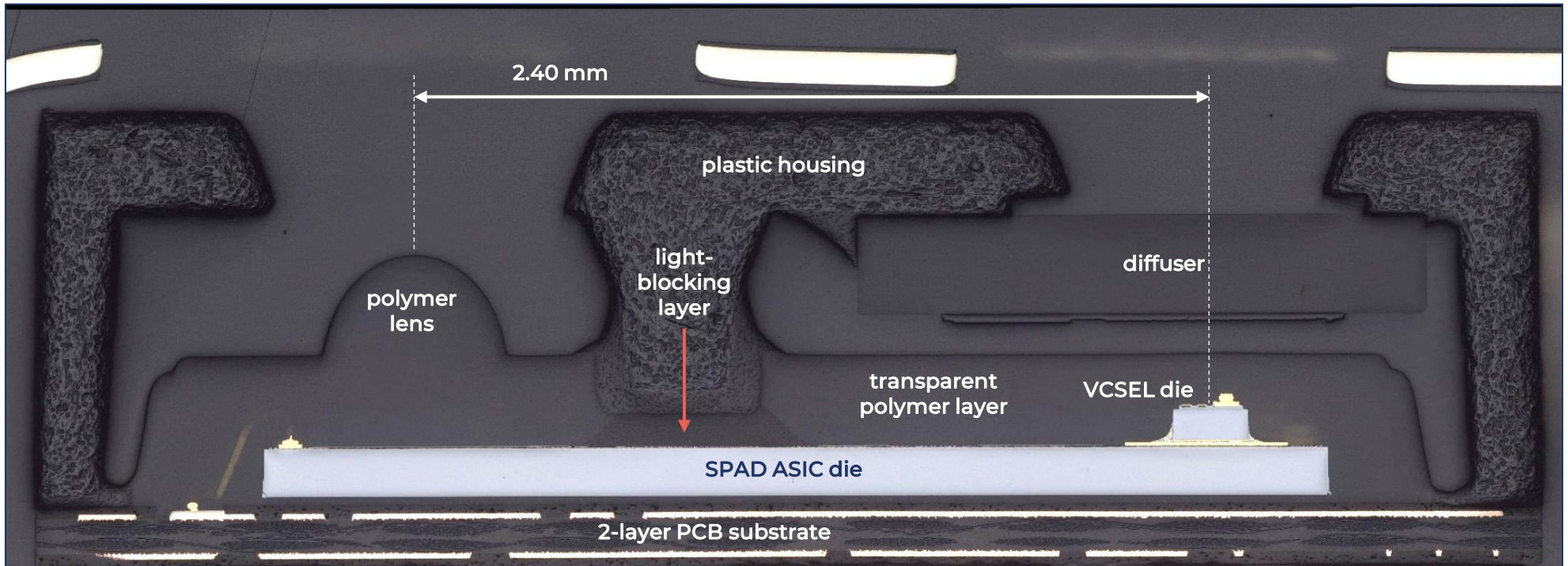
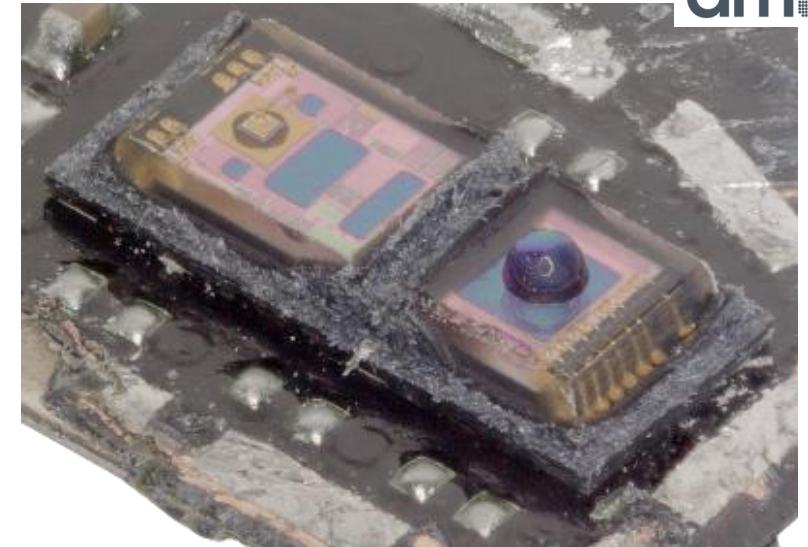
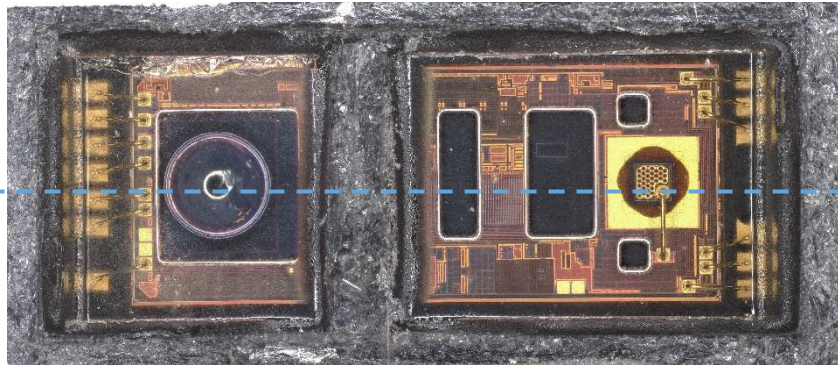
Plastic Housing w/ Diffuser - Tilted View
©2024 Yole SystemPlus

ams TMF8821 Module with Plastic Housing Removed - Tilted View
©2024 Yole SystemPlus

TMF8821

Cross Section

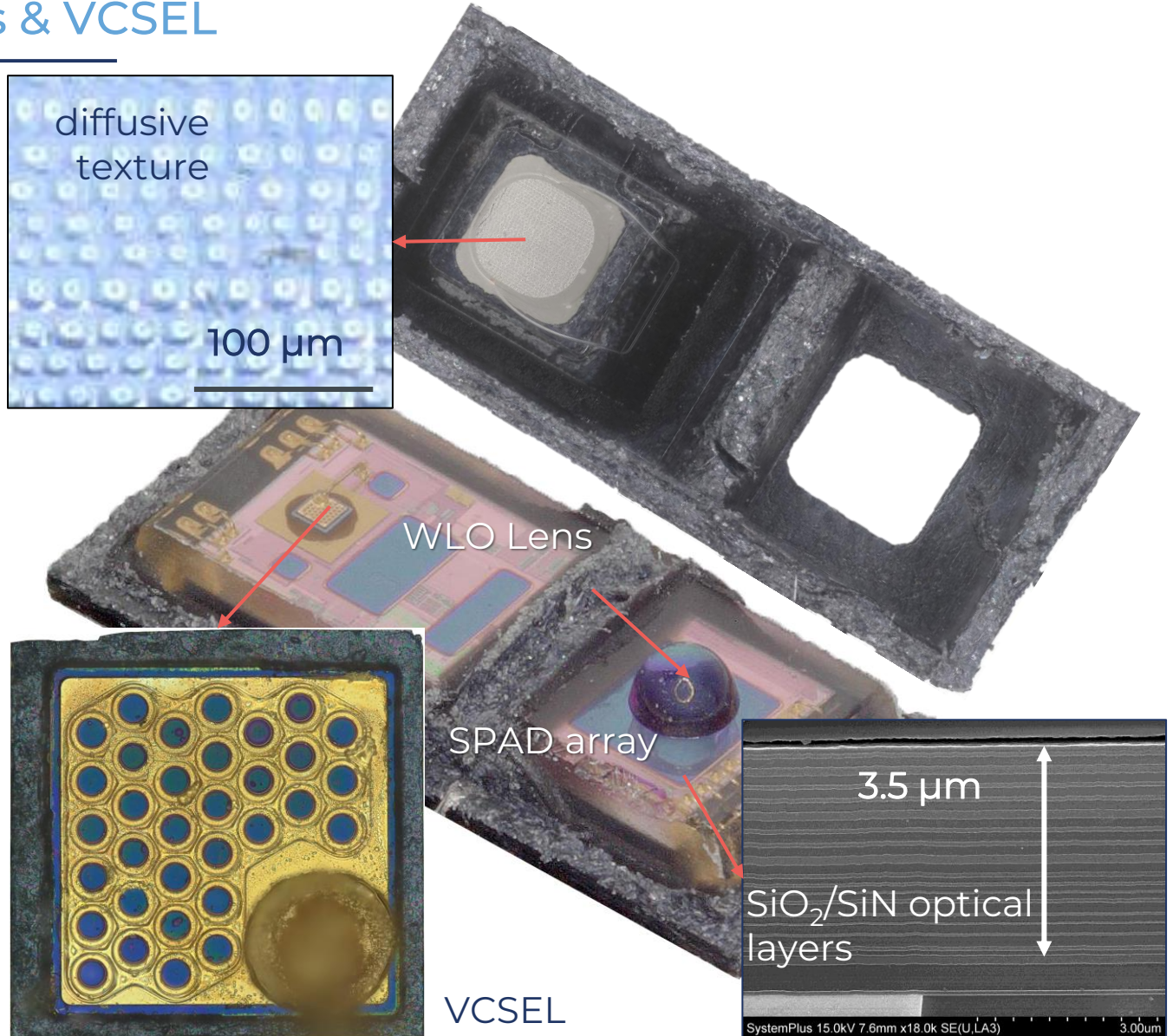
Top View of Opened Module showing the Cross-Sectional Plane
©2024 Yole SystemPlus



Module Cross Section - Optical View ©2024 Yole SystemPlus
ISSW24 | Laser Autofocus Reverse Costing | all images ©2024 Yole Group

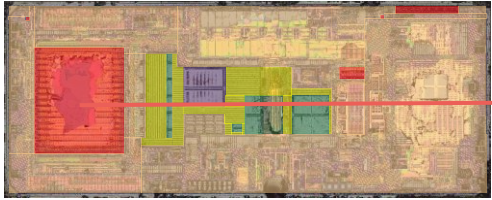
TMF8821

Optics & VCSEL

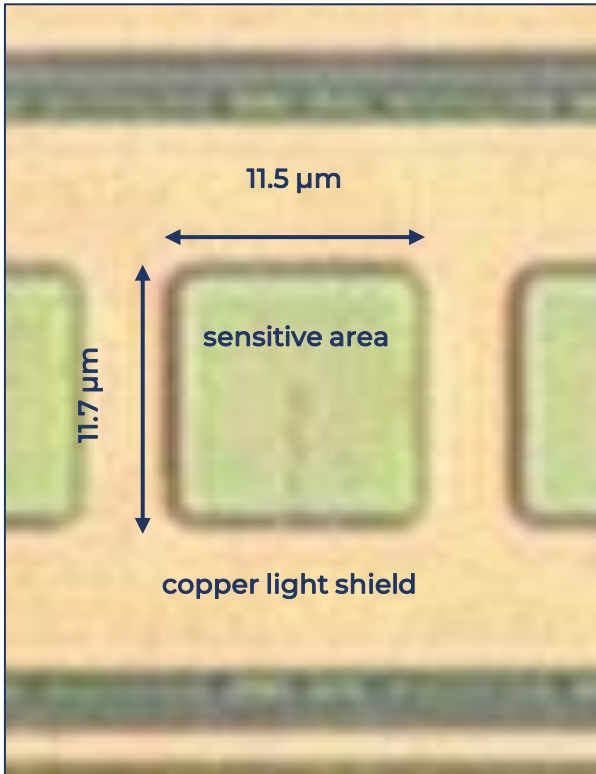


- Tx optic is embossed polymer on glass
- Rx optics are on-chip
- powerful VCSEL

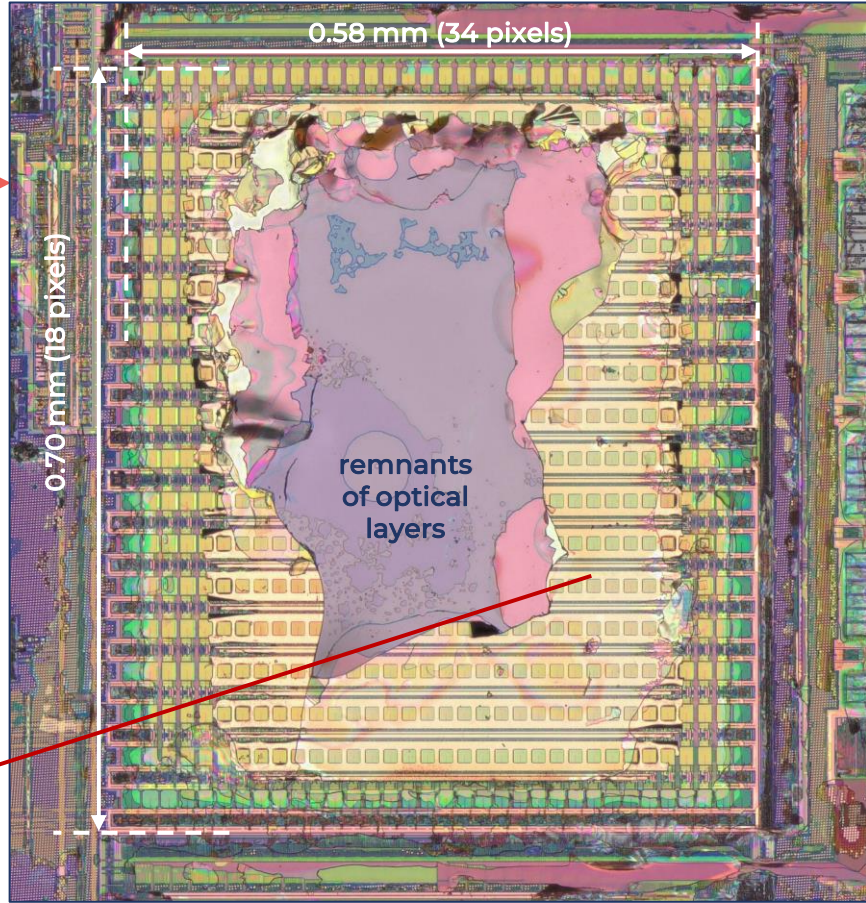
TMF8821 SPAD Array



SPAD ASIC Die with Main Blocks Identified ©2024 Yole SystemPlus



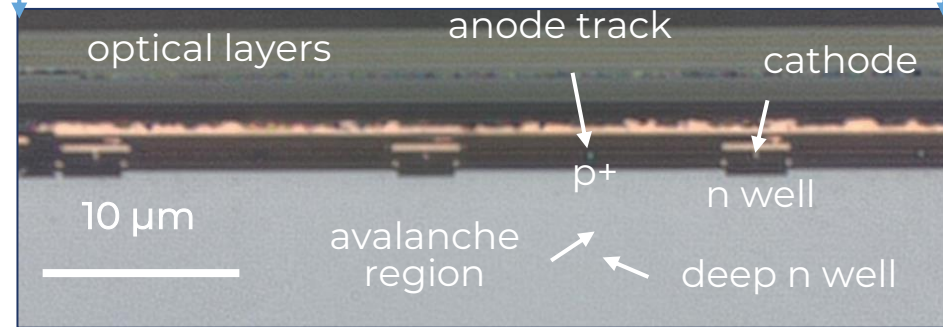
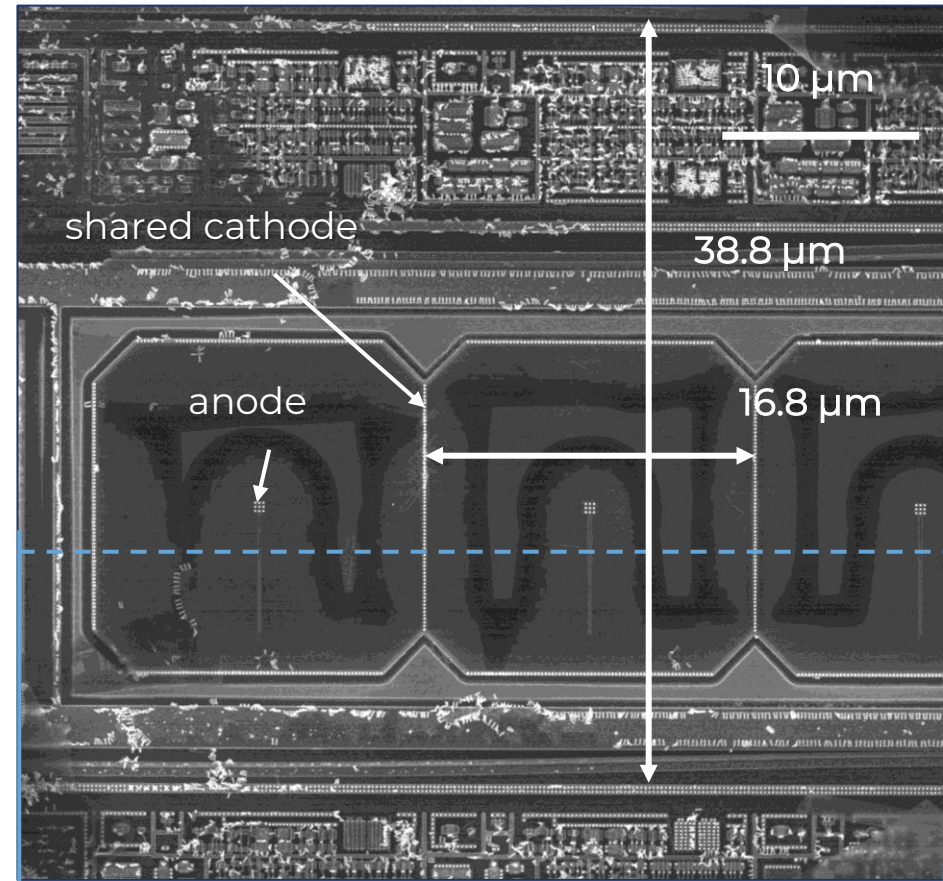
SPAD Pixel Active Area - Optical View ©2024 Yole SystemPlus



Main SPAD Array with Optical Filters and Metal Layers Partially Removed - Optical View ©2024 Yole SystemPlus

[5] R. Kappel. "Multizone, Multiobject D-TOF System in 55nm." ISSW2018.

SPAD Overview – SEM View ©2024 Yole SystemPlus



SPAD Section – Optical View ©2024 Yole SystemPlus

LASER AUTOFOCUS REVERSE COSTING

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« Reverse Costing Methodology »

1. Detailed Physical Analysis

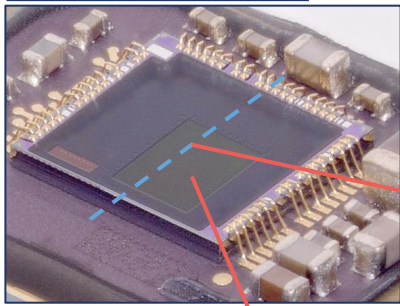
2. Reverse Engineer Manufacturing Process

3. Supply Chain & Financial Analysis

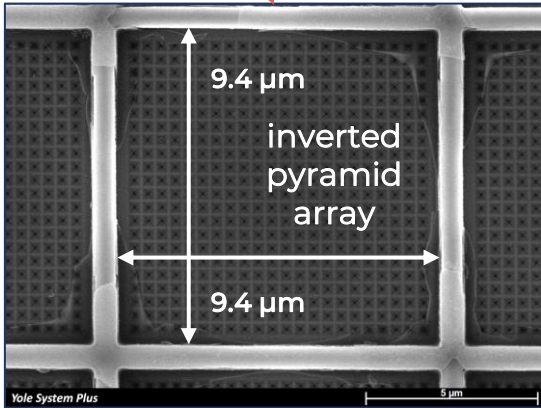
4. Simulate Manufacturing Process to Calculate Cost

REVERSE COSTING METHODOLOGY

Detailed Physical Analysis

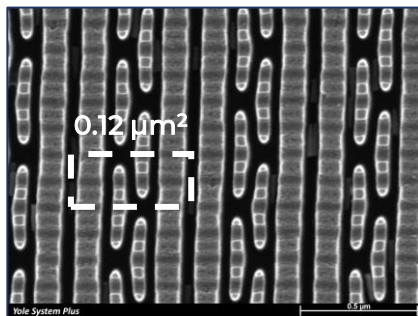


Opened LiDAR Module w/ cross-sectional plane indicated - Optical View ©2024 Yole SystemPlus



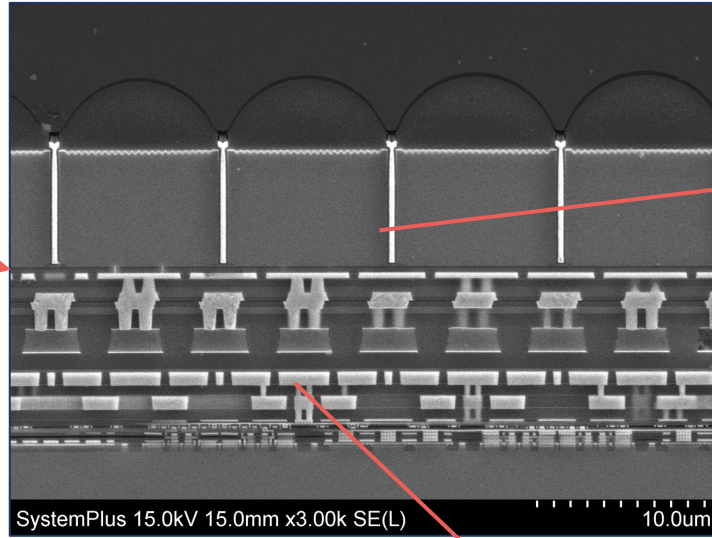
Yole System Plus

5 μm

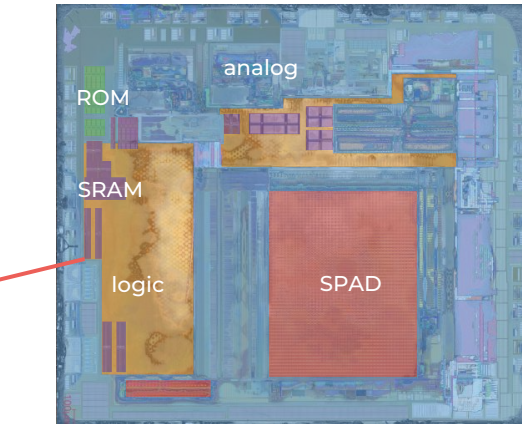


Yole System Plus

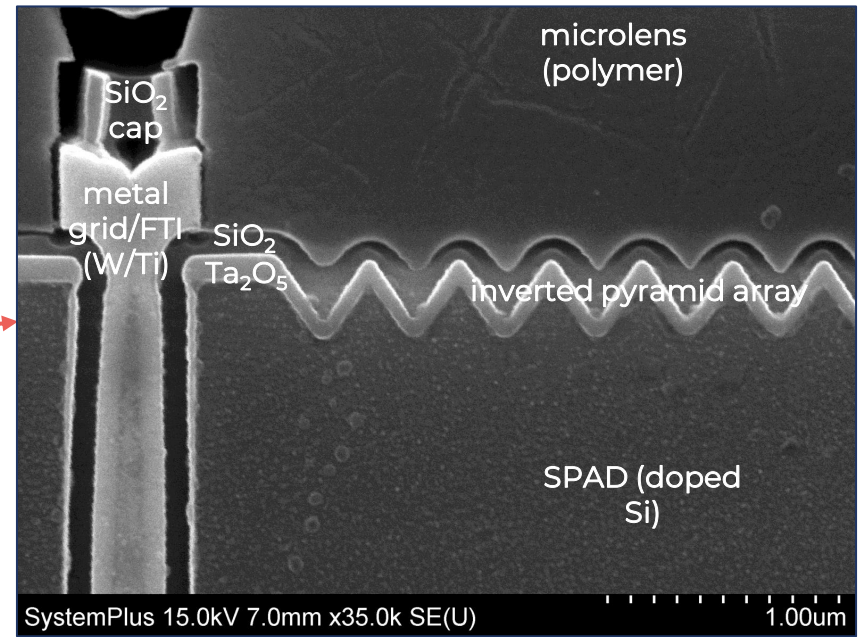
0.12 μm²



Cross Section through the SPAD Pixel Array - SEM View ©2024 Yole SystemPlus

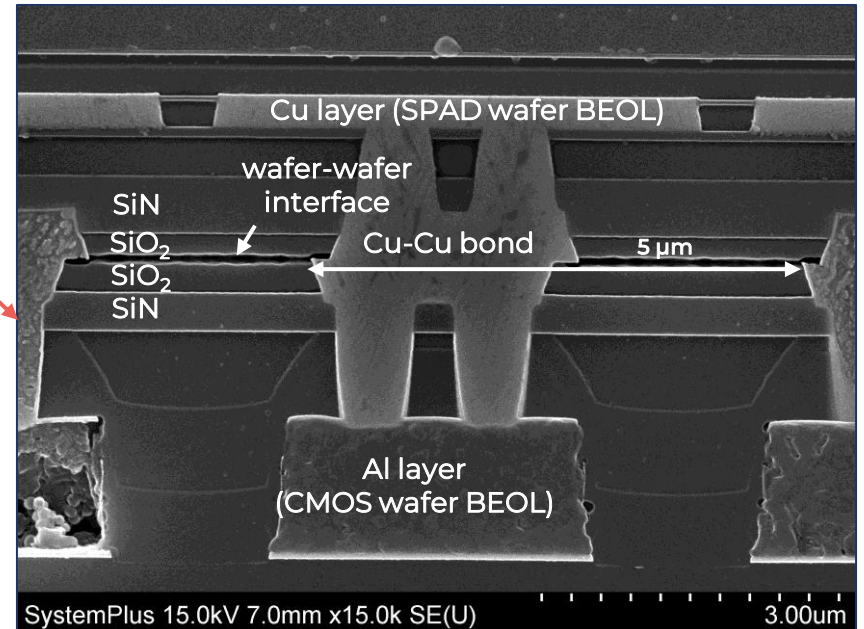


CMOS Die Overview w/ Main Blocks ©2024 Yole SystemPlus



SystemPlus 15.0kV 7.0mm x35.0k SE(U)

1.00μm



SystemPlus 15.0kV 7.0mm x15.0k SE(U)

3.00μm

REVERSE COSTING METHODOLOGY

Outline

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1. Detailed Physical Analysis

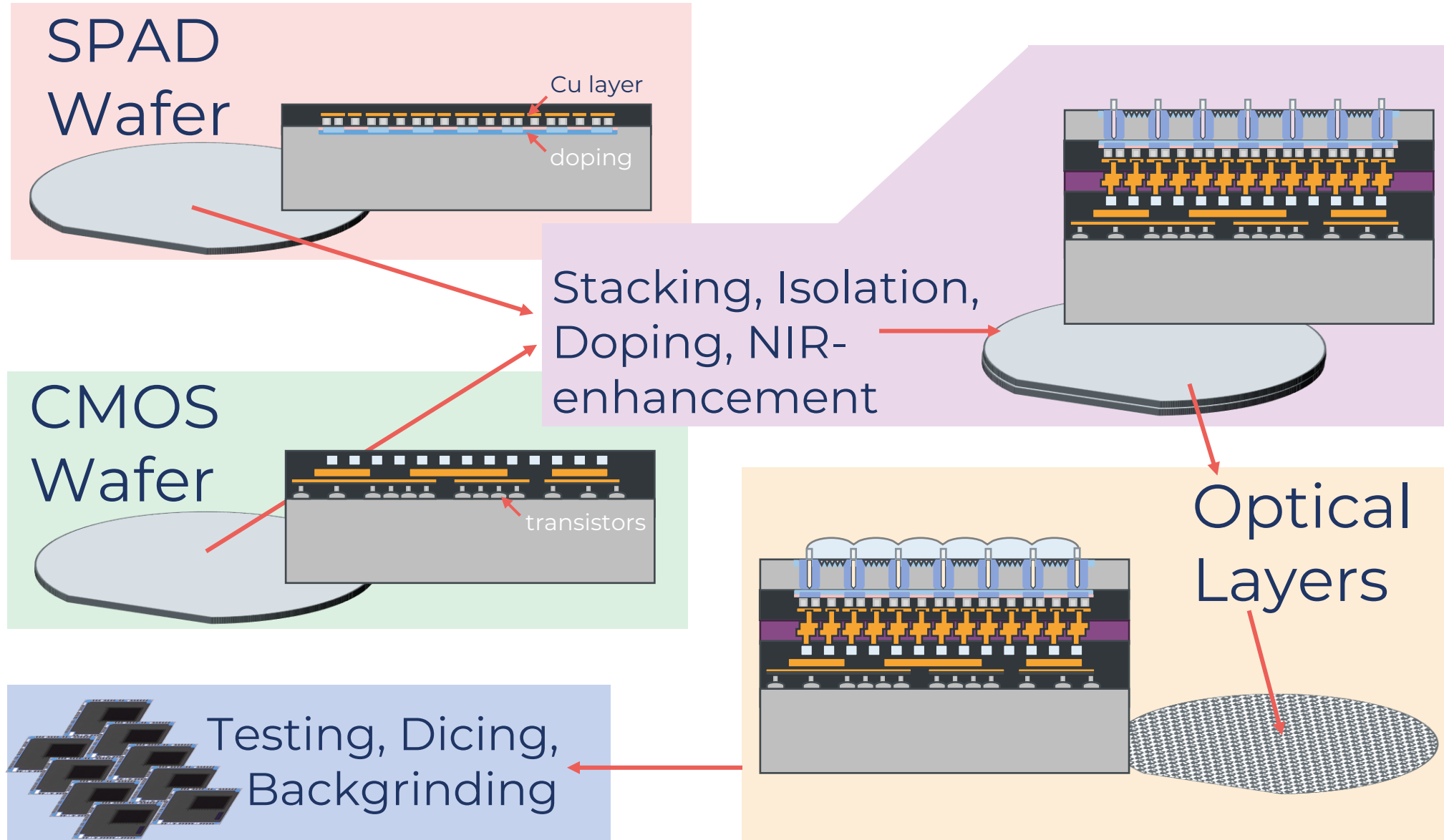
2. Reverse Engineer Manufacturing Process

3. Supply Chain & Financial Analysis

4. Simulate Manufacturing Process to Calculate Cost

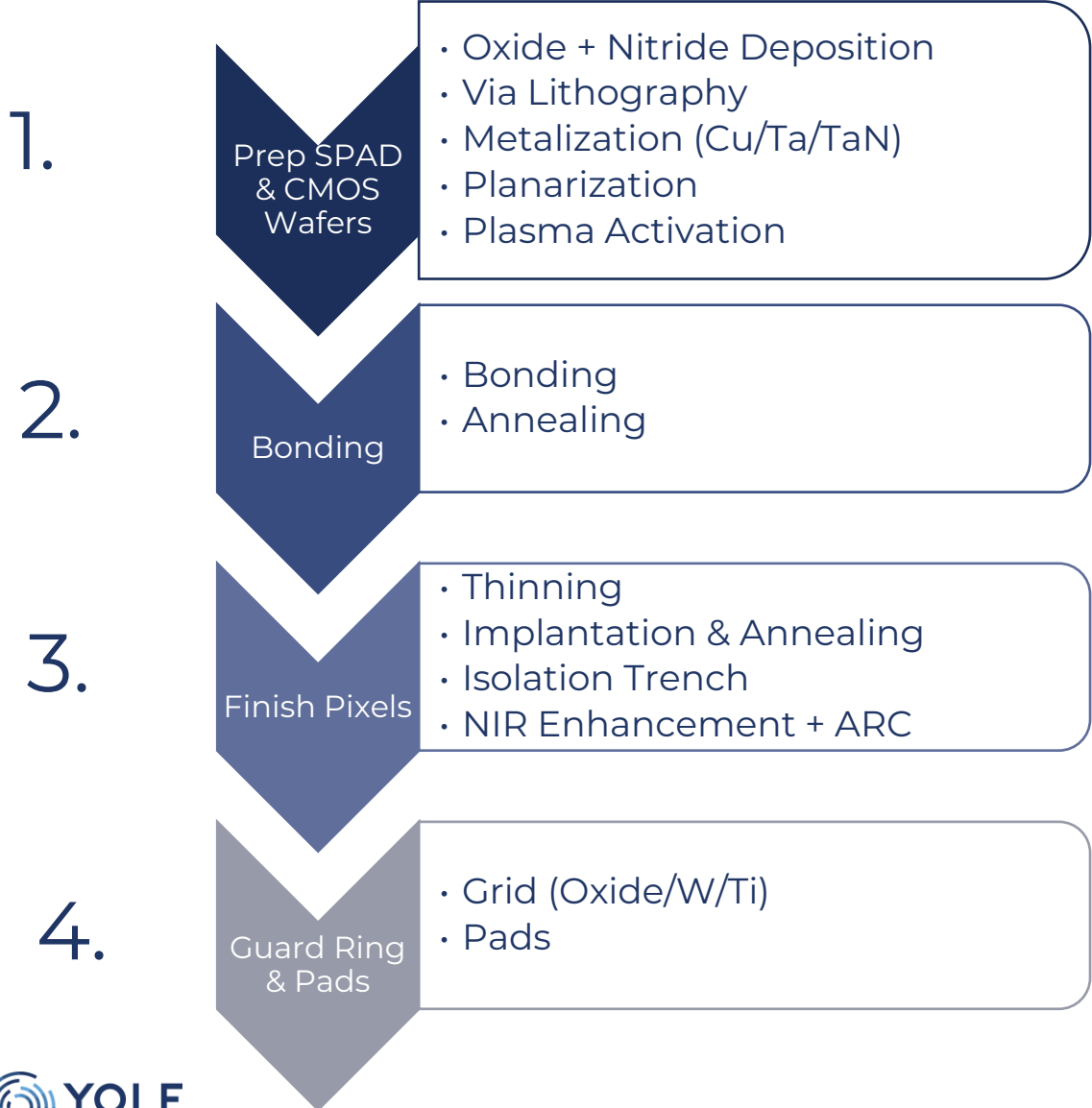
REVERSE COSTING METHODOLOGY

Reverse Engineer the Manufacturing Process



REVERSE COSTING METHODOLOGY

Reverse Engineer the Manufacturing Process



REVERSE COSTING METHODOLOGY

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1. Detailed Physical Analysis

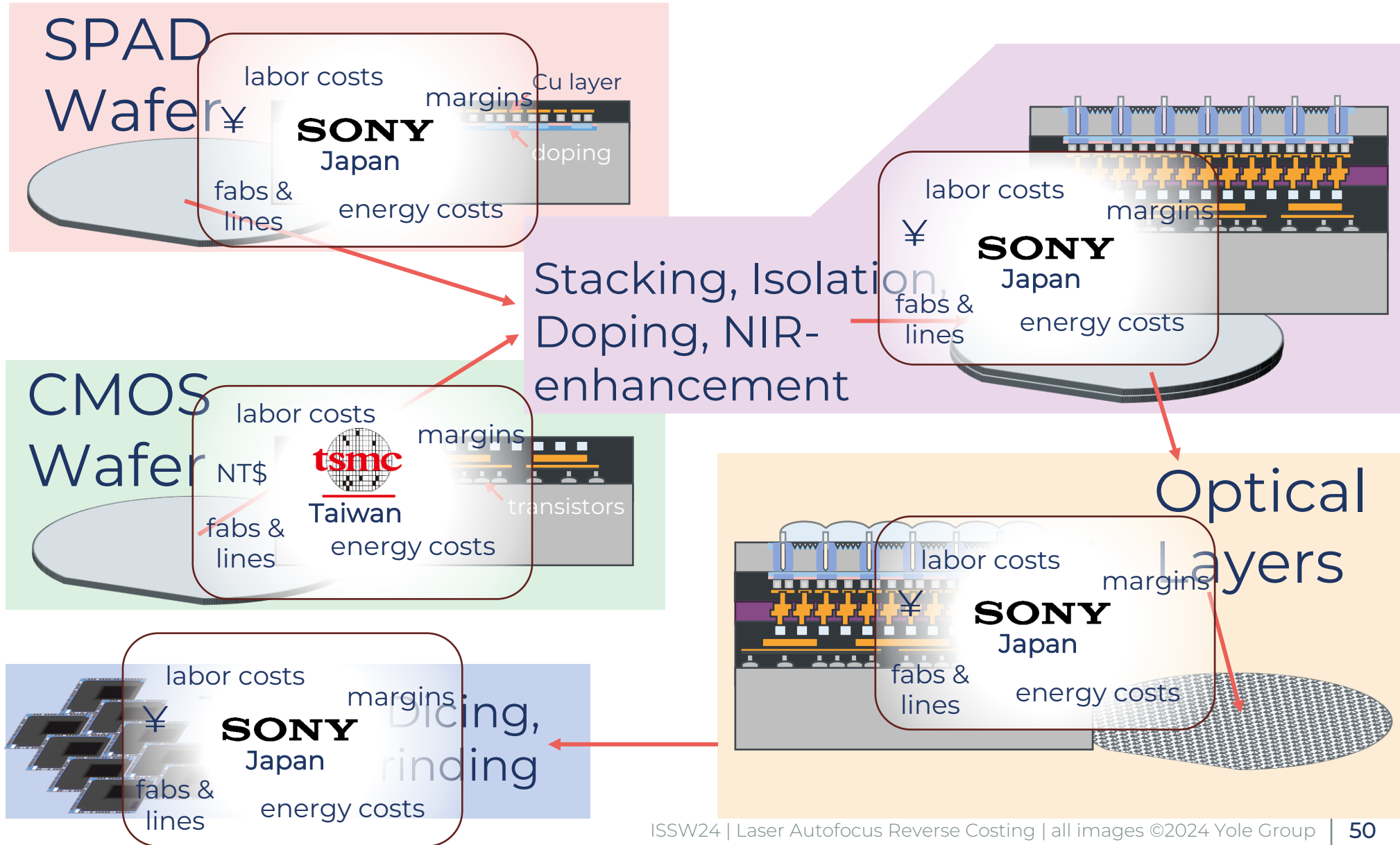
2. Reverse Engineer Manufacturing Process

3. Supply Chain & Financial Analysis

4. Simulate Manufacturing Process to Calculate Cost

REVERSE COSTING METHODOLOGY

Supply Chain and Financial Analysis



REVERSE COSTING METHODOLOGY

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1. Detailed Physical Analysis

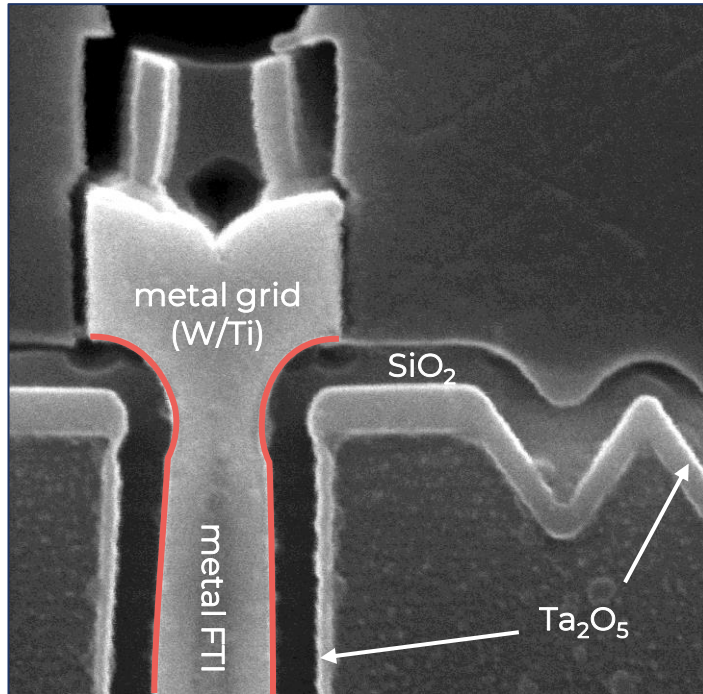
2. Reverse Engineer Manufacturing Process

3. Supply Chain & Financial Analysis

4. Simulate Manufacturing Process to Calculate Cost

REVERSE COSTING METHODOLOGY

Cost Modeling Overview



Cross Section through of Inverted Pyramid Array and Metal Grid - SEM View ©2024 Yole SystemPlus

4.

Guard Ring & Pads

- Grid (Oxide/W/Ti)
- Pads

Operation name	Step Cost (USD/Wafer)
Tungsten grid - Lithography 8	\$18.05
Tungsten grid - Oxide Etching (Dry)	\$0.95
Tungsten grid - Resist Strip	\$2.26
Tungsten grid - Ti Deposition	\$2.95
Tungsten grid - W Deposition	\$5.11
Tungsten grid - Lithography 9	\$18.05
Tungsten grid - W Etching	\$1.08
Tungsten grid - Resist Strip	\$2.26
Oxide Cap - Lithography 10	\$18.05
Oxide Cap - HDP Oxide	\$14.33
Oxide Cap - Resist Strip	\$2.26
Pad Trench - Lithography 11	\$18.05
Pad Trench - Silicon Etching (Dry)	\$2.04
Pad Trench - Resist Strip	\$2.26
Pad Trench - Lithography 12	\$18.05
Pad Trench - Silicon Etching (Dry)	\$1.32
Pad Trench - IMD Etching	\$3.66
Pad Trench - Resist Strip	\$2.26

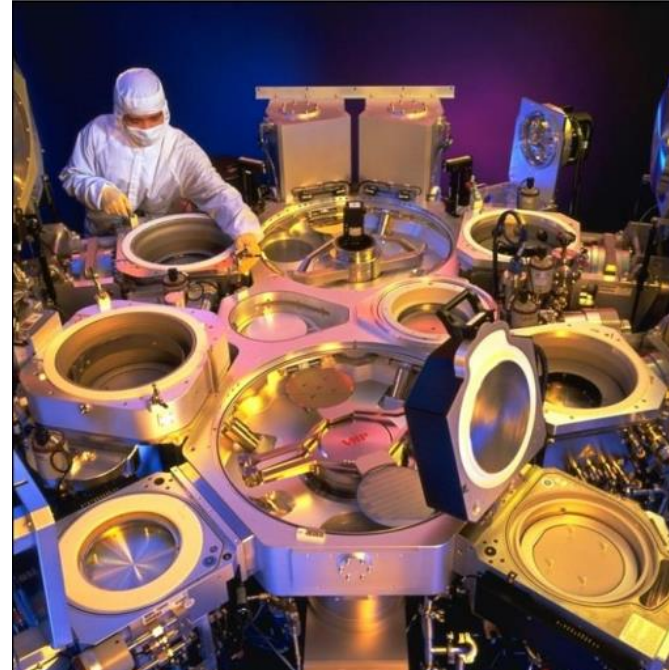
REVERSE COSTING METHODOLOGY

Cost Modeling Overview

Tungsten grid - Ti Deposition \$2.95

Operation (PVD of Ti)

- Wafer spends a certain amount of time in the PVD sputtering equipment.
- The equipment occupies costly cleanroom space.
- The machine is managed by an operator.
- The process consumes a certain amount of Ti target.



Cost Components to calculate:

- Equipment depreciation
- Equipment maintenance
- Cleanroom depreciation
- Cleanroom maintenance
- Labor cost
- Consumable cost
- Energy cost
- Overhead

+

\$2.95



REVERSE COSTING METHODOLOGY

Cost Modeling Overview

Cost Model Parameters (non-exhaustive)

- Equipment details
 - Purchase cost & date
 - Depreciation scheme
 - Maintenance costs
 - Footprint & power
 - Operator time
 - Batch size & loading time
 - Uptime
- Cleanroom details
 - ISO class & constr. date
 - Depreciation scheme
 - Maintenance costs
 - Total area, % load
 - Hours per year
- Country details
 - Salary
 - Energy cost
 - Shift and supervisor structure
 - Govt. incentives
- Consumables costs
- Process
 - Growth rate
 - Consumable consumption
 - Throughput

model

Calculated Cost Components

- Equipment depreciation
- Equipment maintenance
- Cleanroom depreciation
- Cleanroom maintenance
- Labor cost
- Consumable cost
- Energy cost
- Overhead

4.

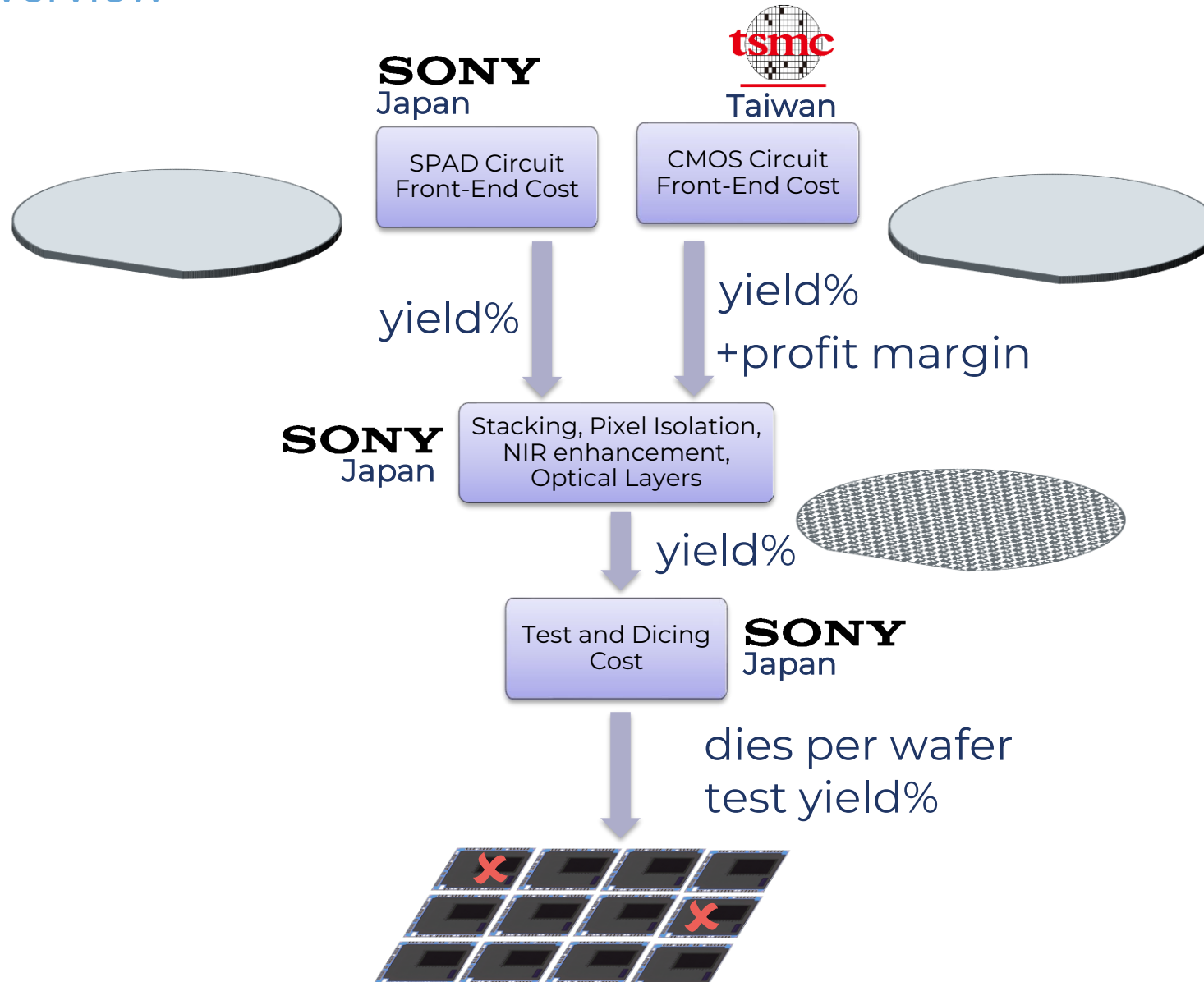
Guard Ring & Pads

- Grid (Oxide/W/Ti)
- Pads

Operation name	Step Cost (USD/Wafer)
Tungsten grid - Lithography 8	\$18.05
Tungsten grid - Oxide Etching (Dry)	\$0.95
Tungsten grid - Resist Strip	\$2.26
Tungsten grid - Ti Deposition	\$2.95
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Tungsten grid - W Etching	\$1.08
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Pad Trench - Resist Strip	\$2.26
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Pad Trench - Silicon Etching (Dry)	\$1.32
Pad Trench - IMD Etching	\$3.66
Pad Trench - Resist Strip	\$2.26

REVERSE COSTING METHODOLOGY

Die Cost Model Overview



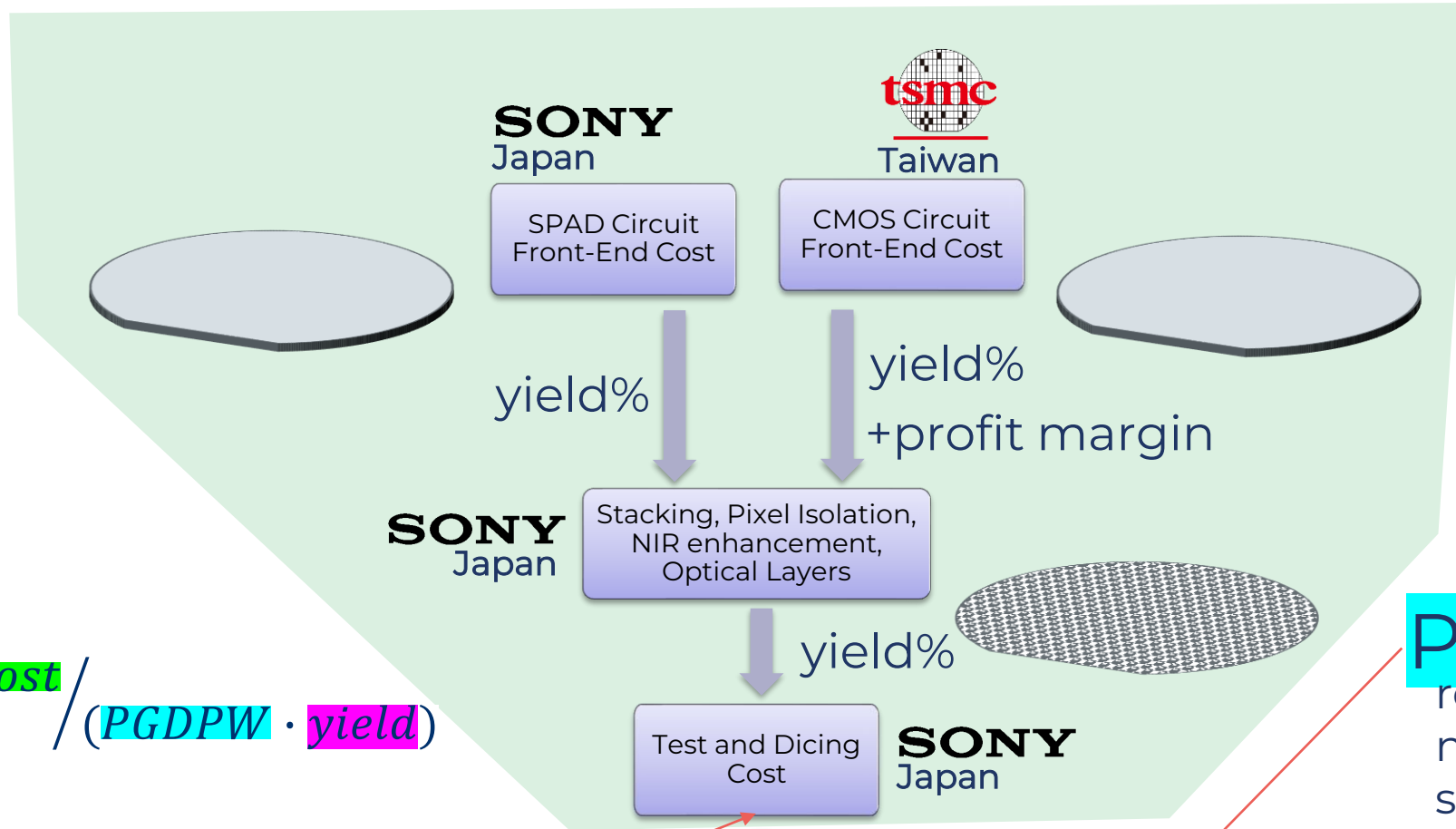
LASER AUTOFOCUS REVERSE COSTING

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APPROXIMATIVE COSTING MODEL

Die Cost Model



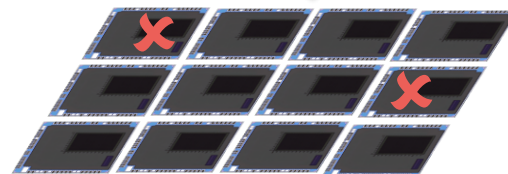
$$diecost = \frac{wafer\ cost}{(PGDPW \cdot yield)}$$

wafer cost
rounded to nearest most significant figure

PGDPW
rounded to nearest most significant figure

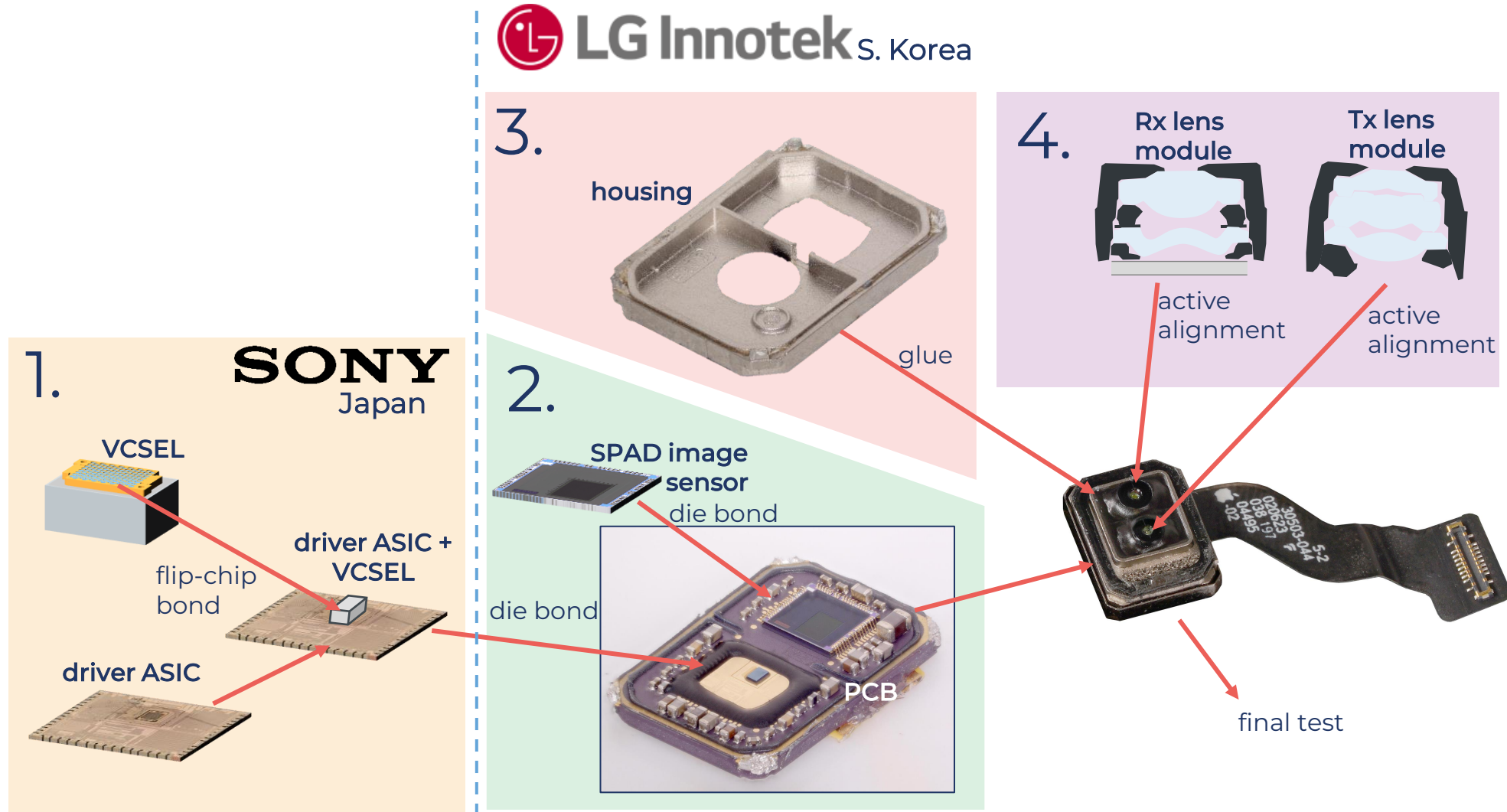
yield
rounded to nearest most significant figure

dies per wafer
test yield%



APPROXIMATIVE COSTING MODEL

Module Cost Model

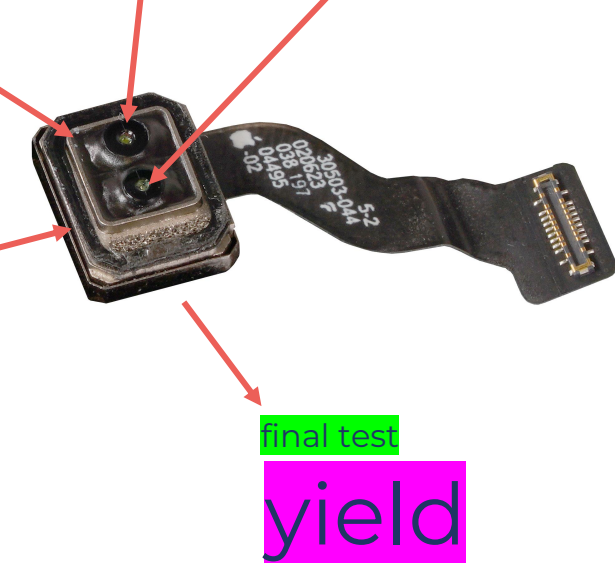
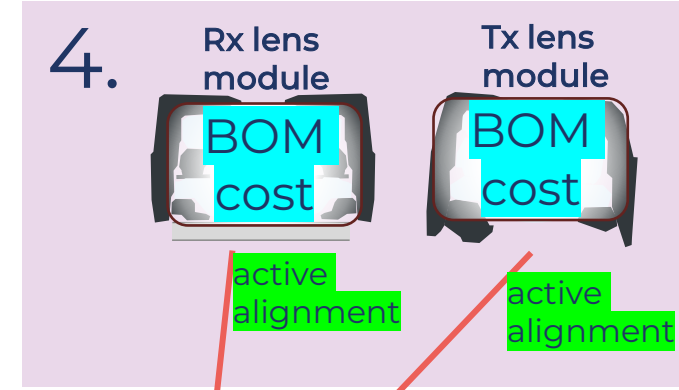
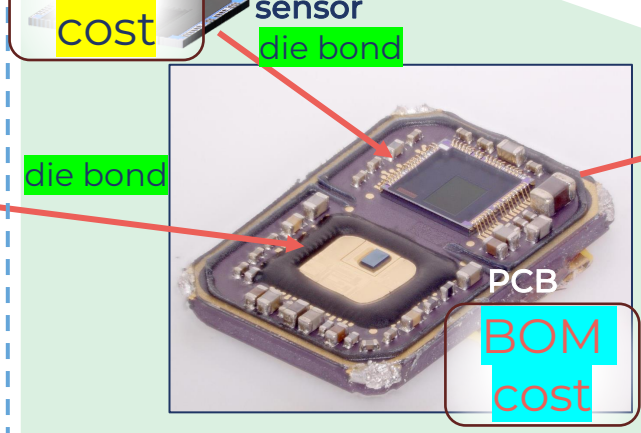
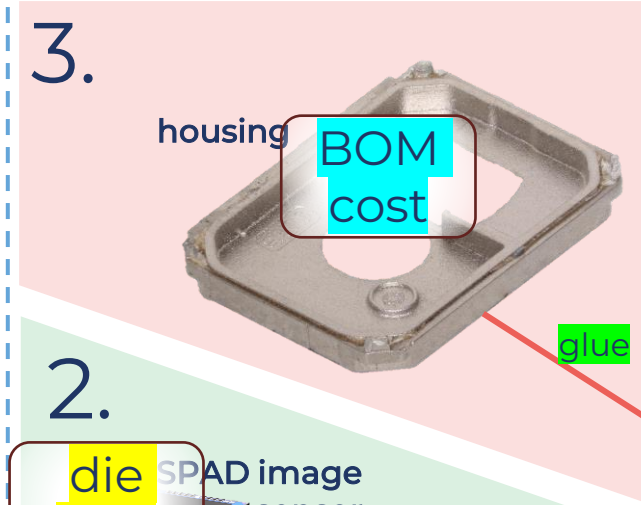
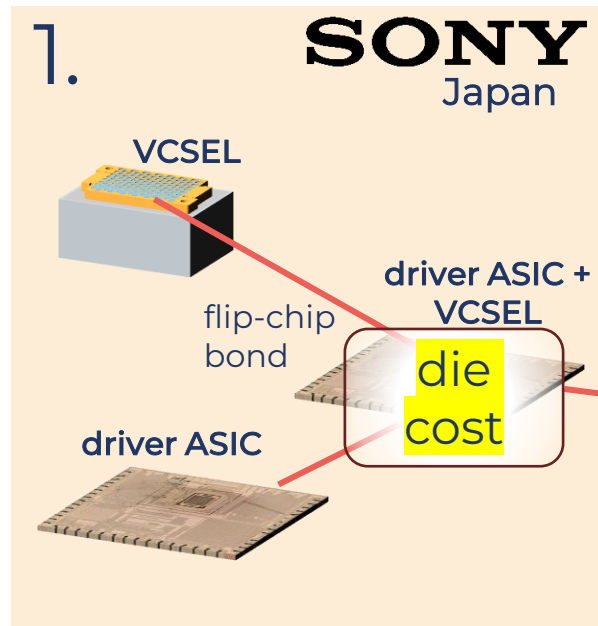


APPROXIMATIVE COSTING MODEL

Module Cost Model

$$\text{cost} = \frac{\sum \text{diecosts} + \sum \text{BOMcosts} + \sum \text{assemblycosts}}{\text{yield}}$$

All components rounded to nearest most significant figure



LASER AUTOFOCUS REVERSE COSTING

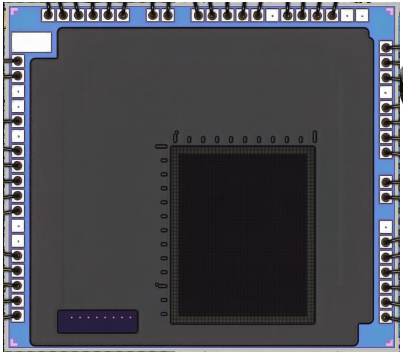
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RESULTS & DISCUSSION

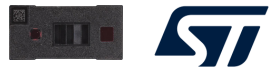
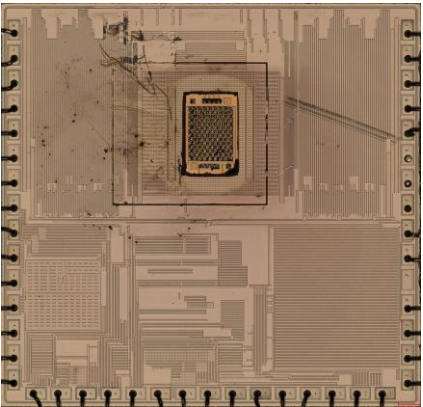
Die Costs

$$diecost = \frac{wafercost}{(PGDPW \cdot yield)}$$

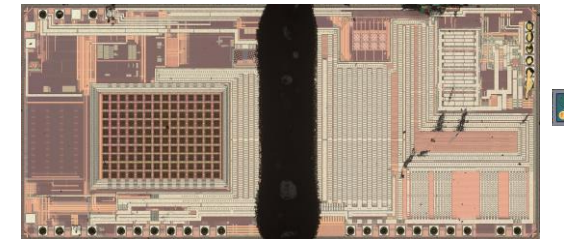


SONY

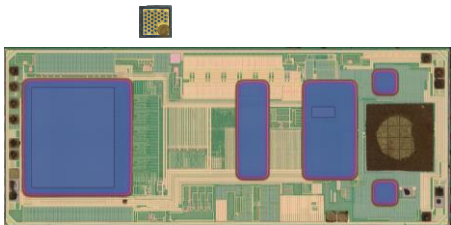
Die	wafercost	PGDPW	yield	diecost
SPAD CIS	\$5,000	9,000	80%	\$0.69
VCSEL+Driver	\$6,000	7,000	70%	\$1.22



Die	wafercost	PGDPW	yield	diecost
SPAD ASIC	\$2,000	10,000	90%	\$0.22
VCSEL	\$2,000	200,000	90%	\$0.01



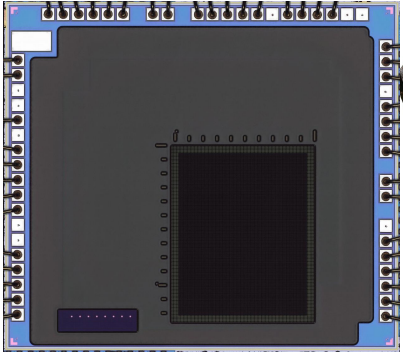
Die	wafercost	PGDPW	yield	diecost
SPAD ASIC	\$3,000	10,000	90%	\$0.33
VCSEL	\$3,000	200,000	90%	\$0.02



RESULTS & DISCUSSION

Die Costs

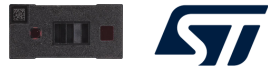
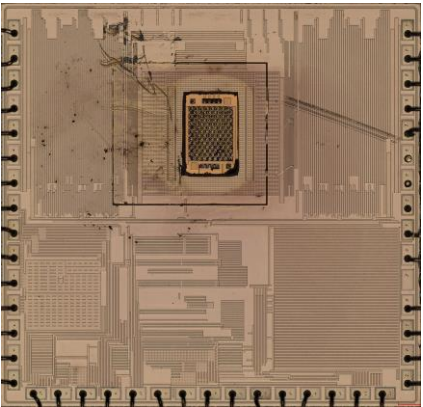
$$diecost = \frac{wafercost}{(PGDPW \cdot yield)}$$



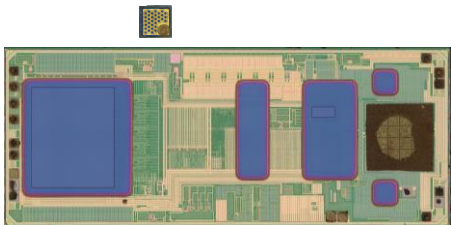
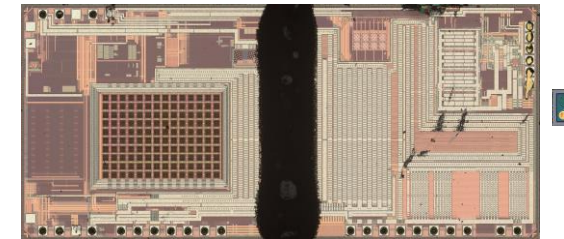
SONY

Die	wafercost	PGDPW	yield	diecost
SPAD CIS	\$5,000	9,000	80%	\$0.69
VCSEL+Driver	\$6,000	7,000	70%	\$1.22

3D-integrated SPAD is costly



Die	wafercost	PGDPW	yield	diecost
SPAD ASIC	\$2,000	10,000	90%	\$0.22
VCSEL	\$2,000	200,000	90%	\$0.01

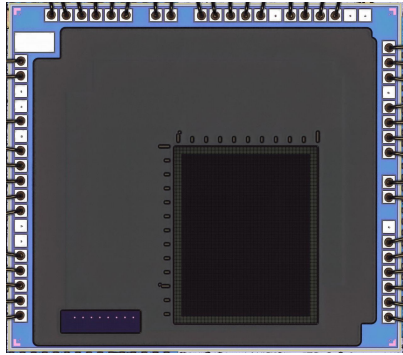


Die	wafercost	PGDPW	yield	diecost
SPAD ASIC	\$3,000	10,000	90%	\$0.33
VCSEL	\$3,000	200,000	90%	\$0.02

RESULTS & DISCUSSION

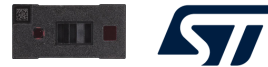
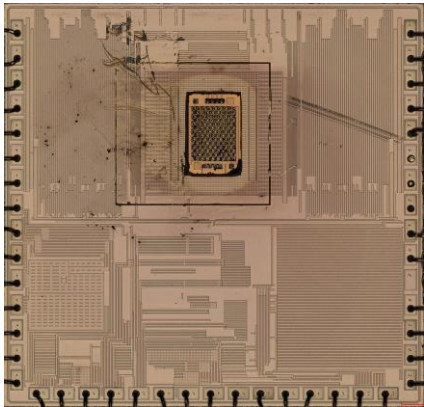
Module Costs

$$cost = \frac{\sum diecosts + \sum BOMcosts + assemblycosts}{yield}$$

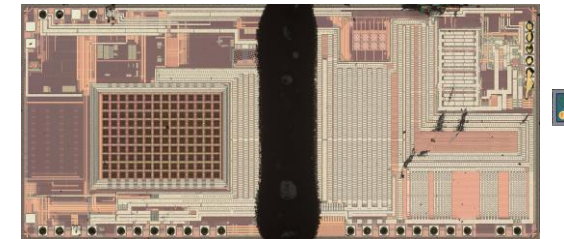


SONY

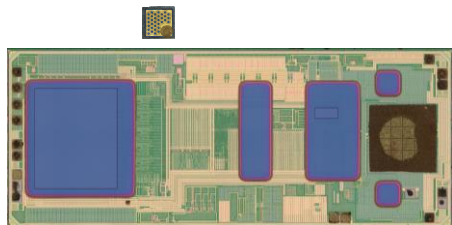
$\sum diecosts$	$\sum BOMcosts$	assembly	Yield	cost
\$1.91	\$3	\$1	90%	\$6.60



$\sum diecosts$	$\sum BOMcosts$	assembly	Yield	cost
\$0.23	\$0.1	\$0.2	90%	\$0.60



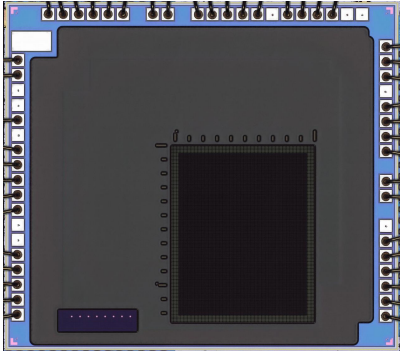
$\sum diecosts$	$\sum BOMcosts$	assembly	Yield	cost
\$0.35	\$0.02	\$0.1	90%	\$0.50



RESULTS & DISCUSSION

Module Costs

$$cost = \frac{\sum diecosts + \sum BOMcosts + assemblycosts}{yield}$$

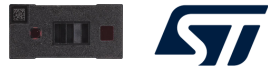
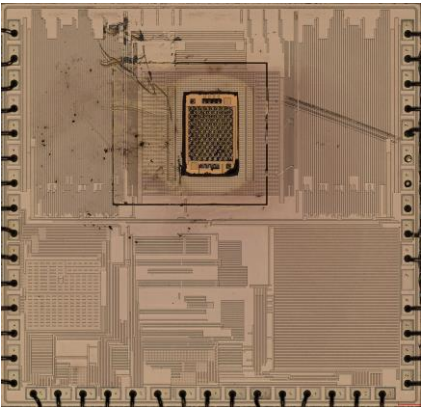


SONY

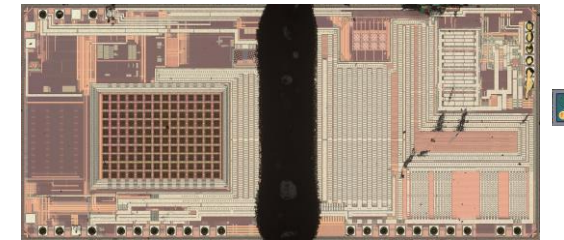
$\sum diecosts$	$\sum BOMcosts$	assembly	Yield	cost
\$1.91	\$3	\$1	90%	\$6.60

Optics and active alignment in the LiDAR are costly.

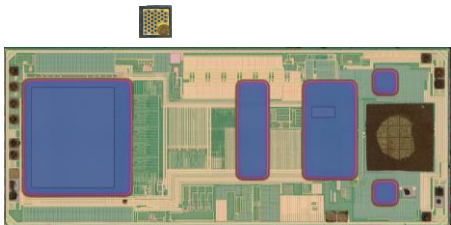
STMicro module also has active alignment of Rx optic.



$\sum diecosts$	$\sum BOMcosts$	assembly	Yield	cost
\$0.23	\$0.1	\$0.2	90%	\$0.60



$\sum diecosts$	$\sum BOMcosts$	assembly	Yield	cost
\$0.35	\$0.02	\$0.1	90%	\$0.50



RESULTS & DISCUSSION

Key Findings

SONY



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TABLE 1. KEY FINDINGS OF PHYSICAL & COSTING ANALYSIS

	iPhone LiDAR	VL53L5	TMF8821
estimated cost	\$6.60	\$0.60	\$0.50
SPAD ASIC Cost	-	\$0.22	\$0.33
VCSEL (alone)	-	\$0.01	\$0.02
Total Die Cost	\$1.91	\$0.23	\$0.35
Total BOM costs	\$3	\$0.1	\$0.02
Assembly costs	\$1	\$0.2	\$0.1
module vol. (LxWxH=V)	10.3x7.6x3.0 = 235 mm ³	6.4x3.0x1.5 = 29 mm ³	4.6x2.0x1.4 = 13 mm ³
VCSEL cavities	112 (indep.)	5	33
VCSEL total cavity area ^a	12,650 μm ²	1,150 μm ²	5,400 μm ²
transmission optic	refractive lens module	diffractive optic	multi-lens diffusor
emission shape	8x14 dot pattern	square	diffuse
baseline	3.0 mm	4.0 mm	2.4 mm
reception optics	refractive lenses, bandpass filter plate, on-chip μlenses, NIR enhanced	Fresnel-like flat lens, on-chip μlenses	WLO refractive lens, on-chip interferometric layers
SPAD process	90nm on 28nm CMOS with in-pixel DBI [1]	40nm CMOS [3-5]	55nm high-voltage CMOS & DMOS [6]
pixel pitch	10.1x10.1 μm ²	54x54 μm ^{2,b}	38.8x16.8 μm ²
detecting area per pixel (μlens area)	68 μm ²	1100 μm ² (μlens area) ^b	132 μm ²
SPAD array resolution	10,672 (116 x 92)	140 (14 x 10) ^b	612 (34 x 18)
total detecting area	0.73 mm ²	0.15 mm ²	0.08 mm ²

a. Cavity estimated by aperture in the anode

b. Per 4x4 macro-pixel

RESULTS & DISCUSSION

Key Findings – LiDAR vs multi-zone ranging

SONY



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TABLE 1. KEY FINDINGS OF PHYSICAL & COSTING ANALYSIS

	iPhone LiDAR	VL53L5	TMF8821
estimated cost	\$6.60	\$0.60	\$0.50
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VCSEL total cavity area ^a	12,650 μm ²	1,150 μm ²	5,400 μm ²
transmission optic	refractive lens module	diffractive optic	multi-lens diffusor
emission shape	8x14 dot pattern	square	diffuse
baseline	3.0 mm	4.0 mm	2.4 mm
reception optics	refractive lenses, bandpass filter plate, on-chip μlenses, NIR enhanced	Fresnel-like flat lens, on-chip μlenses	WLO refractive lens, on-chip interferometric layers
SPAD process	90nm on 28nm CMOS with in-pixel DBI [1]	40nm CMOS [3-5]	55nm high-voltage CMOS & DMOS [6]
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a. Cavity estimated by aperture in the anode

b. Per 4x4 macro-pixel

RESULTS & DISCUSSION

Key Findings – LiDAR vs multi-zone ranging

SONY



TABLE 1. KEY FINDINGS OF PHYSICAL & COSTING ANALYSIS

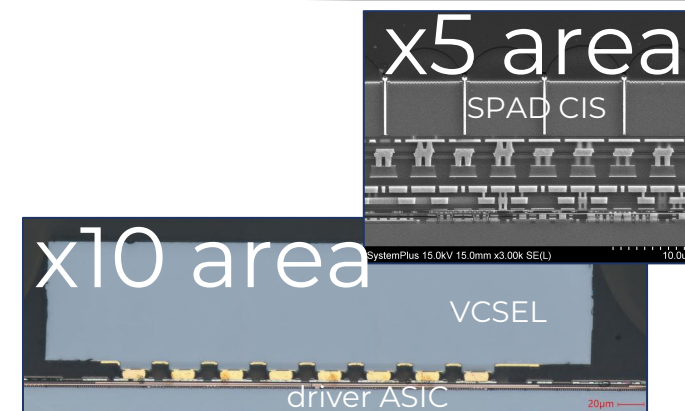
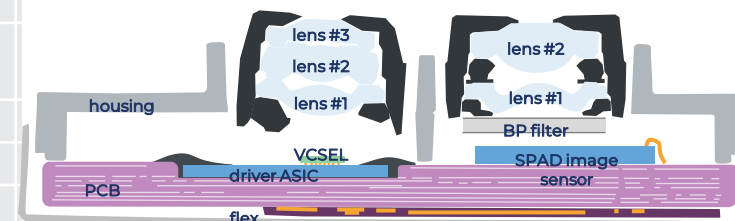
	iPhone LiDAR		VL53L5
estimated cost	\$6.60		\$0.60
SPAD ASIC Cost	-		\$0.22
VCSEL (alone)	-		\$0.01
Total Die Cost	\$1.91		\$0.23
Total BOM costs	\$3	lens modules	\$0.1
Assembly costs	\$1		\$0.2
module vol. (LxWxH=V)	10.3x7.6x3.0 = 235 mm ³		6.4x3.0x1.5 = 29 mm ³
VCSEL cavities	112 (indep.)		5
VCSEL total cavity area^a	12,650 μm²	x10	1,150 μm²
transmission optic	refractive lens module		diffractive optic
emission shape	8x14 dot pattern		square
baseline	3.0 mm		4.0 mm
reception optics	refractive lenses, bandpass filter plate, on-chip μlenses, NIR enhanced		Fresnel-like flat lens, on-chip μlenses
SPAD process	90nm on 28nm CMOS with in-pixel DBI [1]		40nm CMOS [3-5]
pixel pitch	10.1x10.1 μm ²		54x54 μm ^{2,b}
detecting area per pixel	68 μm ² (μlens area)		1100 μm ² (μlens area) ^b
SPAD array resolution	10,672 (116 x 92)		140 (14 x 10) ^b
total detecting area	0.73 mm²	x5	0.15 mm²

a. Cavity estimated by aperture in the anode

b. Per 4x4 macro-pixel

LiDAR 10x more costly

- Large SPAD CIS with costly 3D-integration
- Large back-emitting VCSEL flip-chip bonded directly to driver
- Complex optics for both Rx and Tx

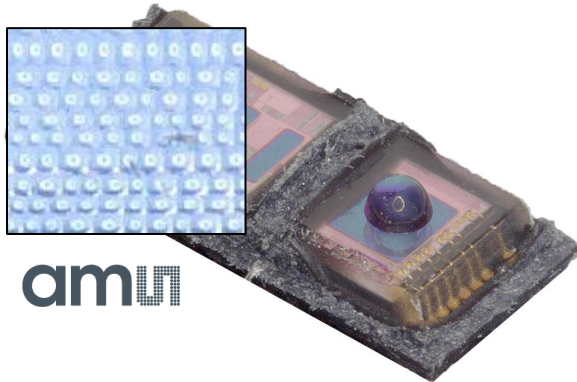


RESULTS & DISCUSSION

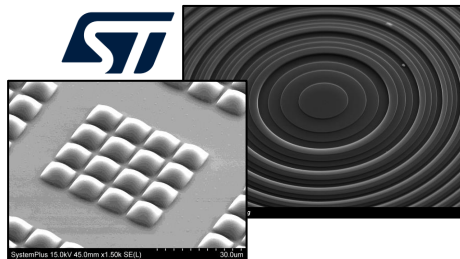
VL53L5 vs TMF8821 – WLO vs optical dies

estimated cost
SPAD ASIC Cost
VCSEL (alone)
Total Die Cost
Total BOM costs
Assembly costs
module vol. (LxWxH=V)
VCSEL cavities
VCSEL total cavity area ^a
transmission optic
emission shape baseline
reception optics
SPAD process
pixel pitch
detecting area per pixel
SPAD array resolution
total detecting area

- WLO Rx inexpensive compared to sophisticated diffractive element
 - Downside: no μlens
- No active alignment in ams AG module



ams



COMPARISONS OF PHYSICAL & COSTING ANALYSIS	
VL53L5	TMF8821
\$0.60	\$0.50
\$0.22	\$0.33
\$0.01	\$0.02
\$0.23	\$0.35
diffractive optical dies \$0.1	HEPTAGON™ WLO inexpensive \$0.02
\$0.2	\$0.1
6.4x3.0x1.5 = 29 mm ³	4.6x2.0x1.4 = 13 mm ³
5	33
1,150 μm ²	5,400 μm ²
diffractive optic	multi-lens diffusor
square	diffuse
4.0 mm	2.4 mm
Fresnel-like flat lens, on-chip μlenses	WLO refractive lens, on-chip interferometric layers
40nm CMOS [3-5]	55nm high-voltage CMOS & DMOS [6]
54x54 μm ^{2,b}	38.8x16.8 μm ²
1100 μm ² (μlens area) ^b	132 μm ²
140 (14 x 10) ^b	612 (34 x 18)
μlenses 0.15 mm ²	no μlenses 0.08 mm ²

RESULTS & DISCUSSION

VL53L5 vs TMF8821 – TSMC

estimated cost	
SPAD ASIC Cost	
VCSEL (alone)	
Total Die Cost	
Total BOM costs	
Assembly costs	
module vol. (LxWxH=V)	
VCSEL cavities	
VCSEL total cavity area ^a	
transmission optic	
emission shape baseline	
reception optics	
SPAD process	
pixel pitch	
detecting area per pixel	
SPAD array resolution	
total detecting area	

ams AG must compensate for smaller detecting area

- Foundry partner makes SPAD ASIC costly for ams AG

a. Cavity estimated by aperture in the anode

b. Per 4x4 macro-pixel



COMPARISONS OF PHYSICAL & COSTING ANALYSIS

	VL53L5	TMF8821
	\$0.60	\$0.50
	\$0.22	TSMC \$0.33
	\$0.01	\$0.02
	\$0.23	\$0.35
	\$0.1	\$0.02
	\$0.2	\$0.1
	6.4x3.0x1.5 = 29 mm ³	4.6x2.0x1.4 = 13 mm ³
	5	33
	1,150 μm ²	5,400 μm ²
	diffractive optic	multi-lens diffusor
	square	diffuse
	4.0 mm	2.4 mm
	Fresnel-like flat lens, on-chip μlenses	WLO refractive lens, on-chip interferometric layers
	40nm CMOS [3-5]	55nm high-voltage CMOS & DMOS [6]
	54x54 μm ^{2,b}	38.8x16.8 μm ²
	1100 μm ² (μlens area) ^b	132 μm ²
	140 (14 x 10) ^b	/2 612 (34 x 18)
	0.15 mm ²	small 0.08 mm ²

detecting area

RESULTS & DISCUSSION

VL53L5 vs TMF8821 – VCSEL solution

estimated cost
SPAD ASIC Cost
VCSEL (alone)
Total Die Cost
Total BOM costs
Assembly costs
module vol. (LxWxH=V)
VCSEL cavities
VCSEL total cavity area ^a
transmission optic
emission shape
baseline
reception optics
SPAD process
pixel pitch
detecting area per pixel
SPAD array resolution
total detecting area

ams AG must compensate for smaller detecting area

- Foundry partner makes SPAD ASIC costly for ams AG
- Powerful VCSEL
 - downside: power hungry

a. Cavity estimated by aperture in the anode

b. Per 4x4 macro-pixel



COMPARISONS OF PHYSICAL & COSTING ANALYSIS	
VL53L5	TMF8821
\$0.60	\$0.50
\$0.22	\$0.33
\$0.01	\$0.02
\$0.23	\$0.35
\$0.1	\$0.02
\$0.2	\$0.1
6.4x3.0x1.5 = 29 mm ³	4.6x2.0x1.4 = 13 mm ³
5	33
1,150 μm ²	5,400 μm ²
diffractive optic	multi-lens diffusor
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1100 μm ² (μlens area) ^b	132 μm ²
140 (14 x 10) ^b	612 (34 x 18)
0.15 mm ²	0.08 mm ²

x5

powerful VCSEL

/2

small detecting area

LASER AUTOFOCUS REVERSE COSTING

Conclusions

3D Imaging (LiDAR) is 10x the cost and 10x the module volume

- Large SPAD CIS with costly 3D-integration
- Large and innovative back-emitting VCSEL flip-chip bonded directly to driver
- Complex optics for both Rx and Tx

STMicroelectronics module has highly engineered optics, including microlenses

ams AG module designed to optimize costs

- Heptagon WLO very inexpensive
 - Downside: doesn't allow μ lenses
 - Downside: Tx pattern less engineered
- Challenge: Small sensitive area (no μ lens, TSMC partner)
 - Solution: compensate with large VCSEL (power hungry)

Fin.