A PVT-Insensitive Body-Biased Time-to-Digital Converter in 28nm FD-SOI CMOS Technology

Yining Wang [1], Hanning Mai [1,2] , Yining Wang[1], Robert K.Henderson[1]

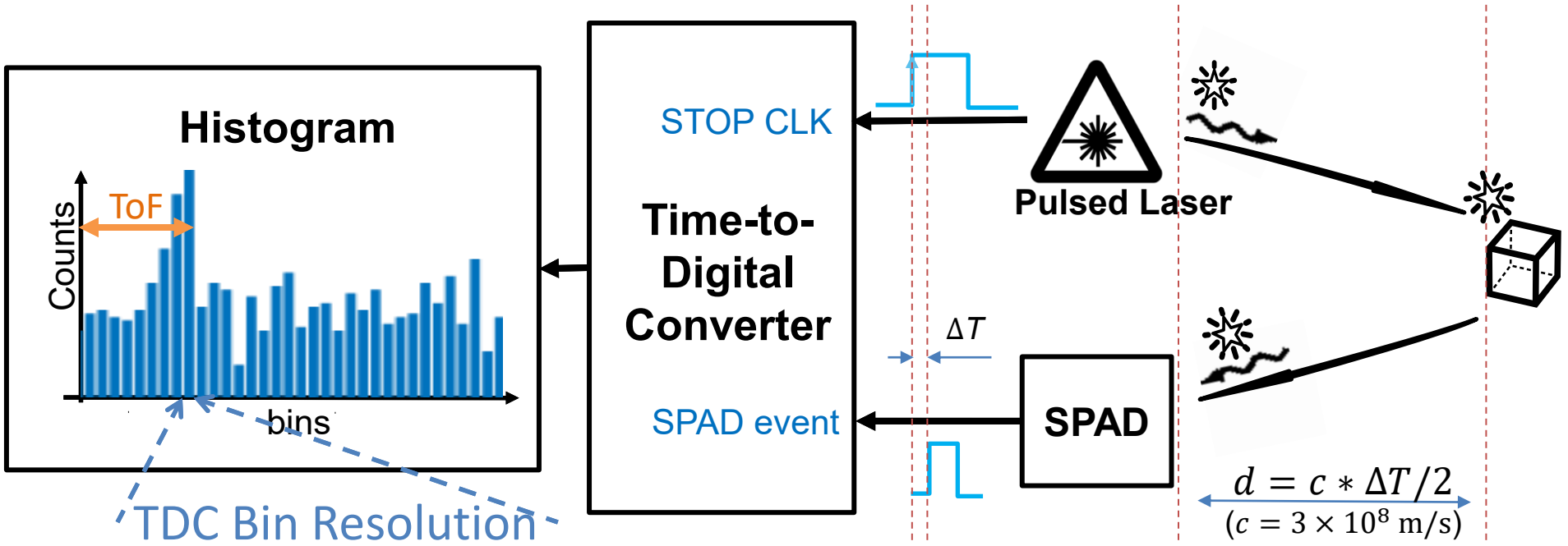
1 School of Engineering, The University of Edinburgh, United Kingdom

2 Now with Sony EUTDC, Trento, Italy

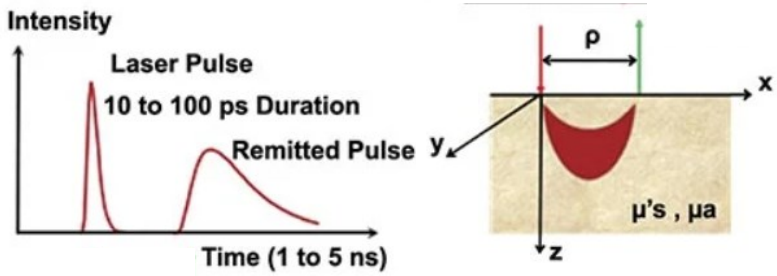
Outline

- Introduction – dToF sensor and FD-SOI
- Architecture of the TDC pixels and the DLL
- Experimental results
- Conclusion

Direct Time-of-Flight (dToF) Systems

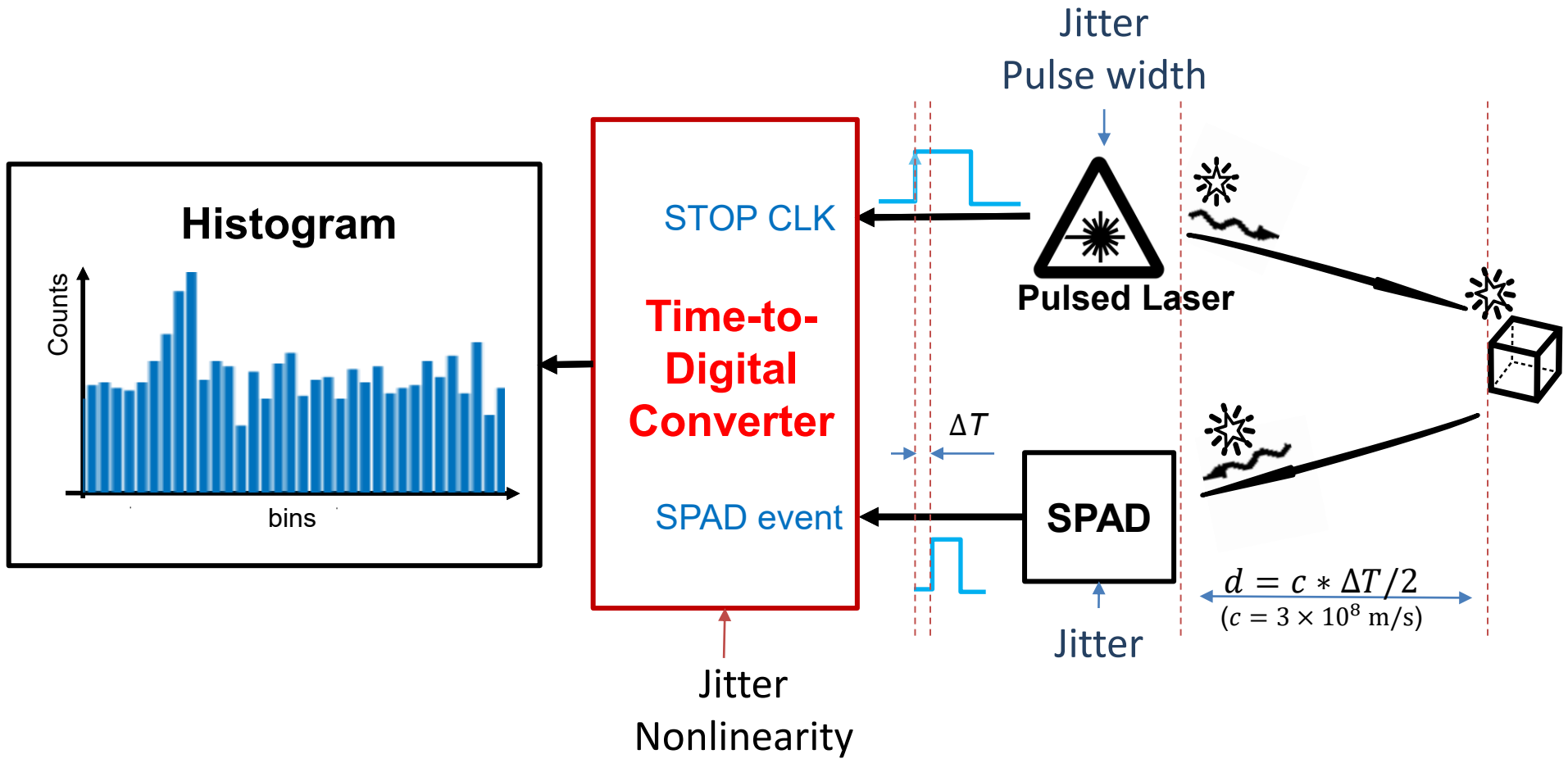


… in Different Depth Scenes

Outdoor	Indoor	Biomedical
		**Time Domain – Near Infrared Spectroscopy (TD-NIRS)**  [Torricelli et al. NeuroImage 2014]
Bin Resolution: **~ 700 ps**	**~ 350 ps**	**~ 70 ps**
Max Range **~ 1.4 us / 200m**	**~ 40 ns / 5m**	**~ 1.4 ns / 20cm**

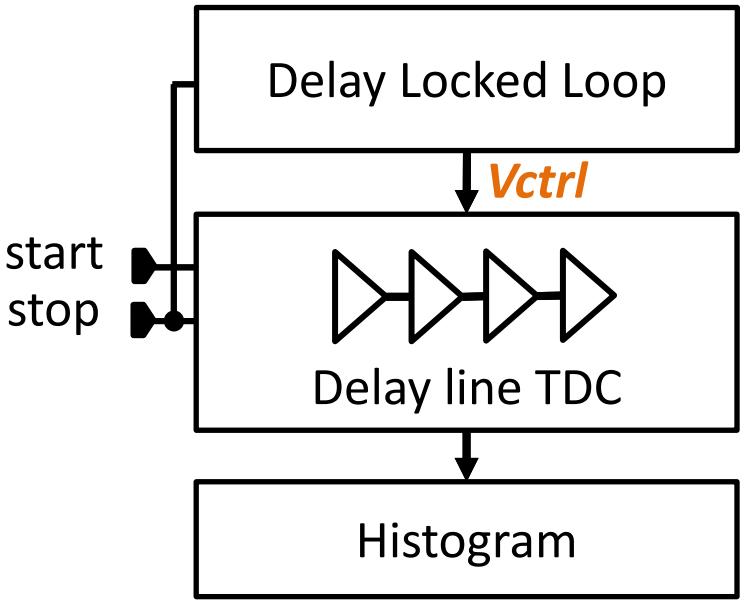
Accuracy Requirement

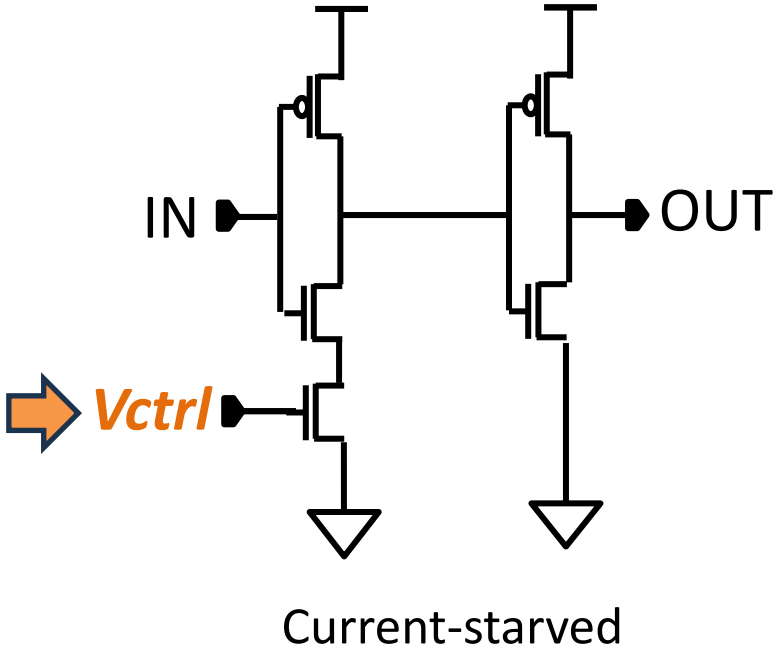
Direct Time-of-Flight (dToF) Systems



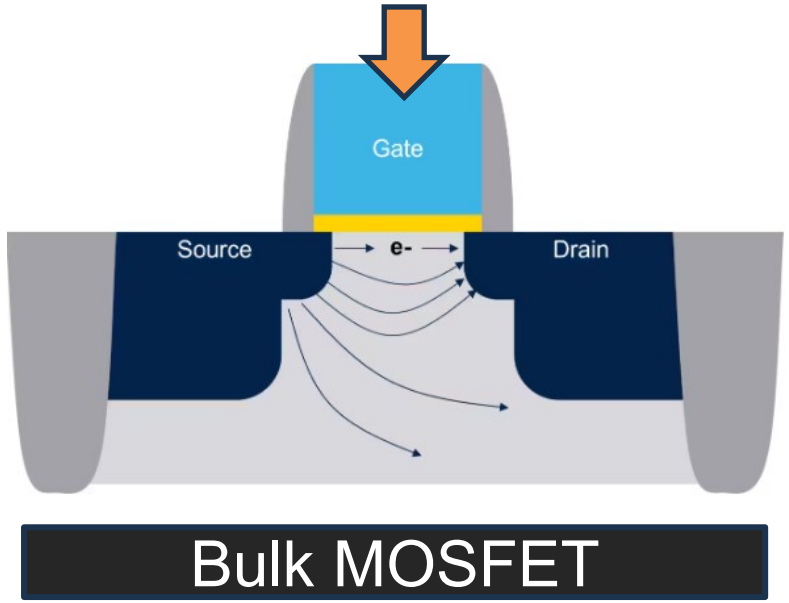
Process, Voltage, Temperature (PVT) variation

Conventional PVT-insensitive TDC Design





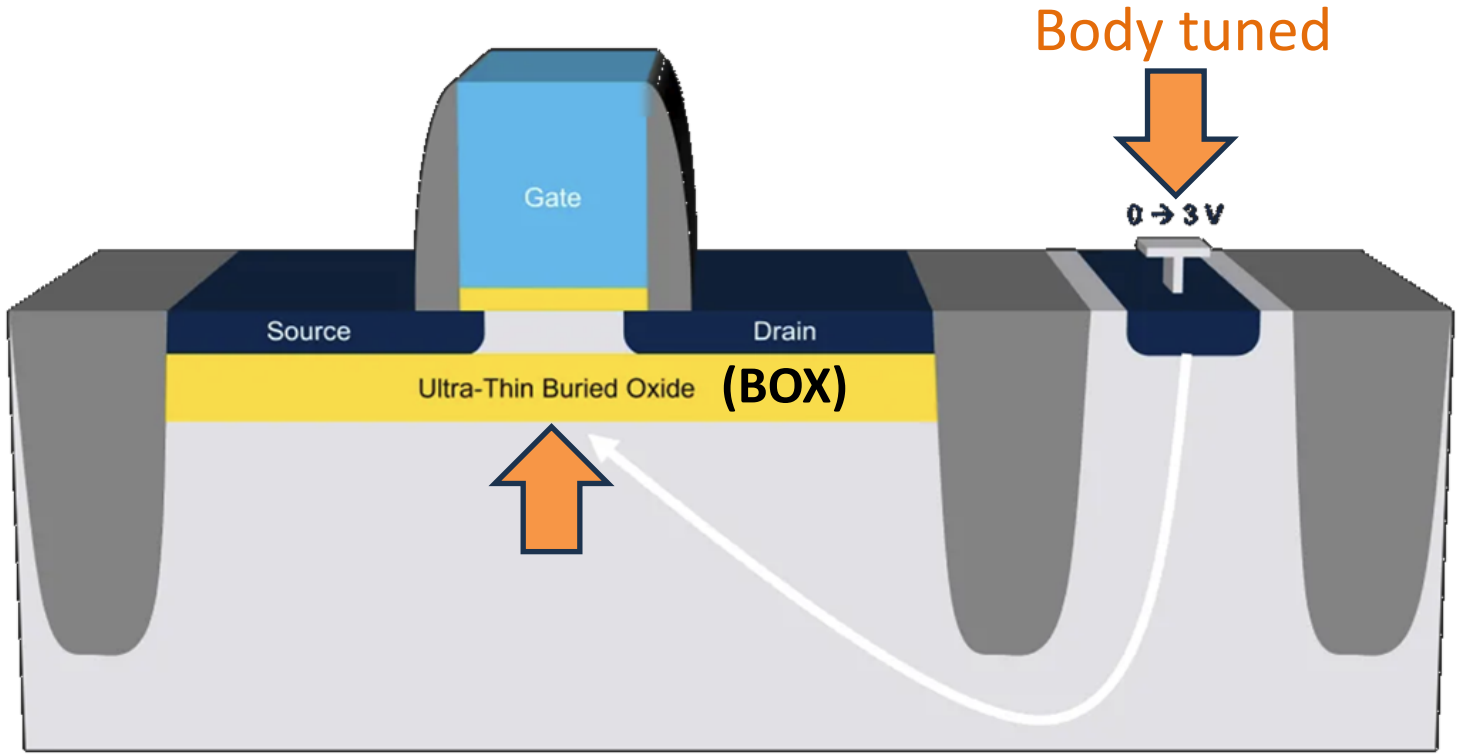
Gate tuned



[STMicroelectronics]

This Work

- Planar technology
- Lower leakage current
- Lower process variability
- Vertical double gate structure

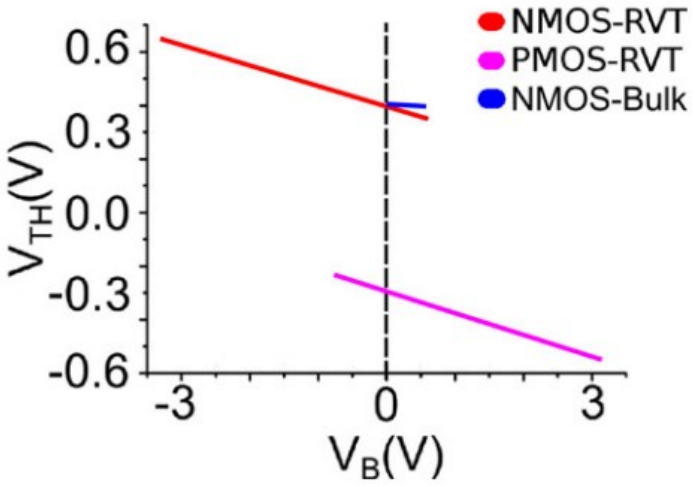


Fully Depleted Silicon-on-Insulator (FD-SOI)

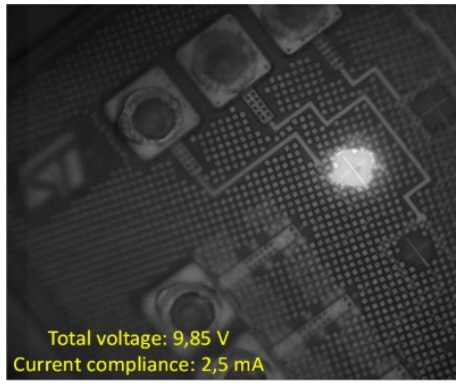
[STMicroelectronics]

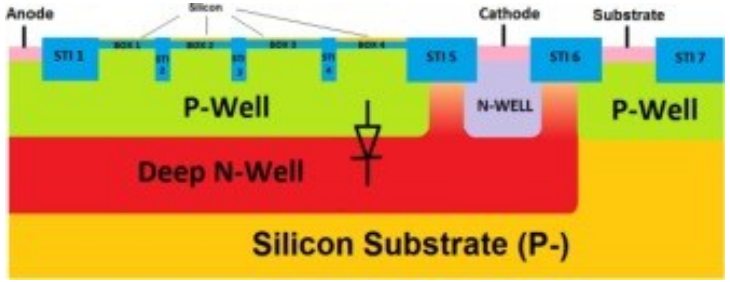
This Work

- Planar technology
- Lower leakage current
- Lower process variability
- Vertical double gate structure
- Efficient Vth modulation
- SPAD integration capability



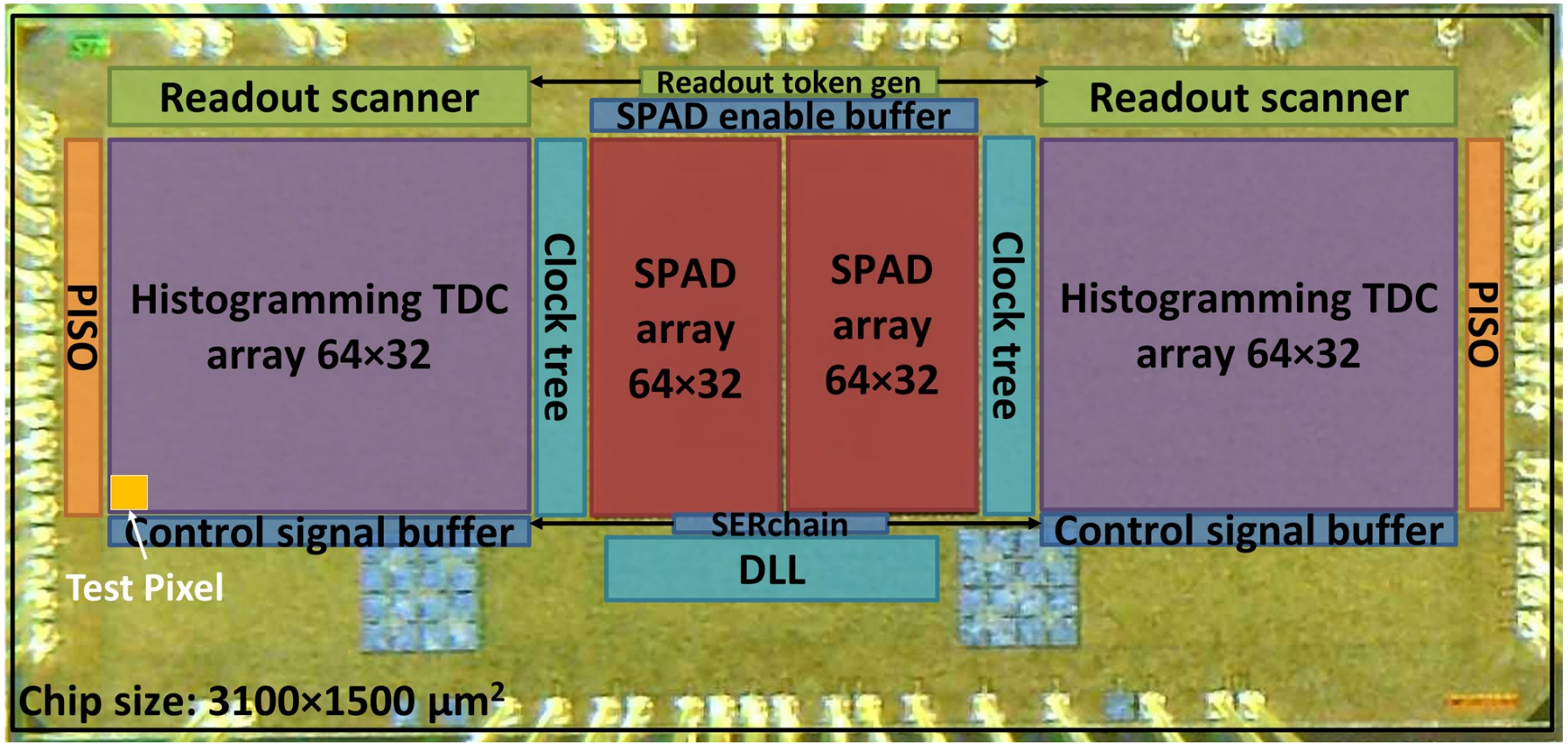
[I. Sourikopoulos et.al, ESSCIRC 2016]

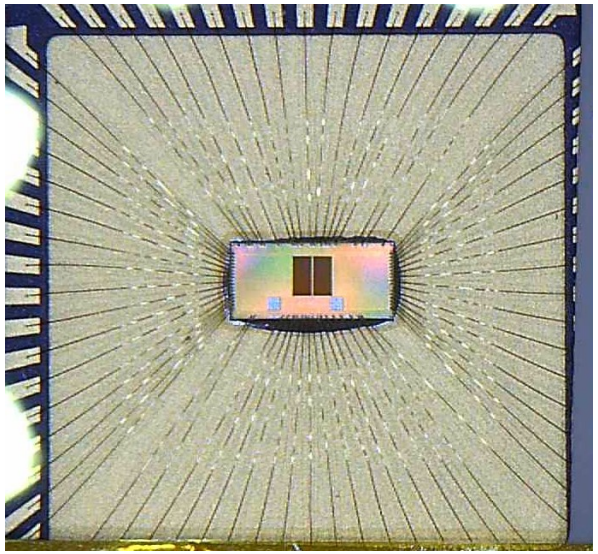




[T. C. de Albuquerque *et al.* ESSDERC 2018]

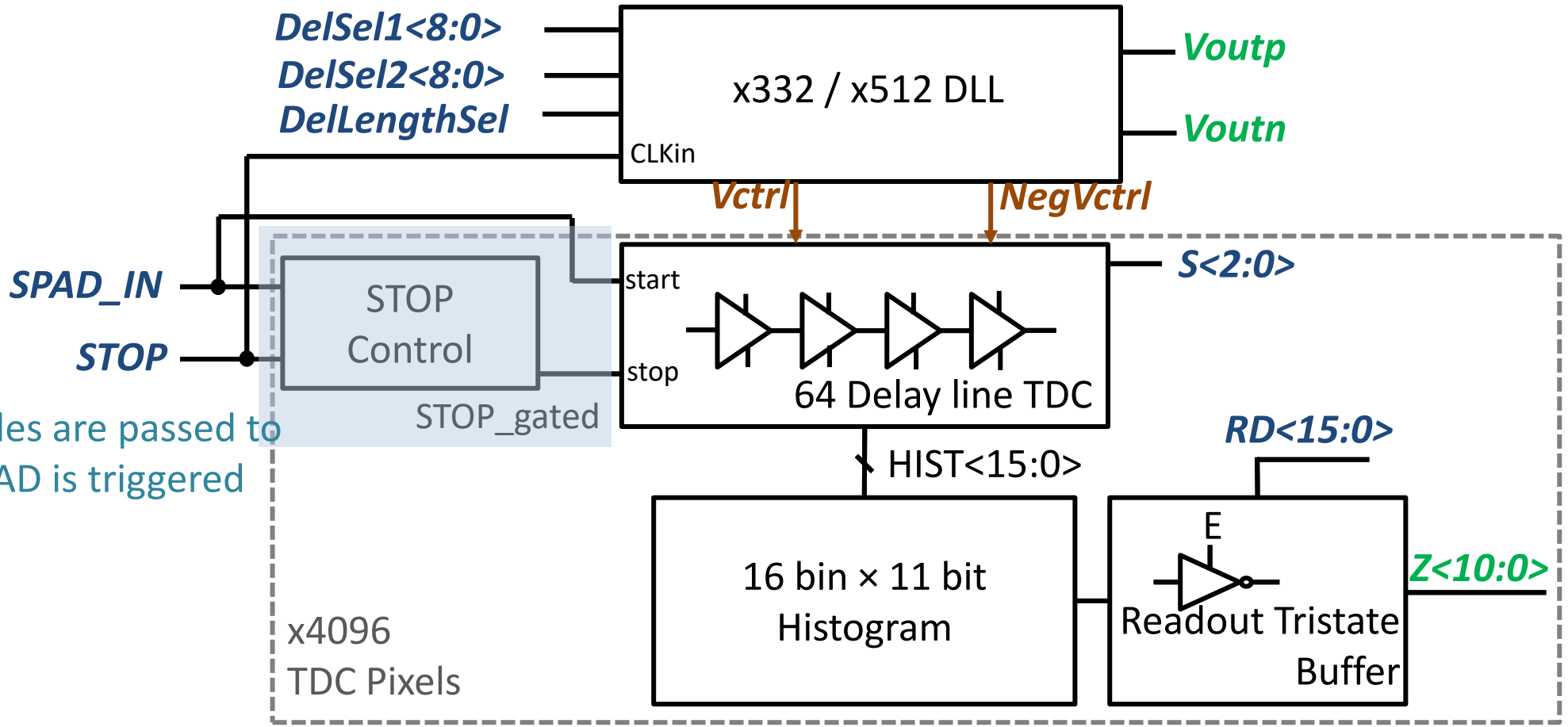
Chip Proposed





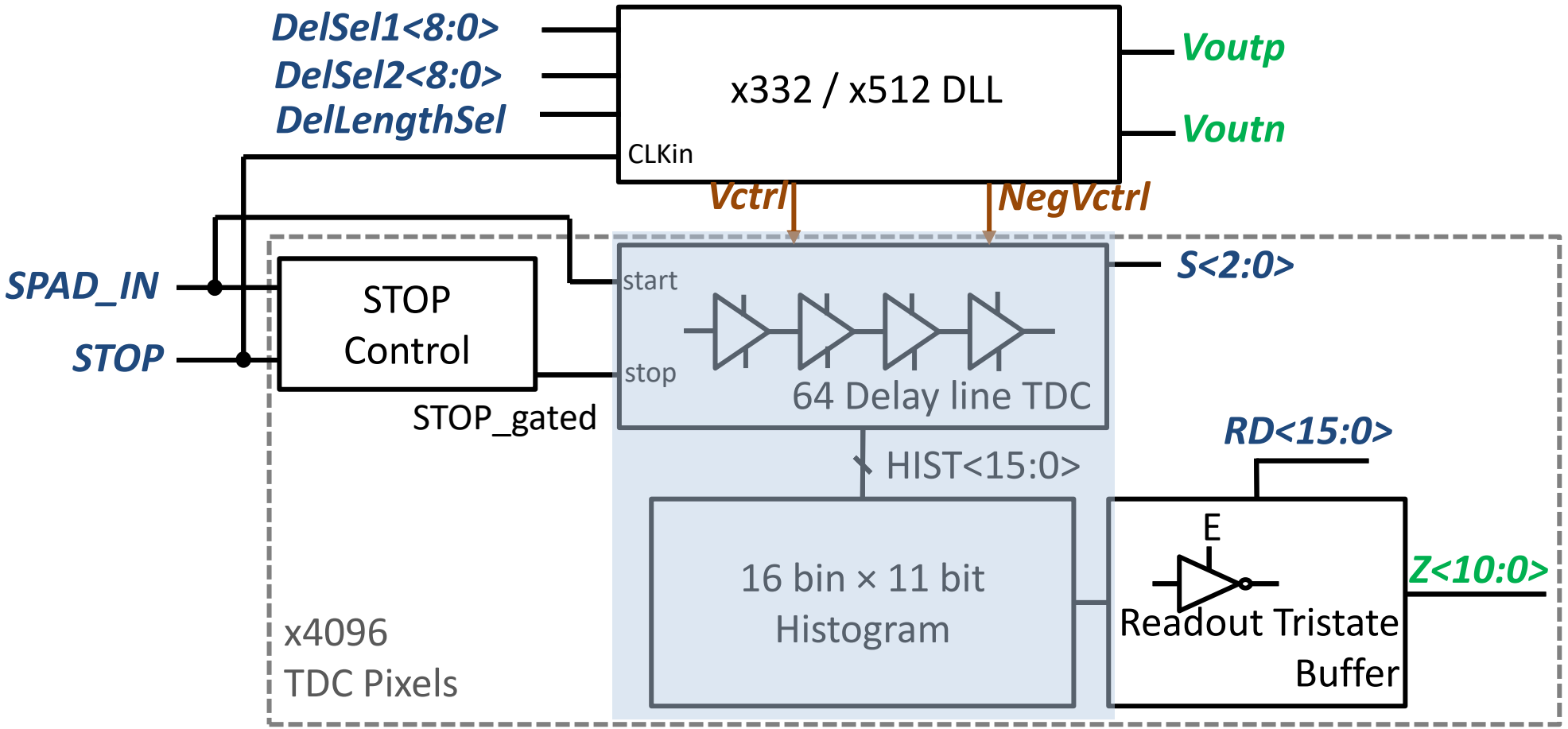
Manufactured in 28nm FD-SOI CMOS

DLL-based TDC Architecture

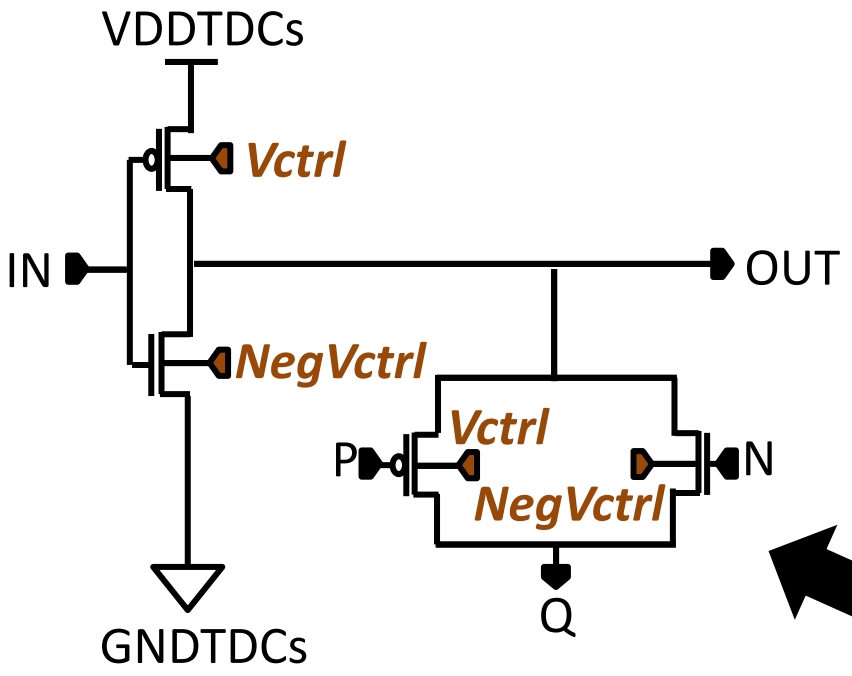


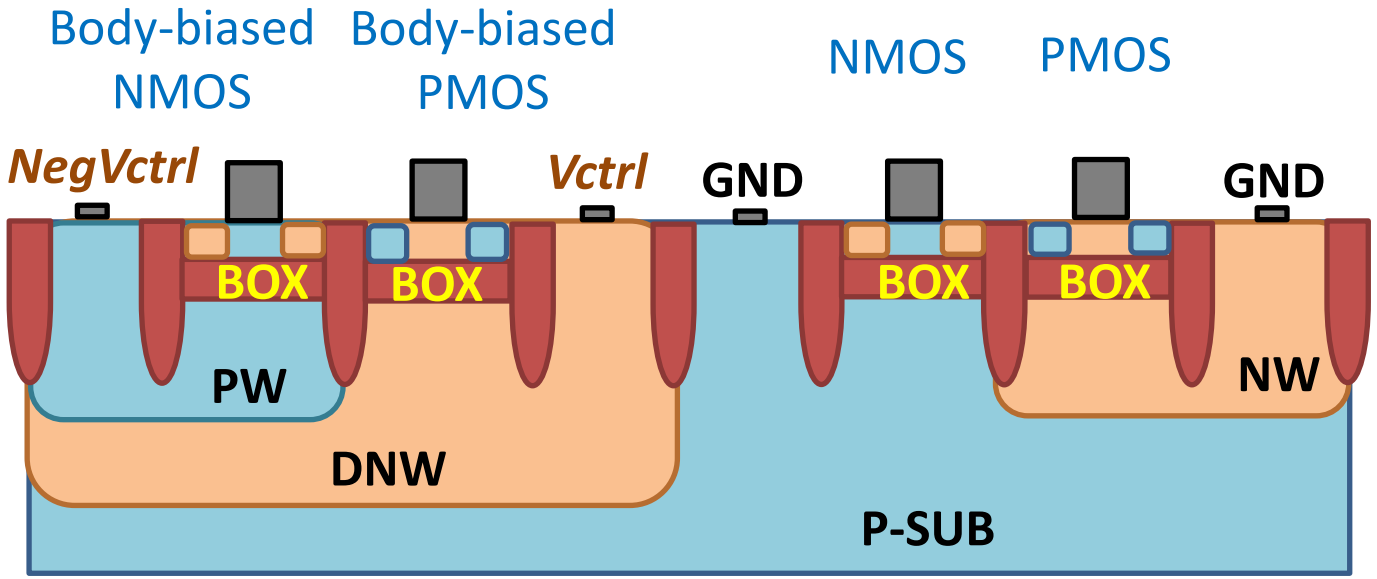
STOP cycles are passed to TDC if SPAD is triggered

DLL-based TDC Architecture

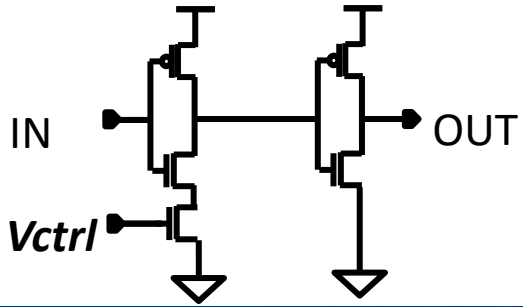


Body-biased Delay Element





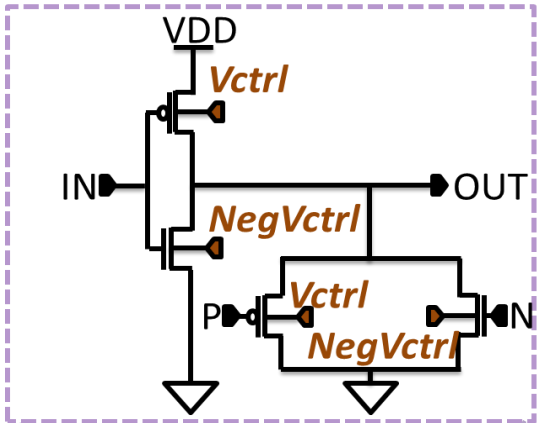
TDC delay line

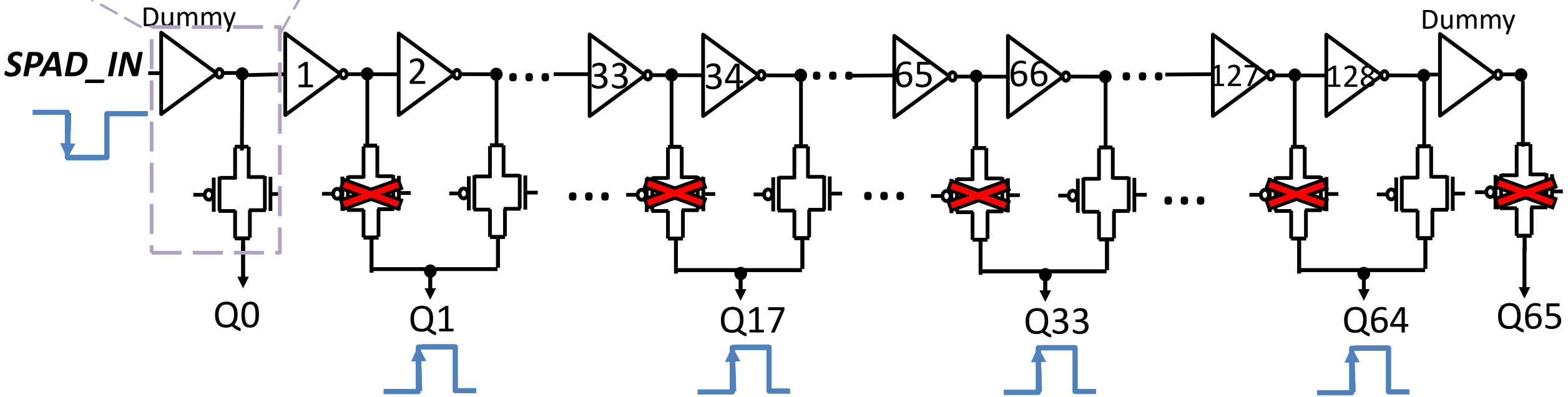


Other electronics
(DFFs, Histogram)

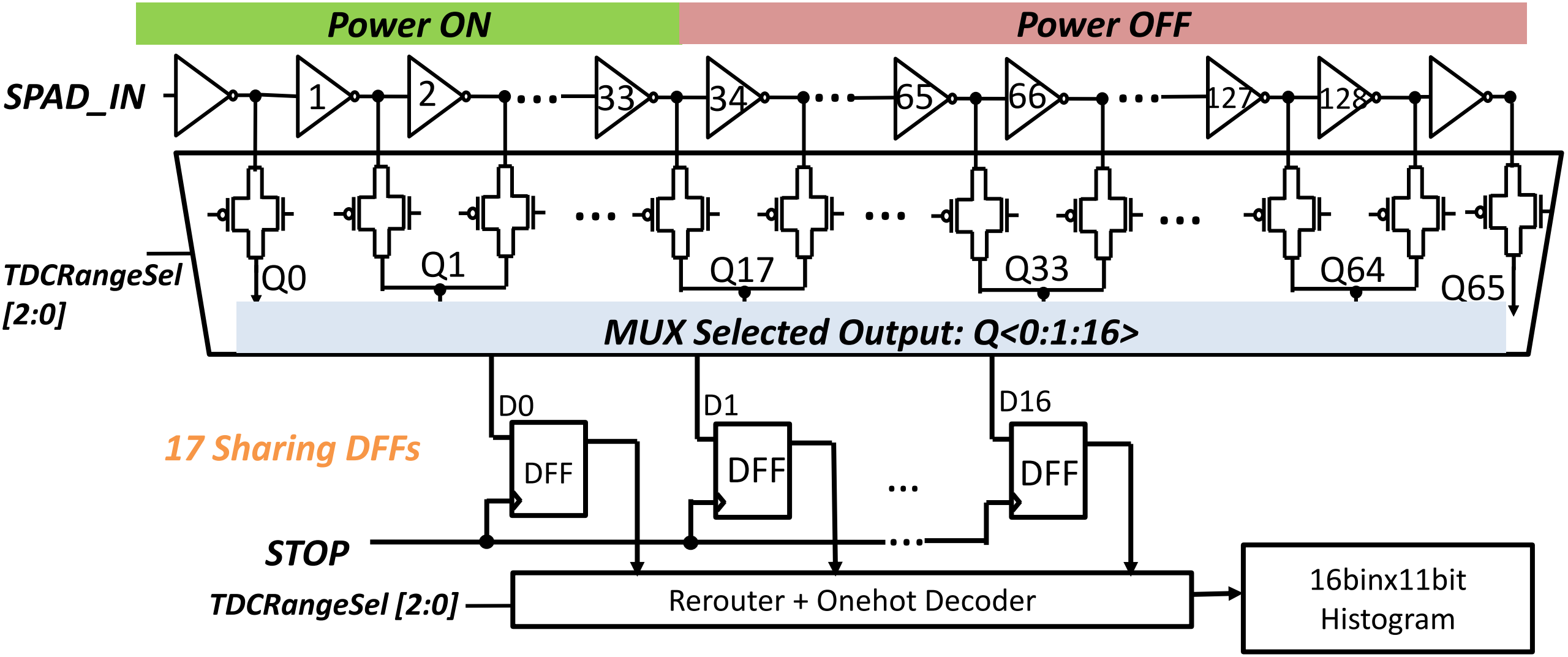
- Balance rising and falling time
- Full voltage swing
- Small area

64-Stage Delay Line TDC

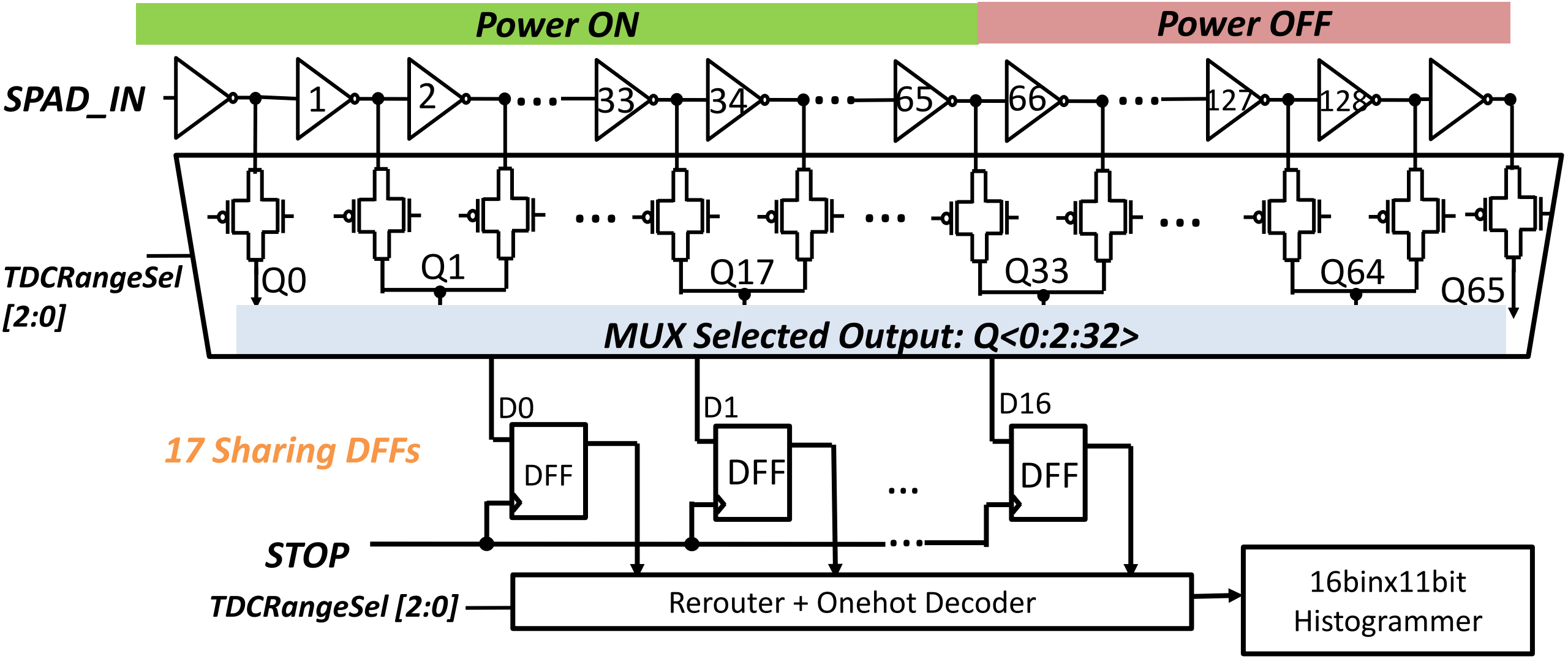




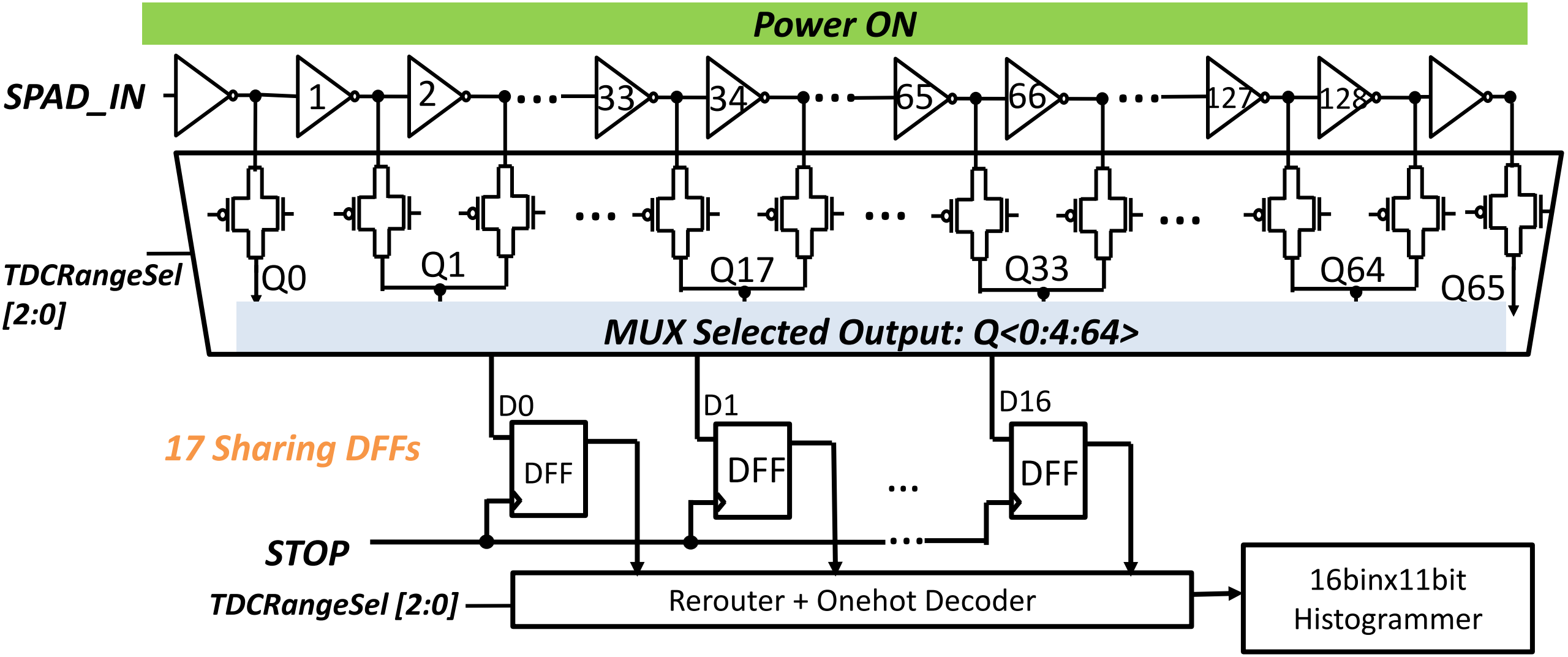
TDC Range 0 (0.87ns)



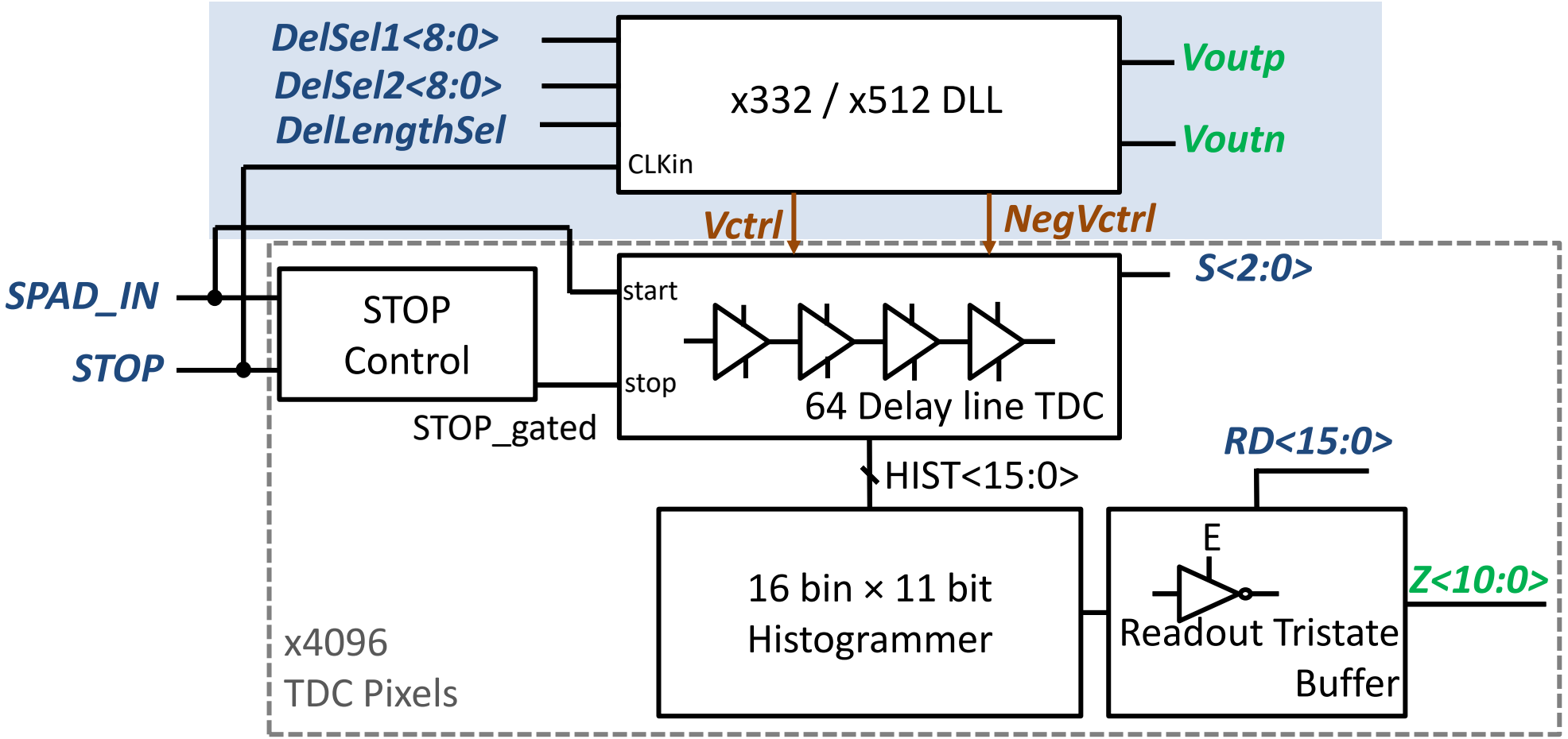
TDC Range 1 (1.76ns)



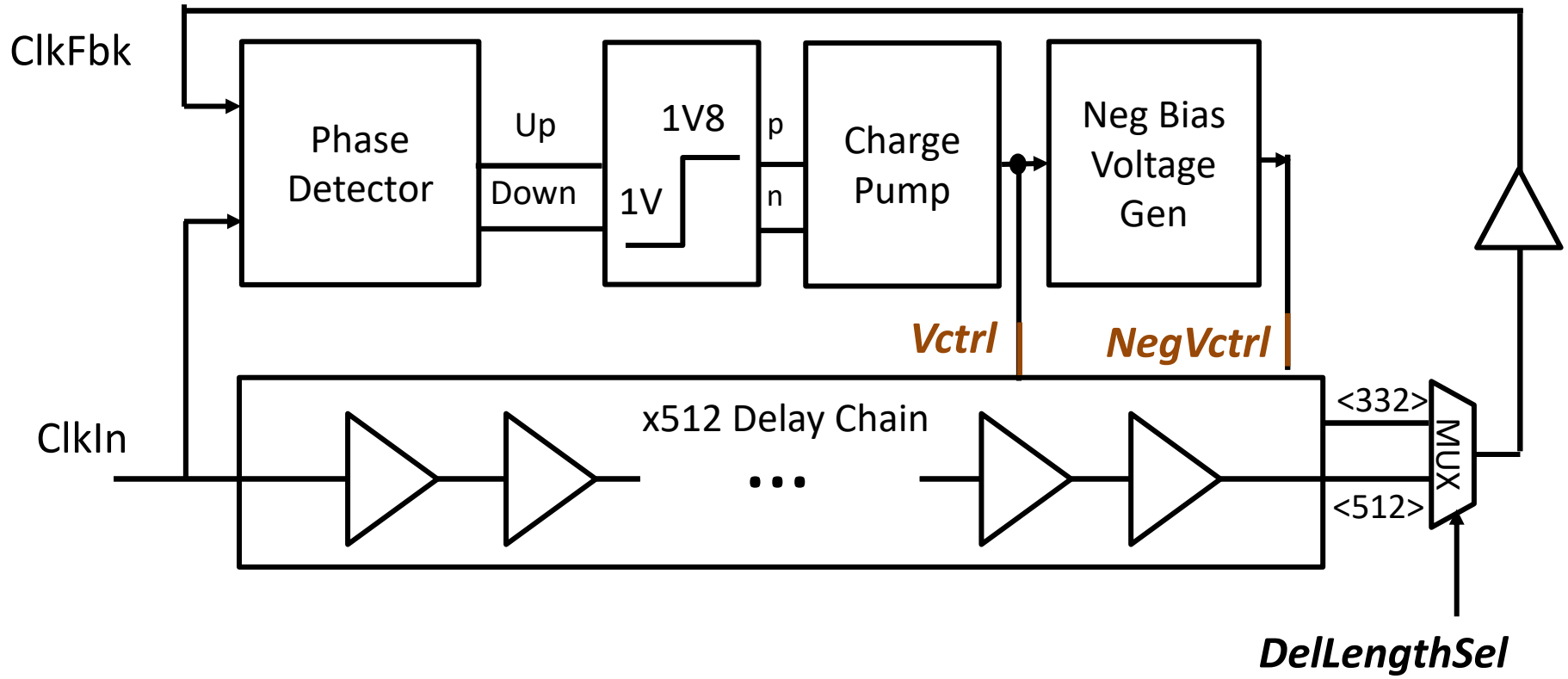
TDC Range 2 (2.24ns)



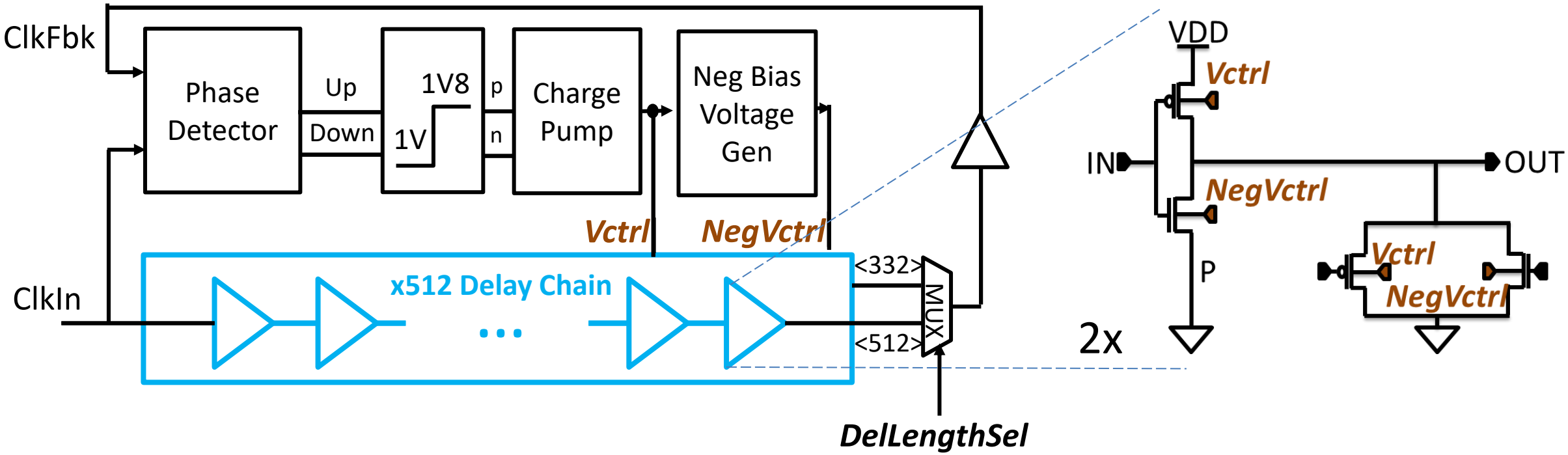
DLL-based TDC Architecture



Delay Locked Loop



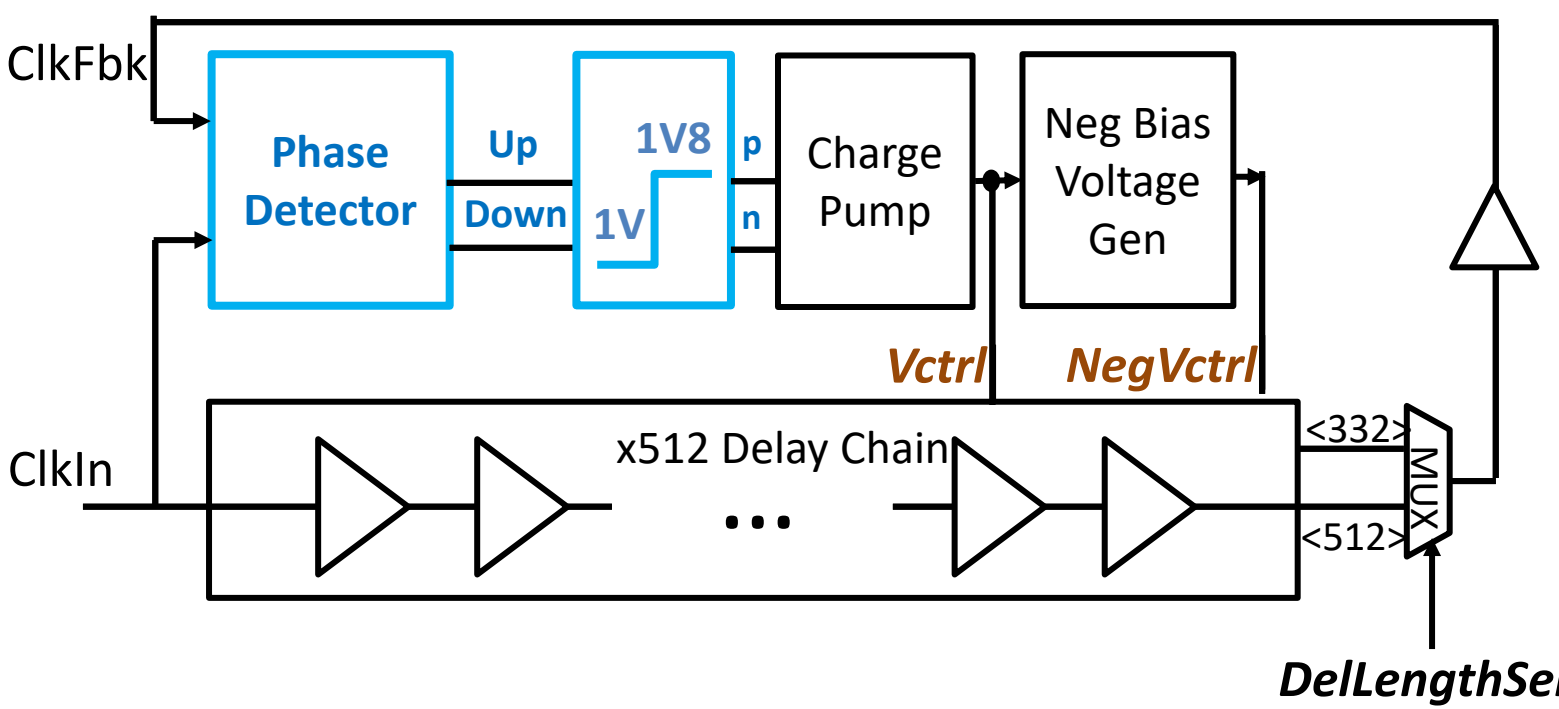
Delay Locked Loop

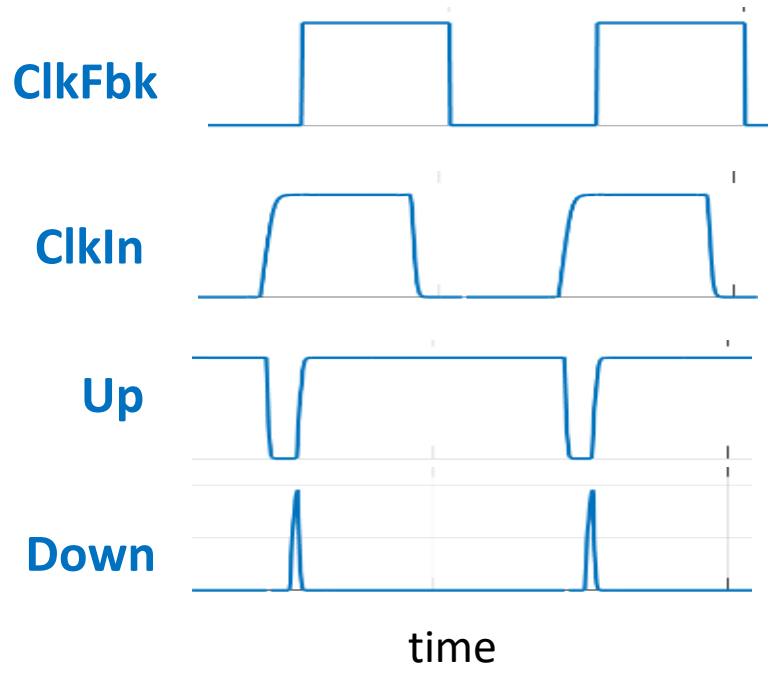


332 tap: 10ns range / 100MHz

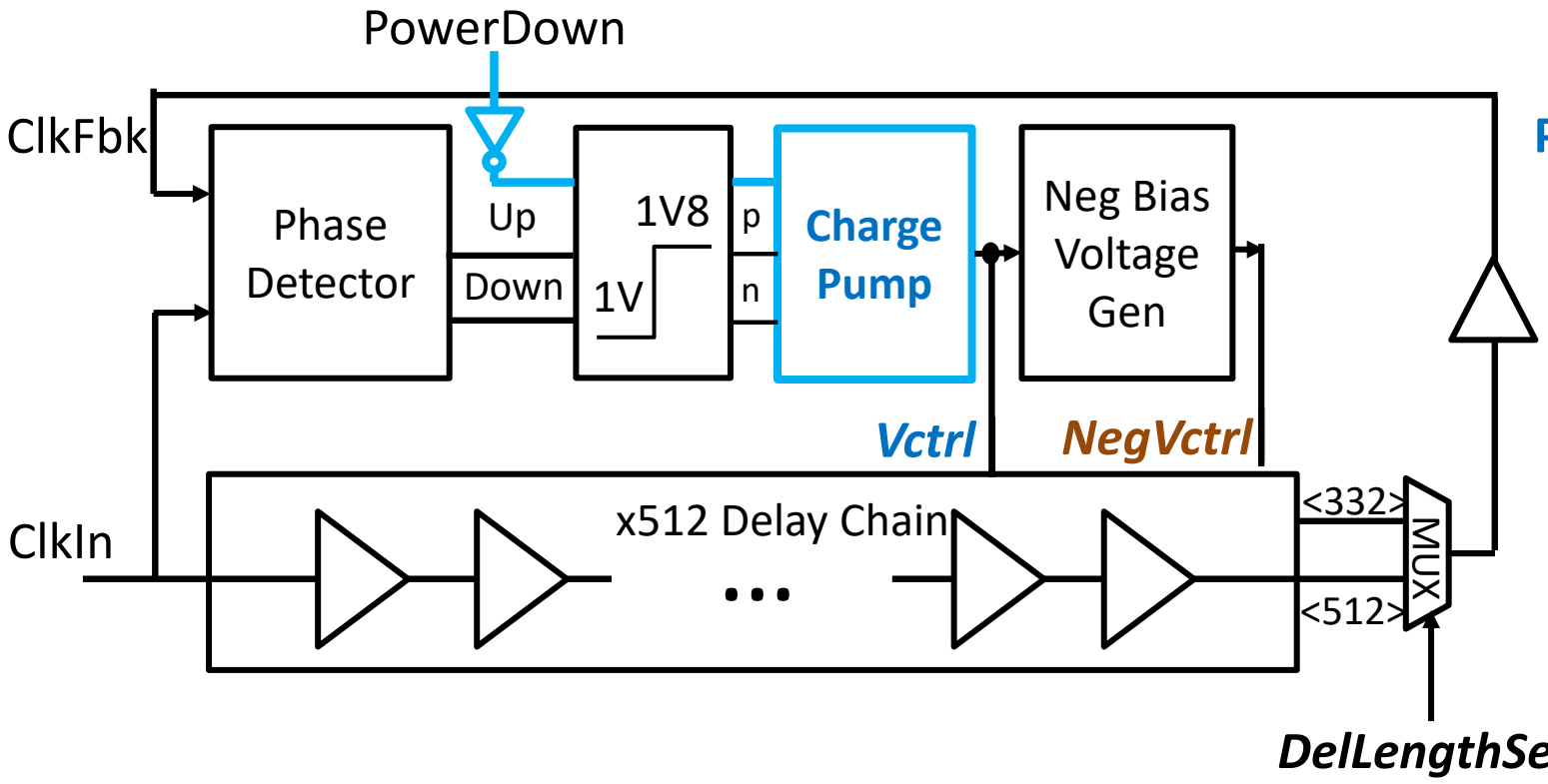
512 tap: 15ns range / 66.66MHz

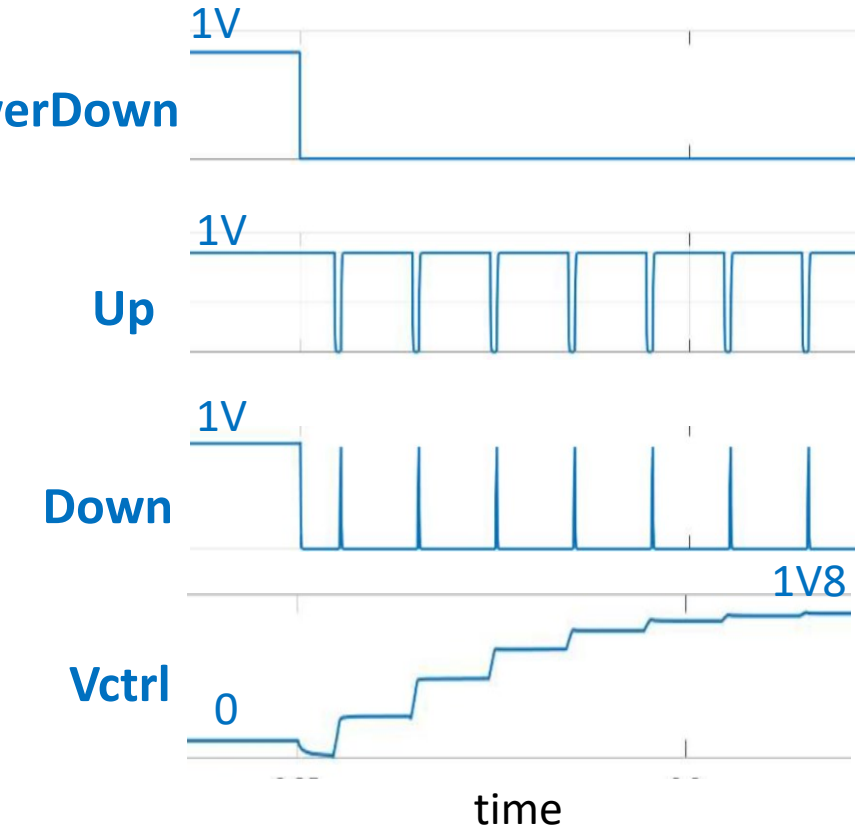
Delay Locked Loop



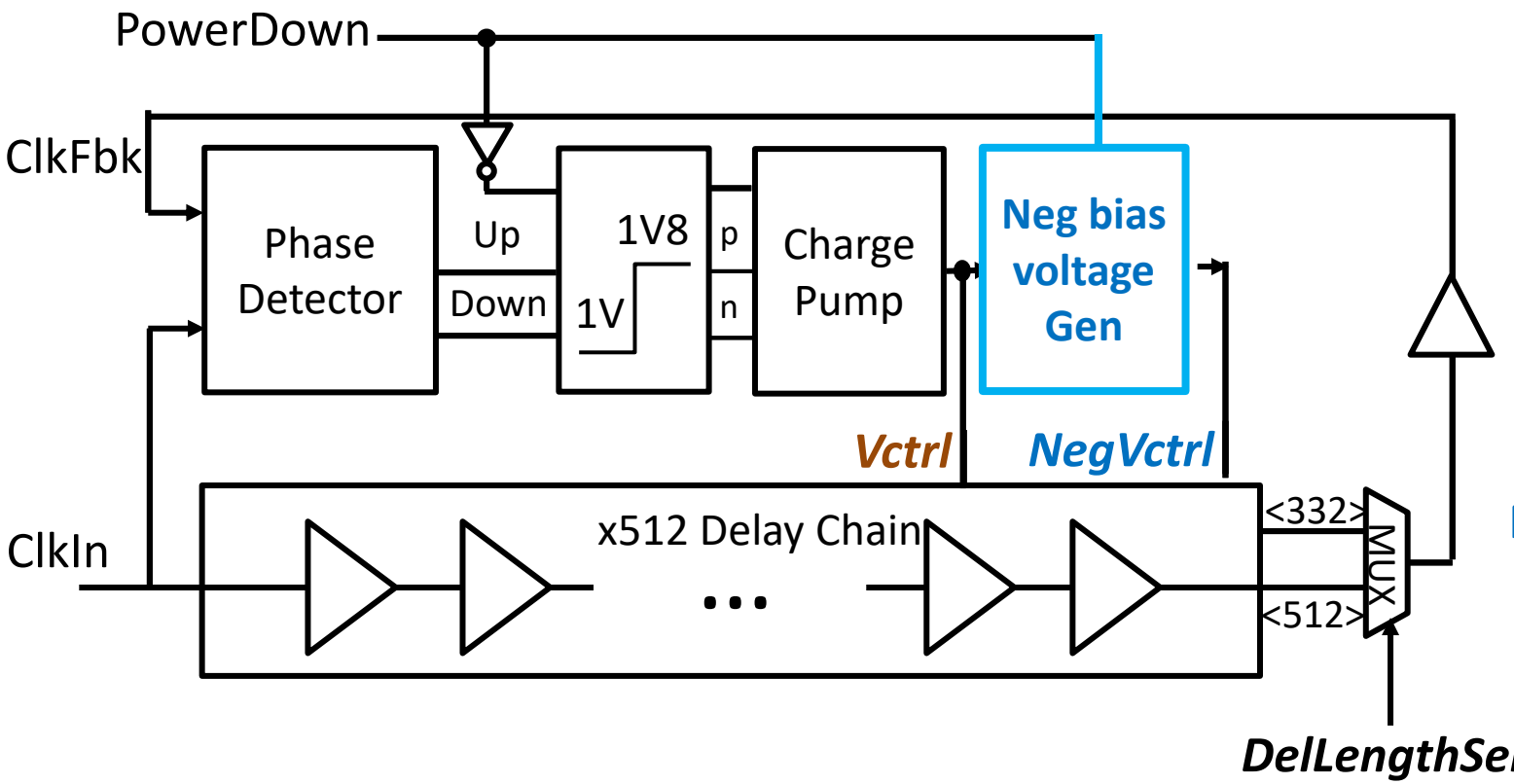


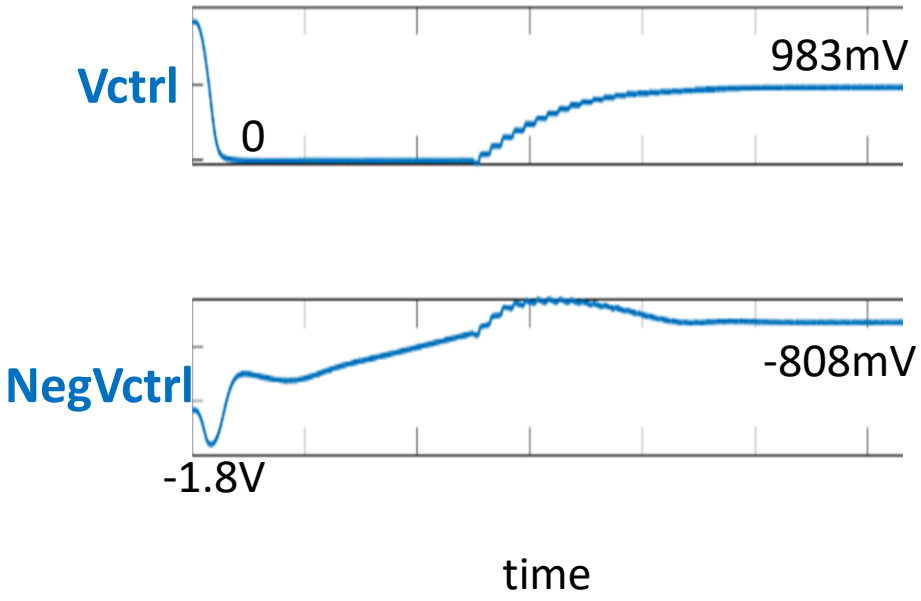
Delay Locked Loop



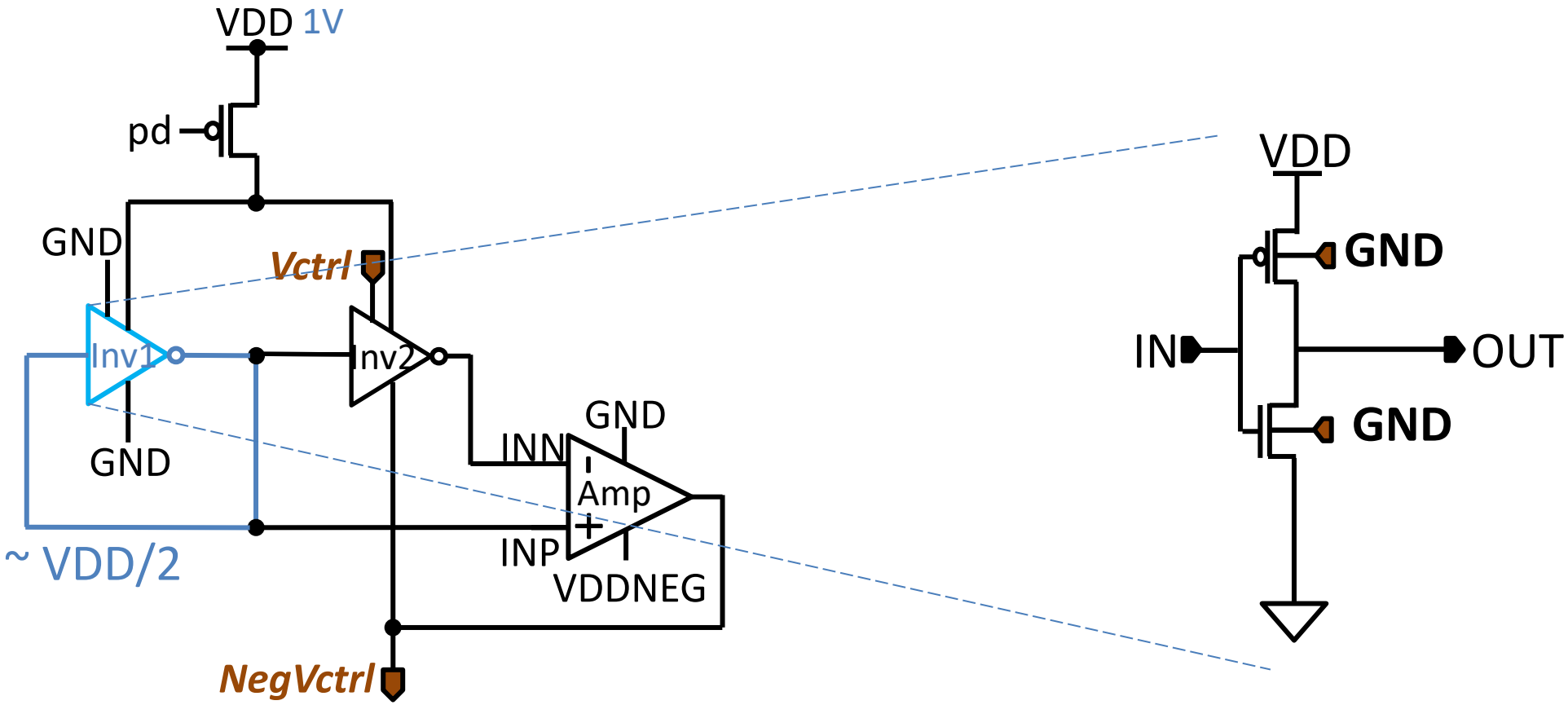


Delay Locked Loop

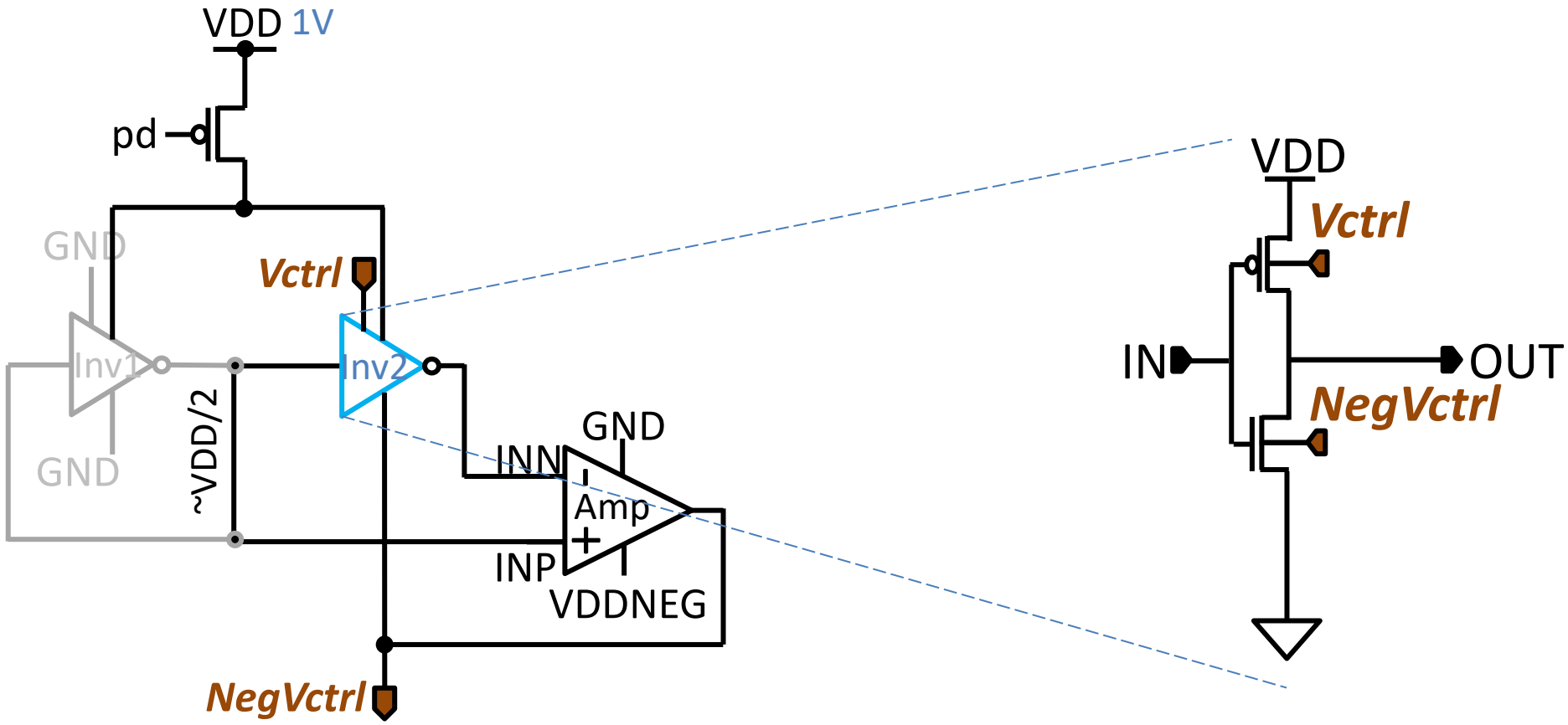




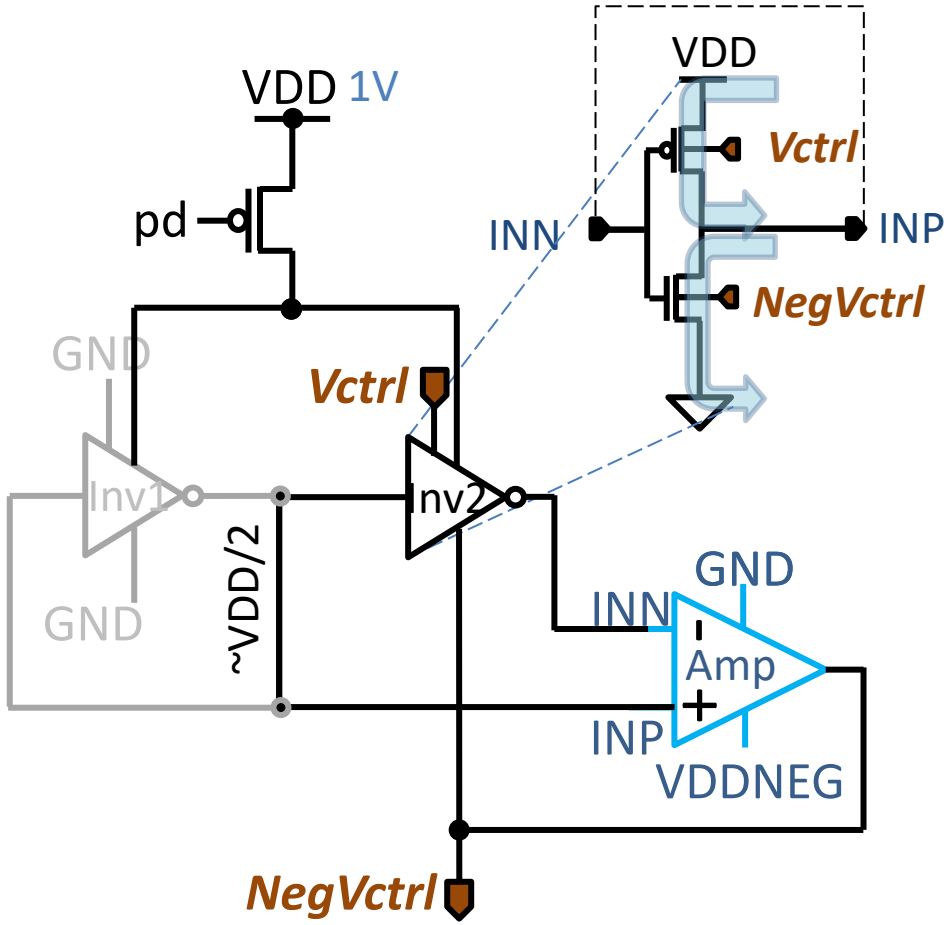
Negative Bias Voltage Generator

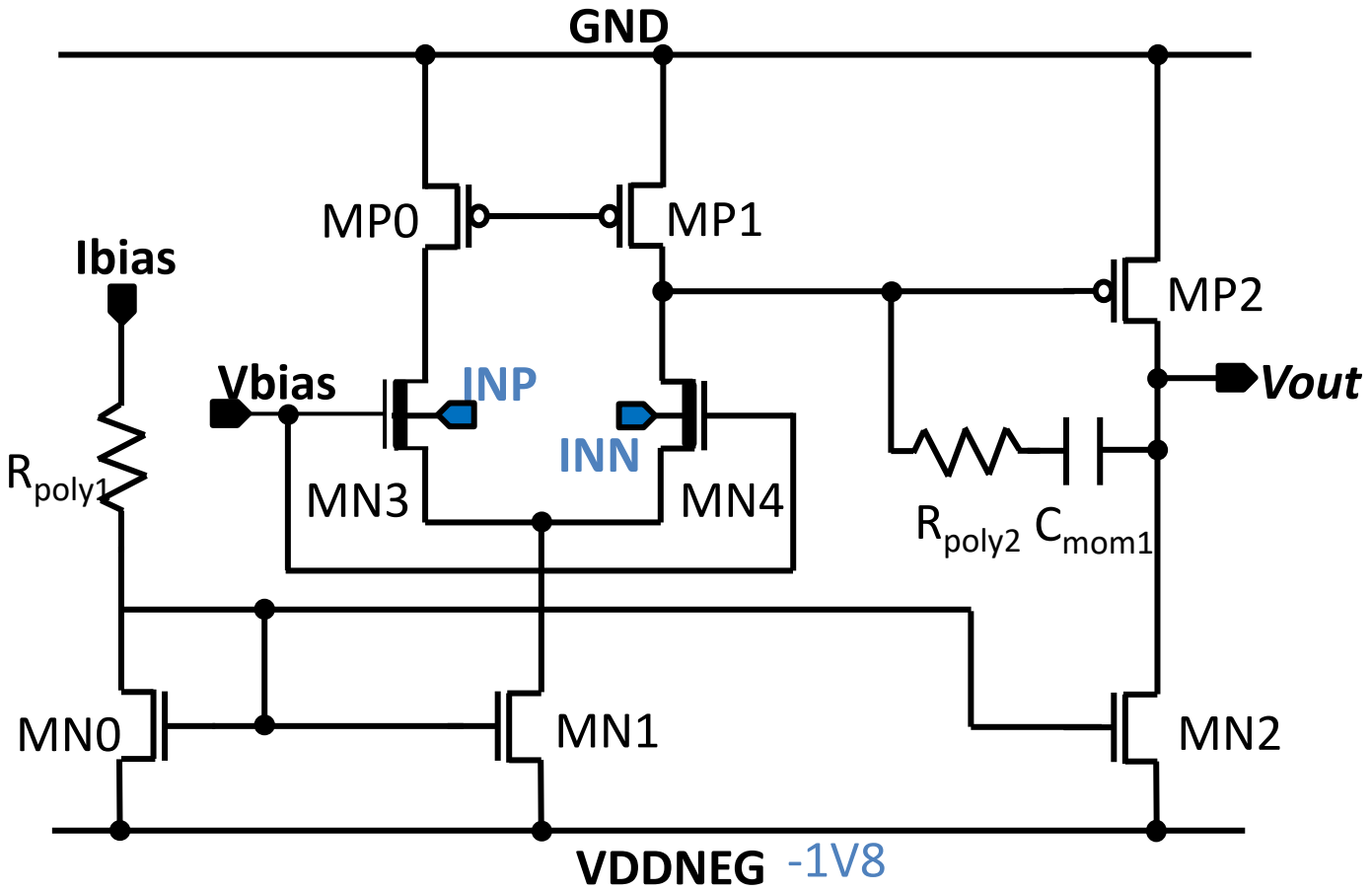


Negative Bias Voltage Generator



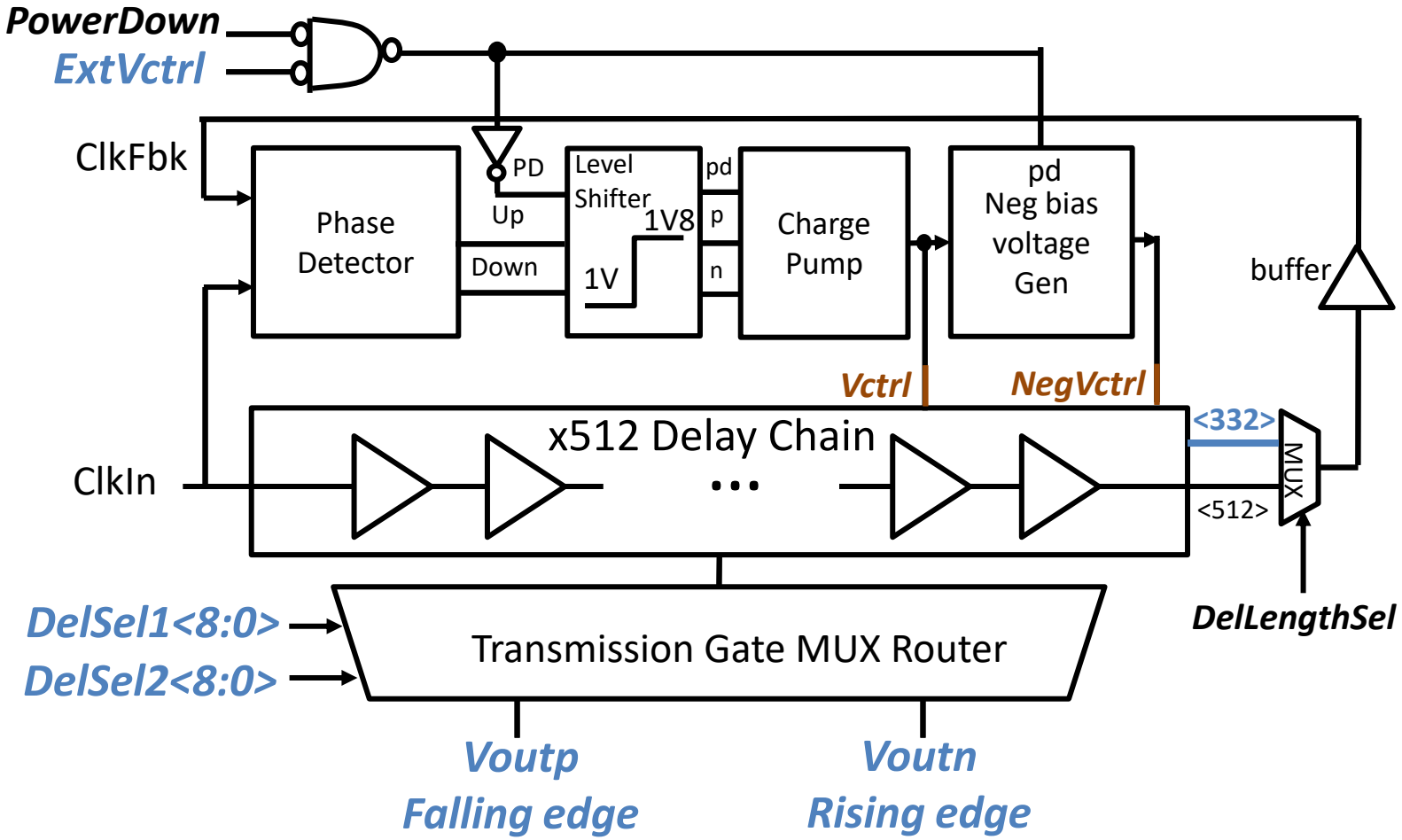
Negative Bias Voltage Generator

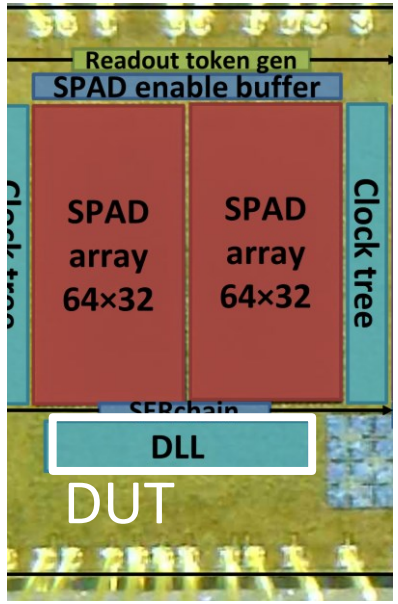


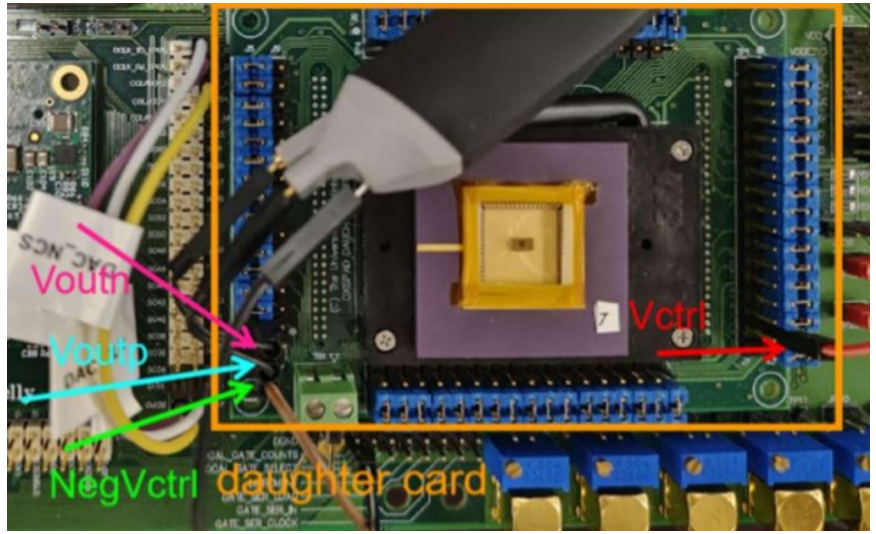


[G.de Stree et al. JSSC 2017]

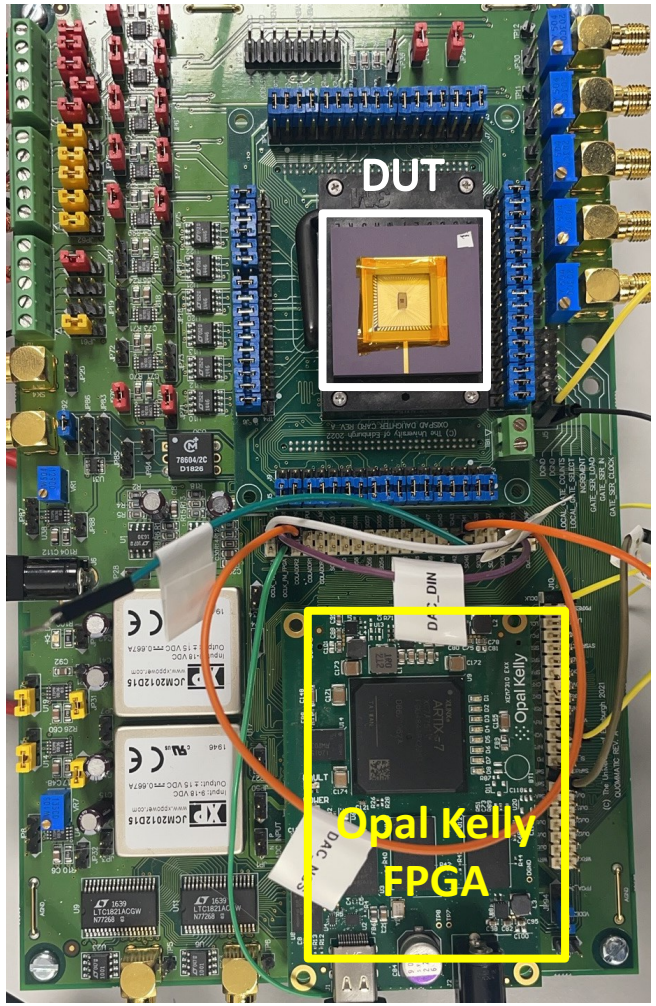
DLL Measurement

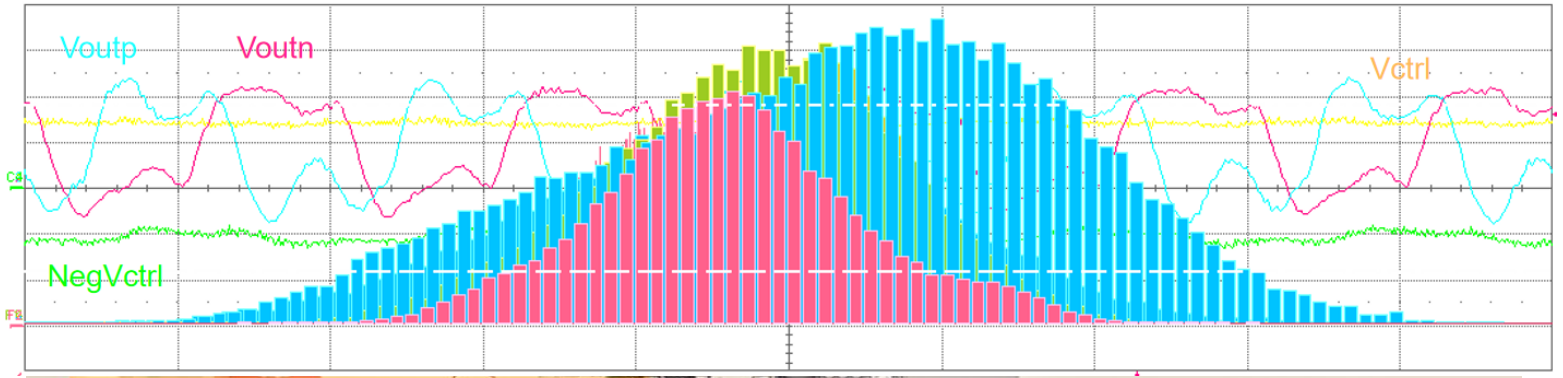


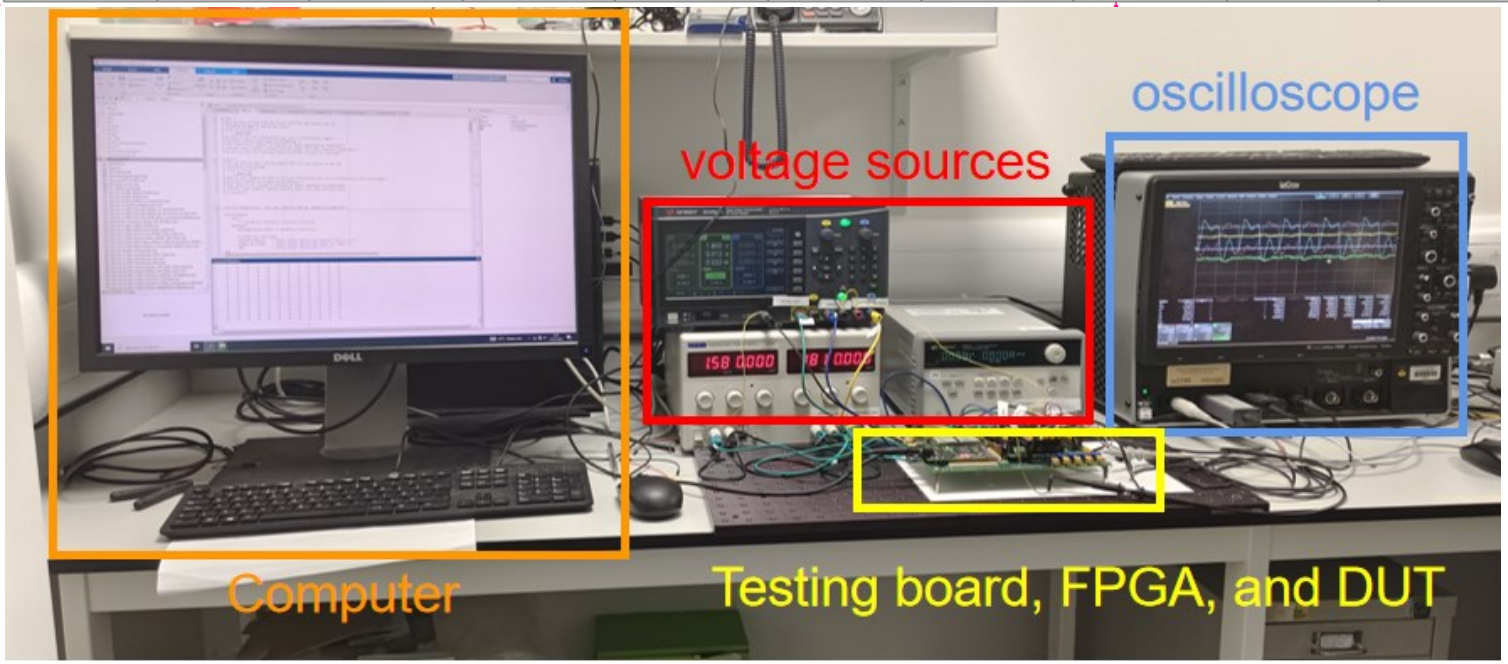




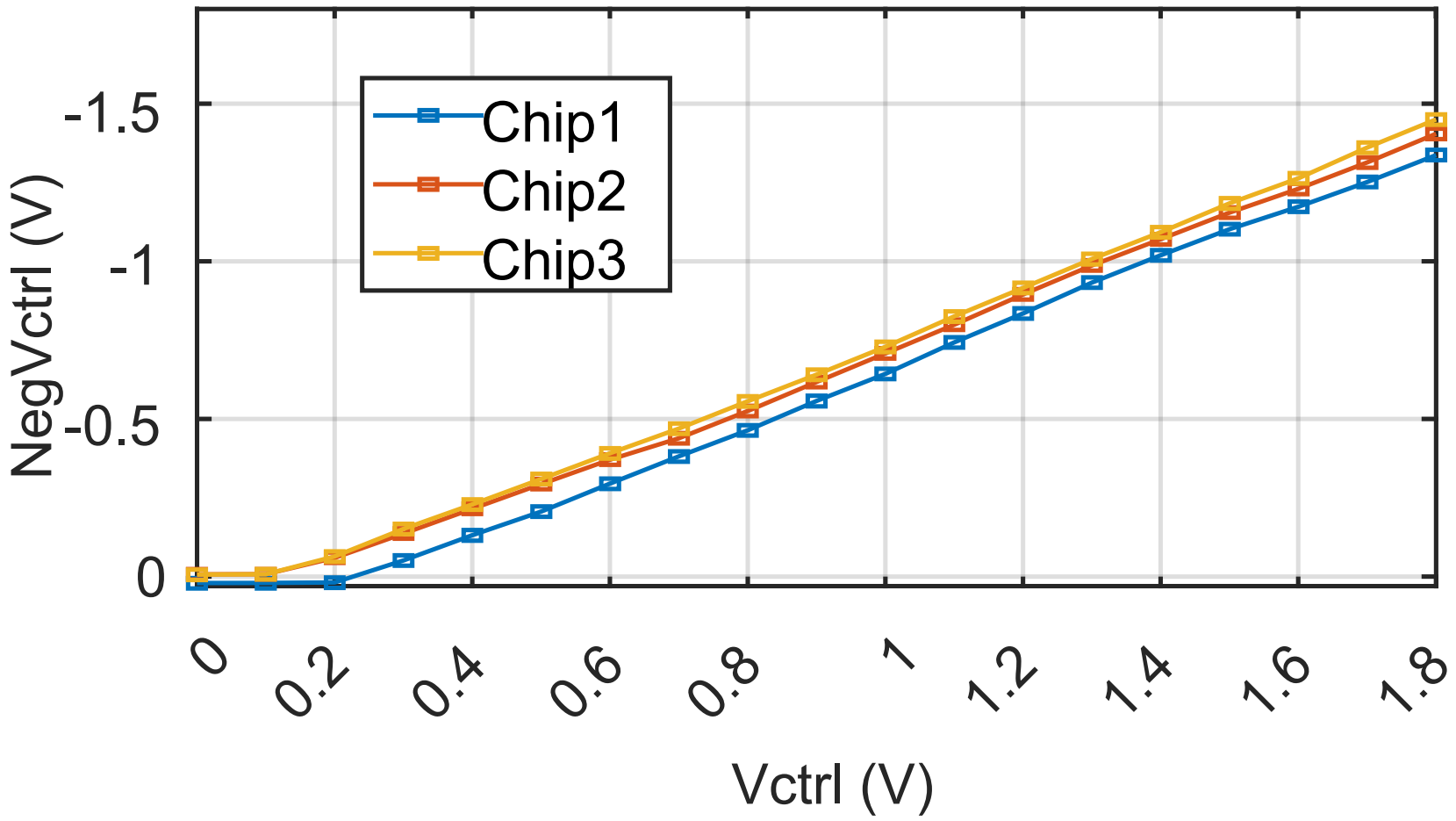
Experimental Setup



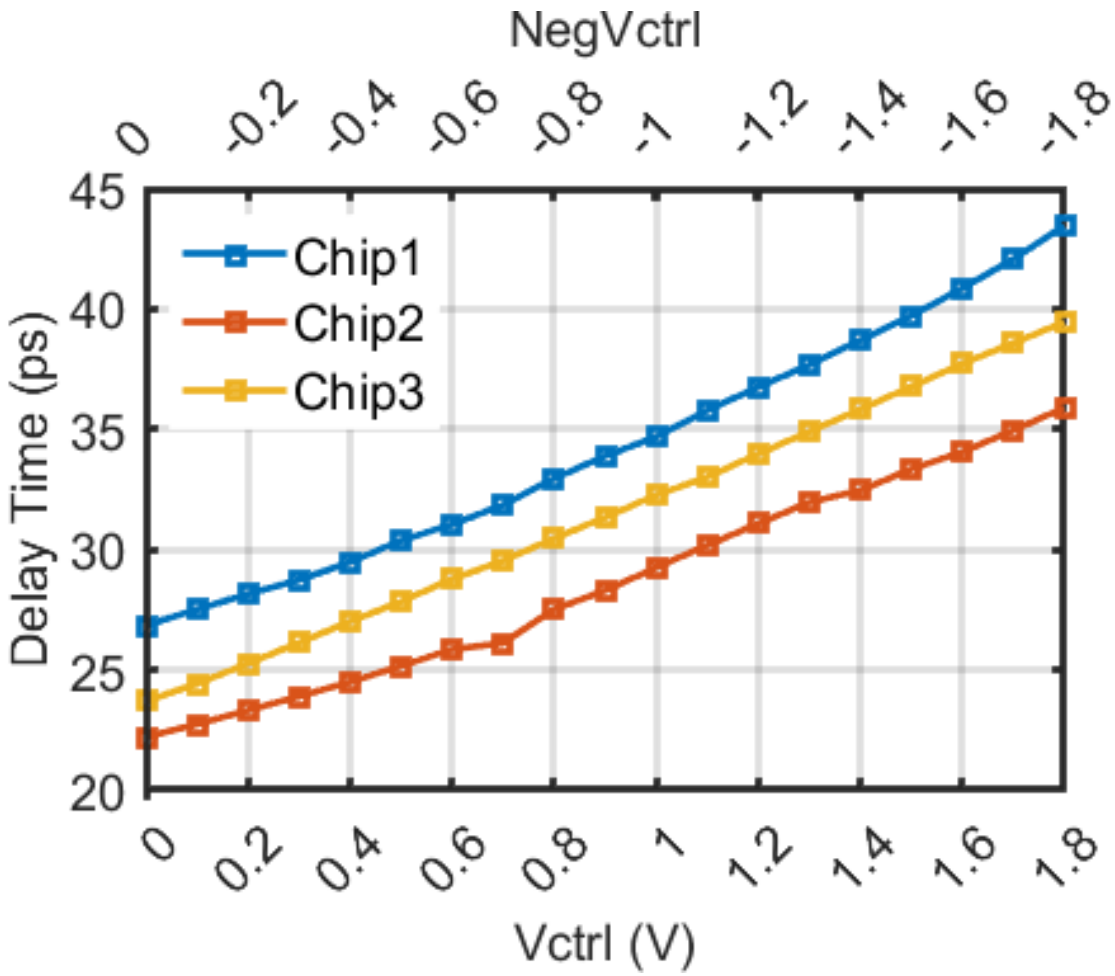




Negative Bias Voltage Generator



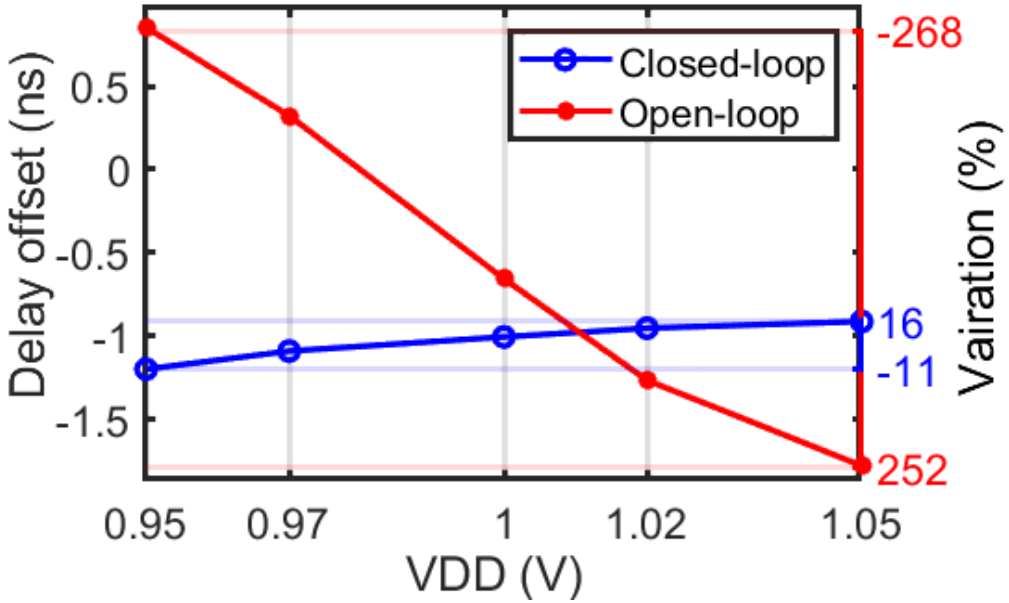
Propagation delay time against control voltages

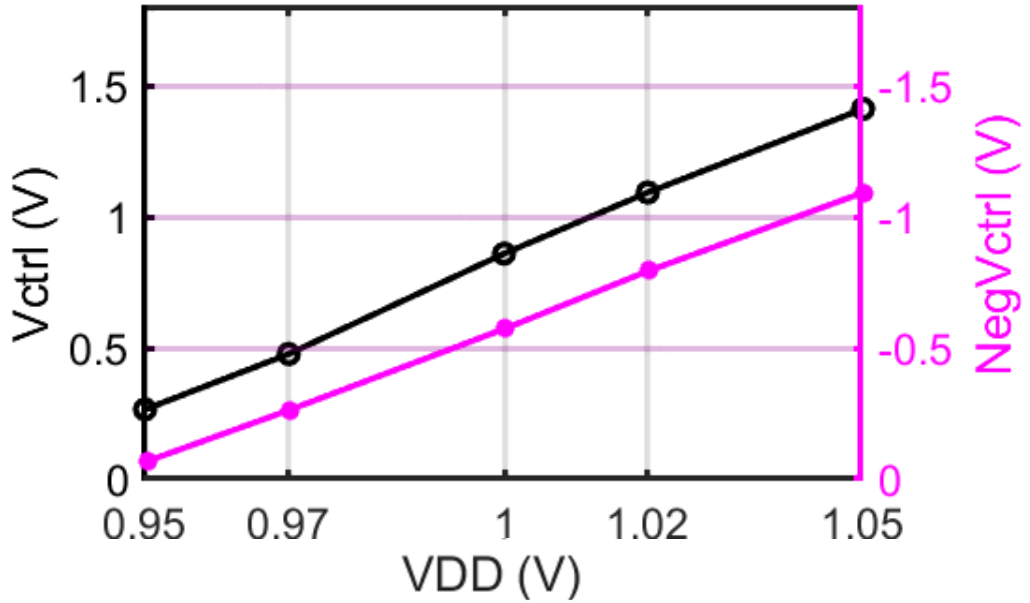


- Open-loop Configuration
- Tunning range: ~15.5ps/bin

DLL Phase Skew vs. Supply

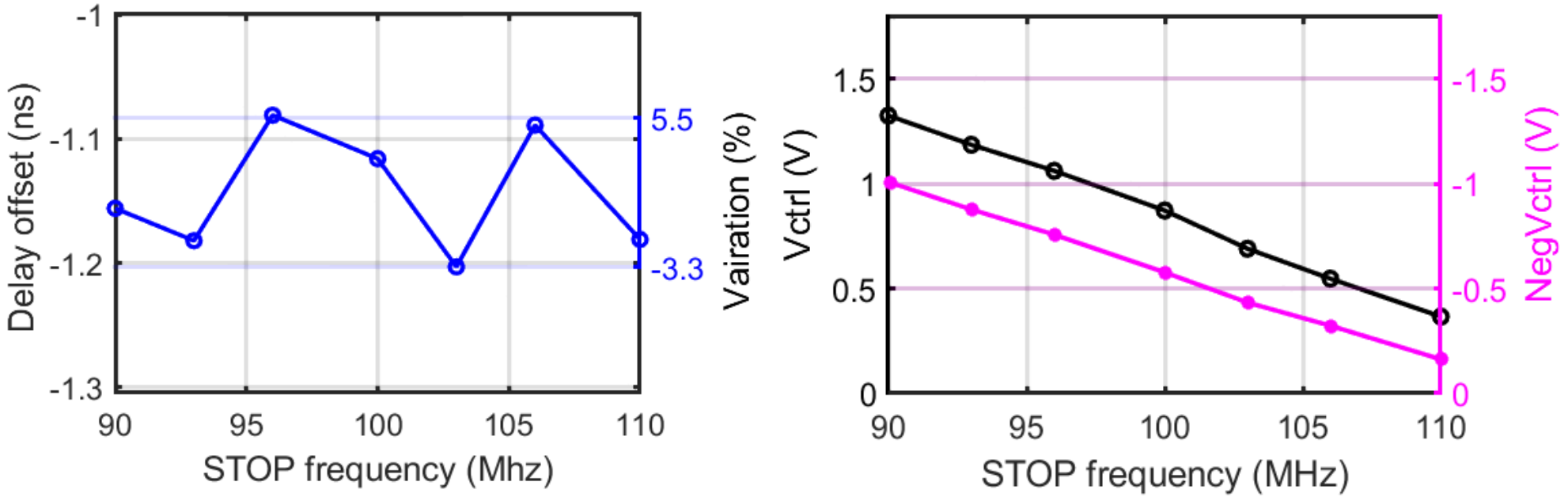
14x smaller variations in closed-loop DLL under 10% VDD change





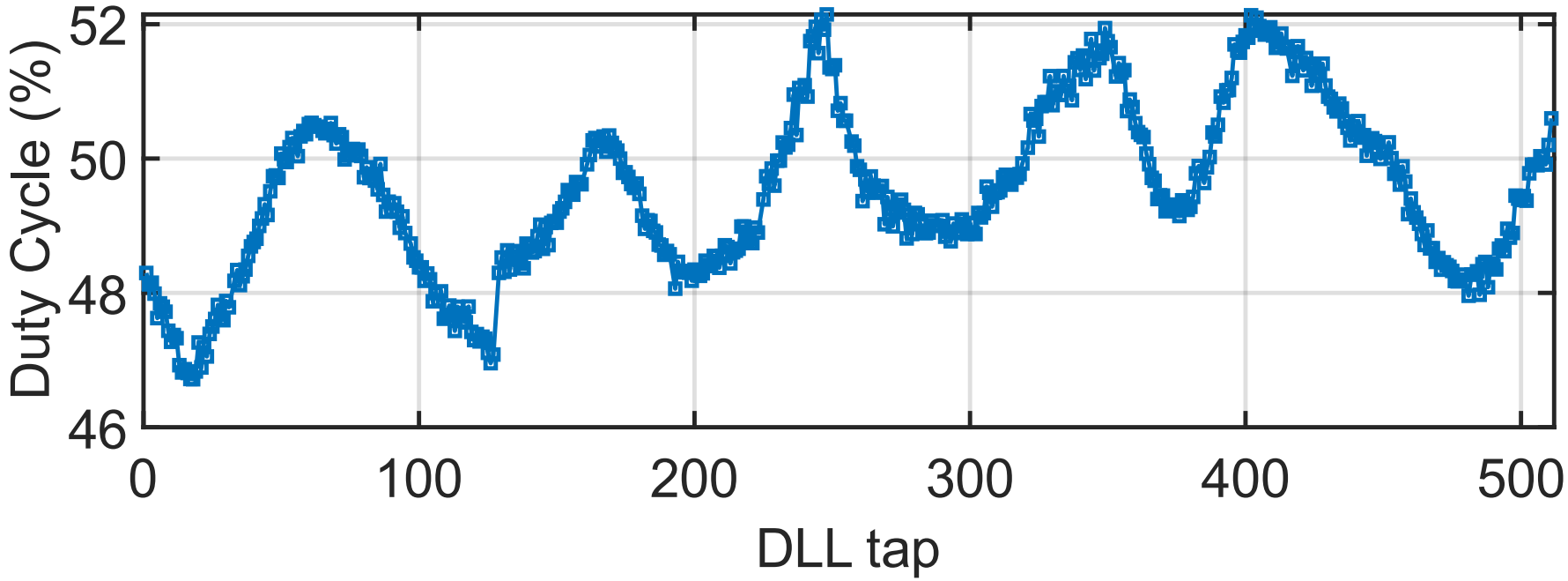
DLL Phase Skew vs. Freq

Phase skew only changes 0.12ns against 2ns STOP period change (20% frequency variation)

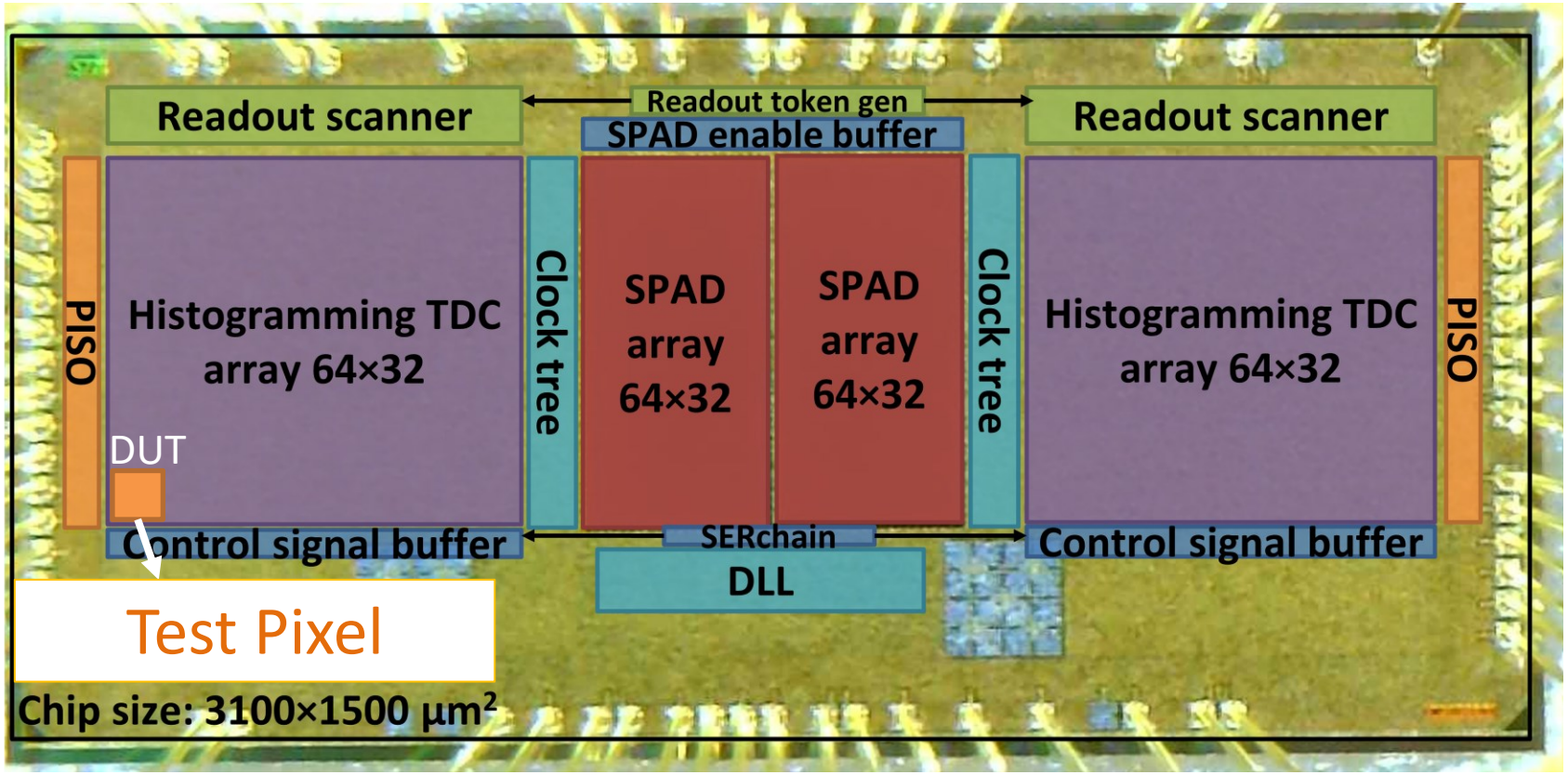


Duty cycle Full Sweep

Average duty cycle: 49.52%

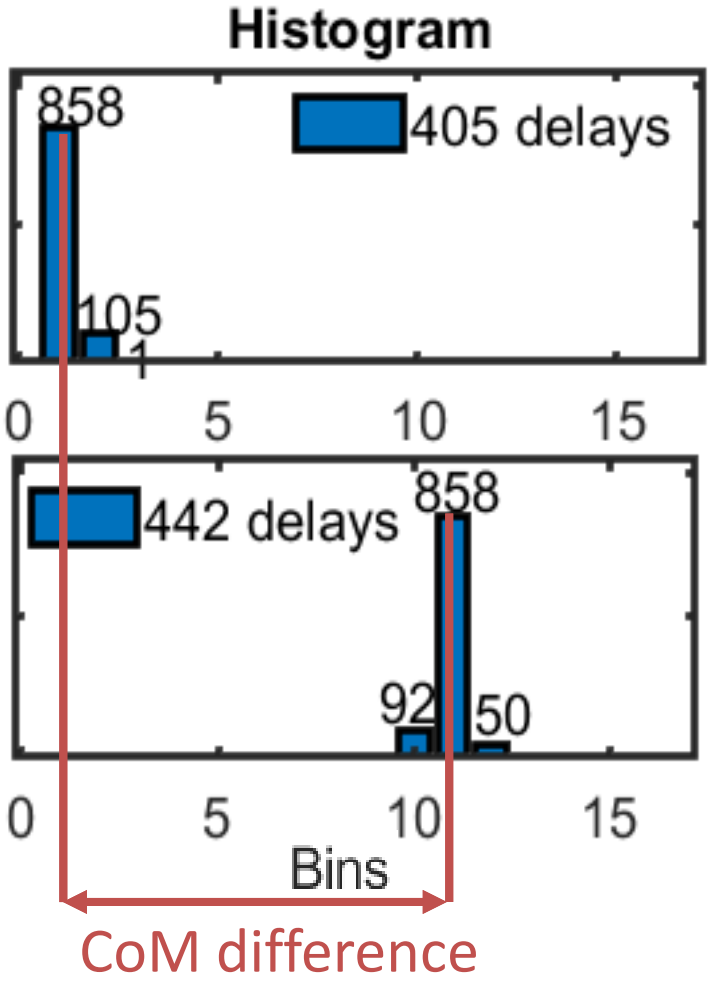


TDC Electrical Measurement



The SPAD_IN of the test TDC pixel is driven by an FPGA, allowing for a 15ps delay step.

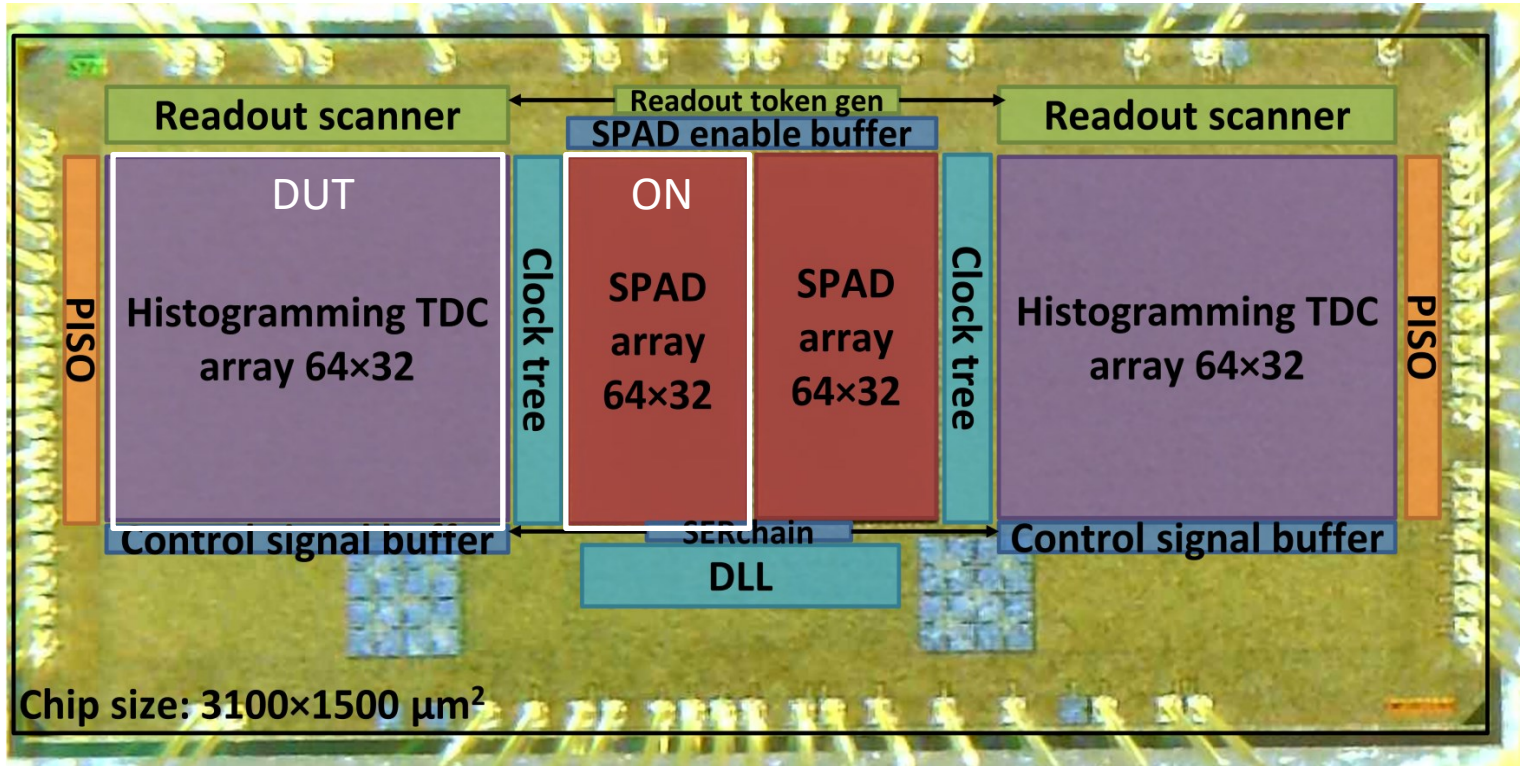
TDC Bin Size Electrical Measurement



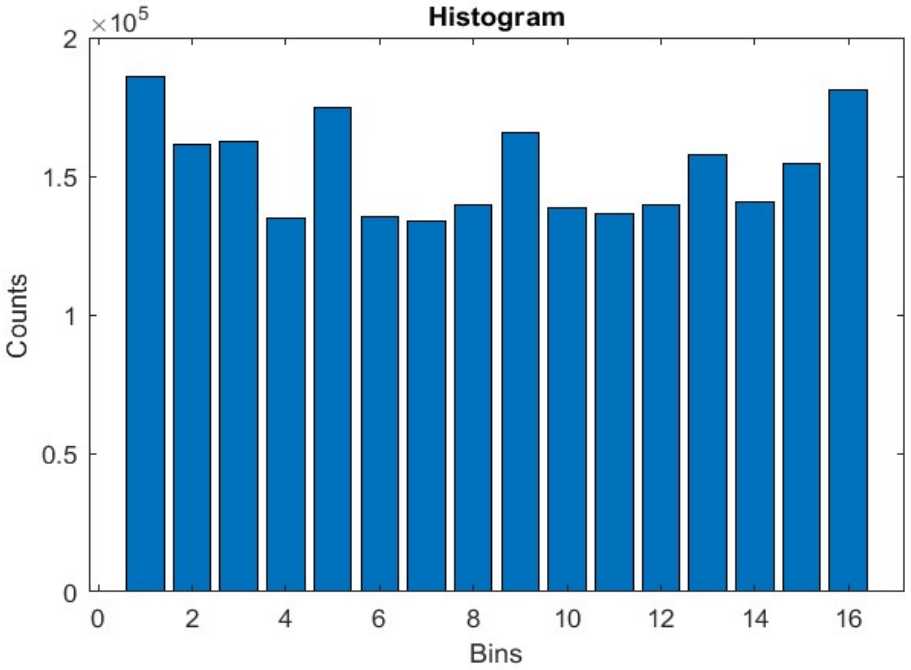
Estimated bin size = COM difference/delay difference

	TDC Range	VDD		
		0.97V	1V	1.03V
Closed-loop estimated bin size (ps)	Short	52.46	54.61	51.418
	Middle	110.02	110.13	110.15
	Long	140.68	140.58	140.51
Open-loop estimated bin size (ps)	Short	55.20	47.47	41.15
	Middle	110.57	105.90	99.20
	Long	147.99	140.37	127.57

TDC Code Density Test



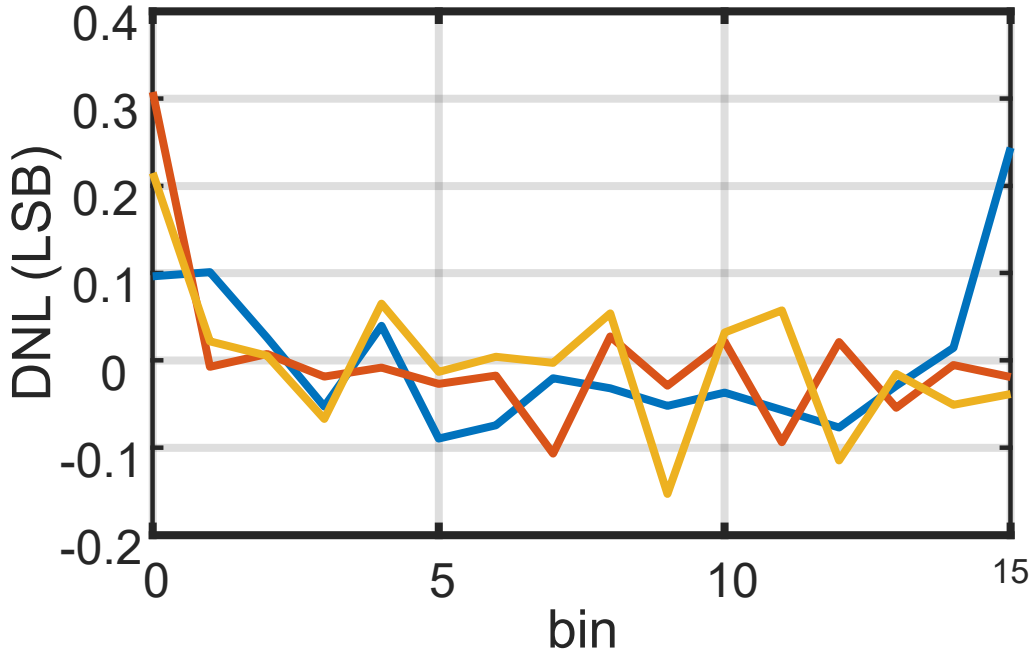
Uniform light source

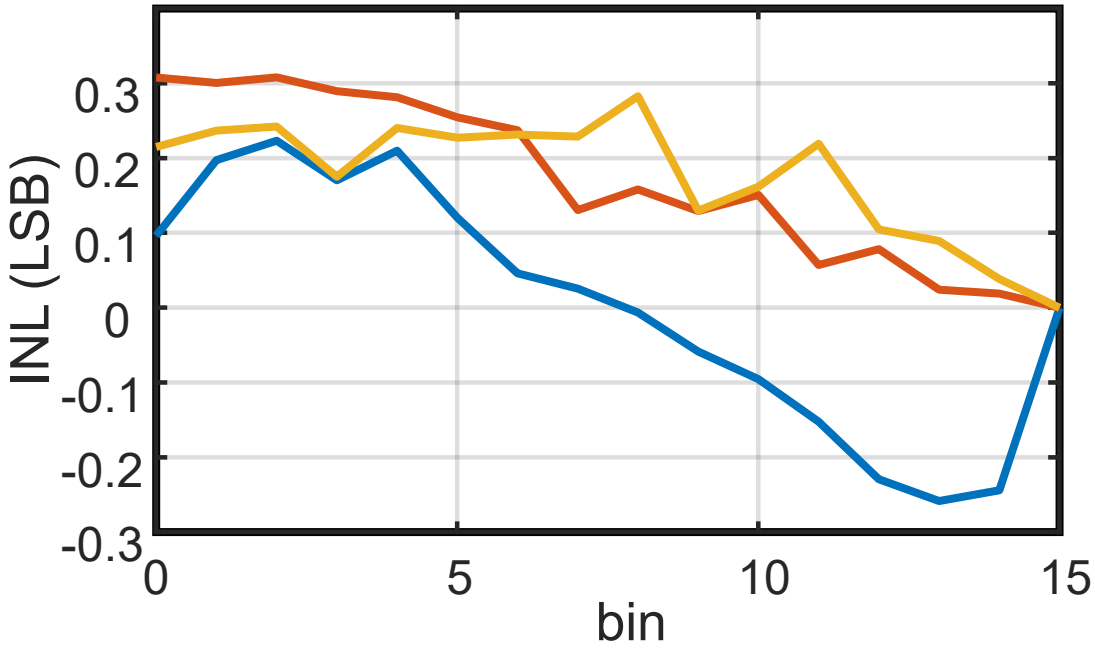


$$DNL(i) = \frac{counts\ in\ bin(i)/total\ counts}{1/number\ of\ bins} - 1$$

$$INL(i) = \sum_{1}^{i} DNL(i)$$

TDC Non-linearity





Range 0 (0.87ns)
Range 1 (1.76ns)
Range 2 (2.24ns)

	Range0	Range1	Range2
DNL(LSB)	+0.24/-0.09	+0.21/-0.15	+0.31/-0.11
INL(LSB)	+0.22/-0.26	+0.28/0	+0.31/0

Conclusions

- First body-biased TDC pixel in 28nm FDSOI
- A novel DLL solution for the negative body-biased voltage generation
- Demonstrates the body-biased TDC's robustness against voltage and frequency variations
- Requires optical IRF characterisation with SPAD, variation assessment across the TDC pixel array

Performance Summary Table			
Technology	28nm FDSOI		
Histogram bins	16*11b		
STOP frequency	100MHz		
Pixel size	12.02×29.87μm^2		
TDC resolution/ps	54.6	110.1	140.5
TDC range / ns	0.87	1.76	2.24
TDC DNL / LSB	+0.24/-0.09	0.21/-0.15	+0.31/-0.11
TDC INL / LSB	+0.22/-0.26	+0.28/0	+0.31/0

Thank you