SONY

The Path of CMOS Image Sensor Technologies Introduced to the Market

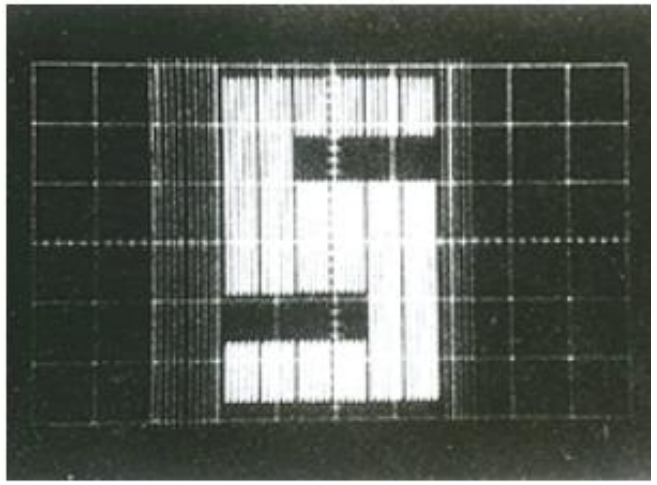
Tetsuo Nomoto

Sony Semiconductor Solutions

OUTLINE

1. CCD
2. CMOS Image Sensor Motivation
3. Evolution of Readout
4. Evolution of Pixel/Structure
5. Conclusion

CCD Exceeding Film Quality

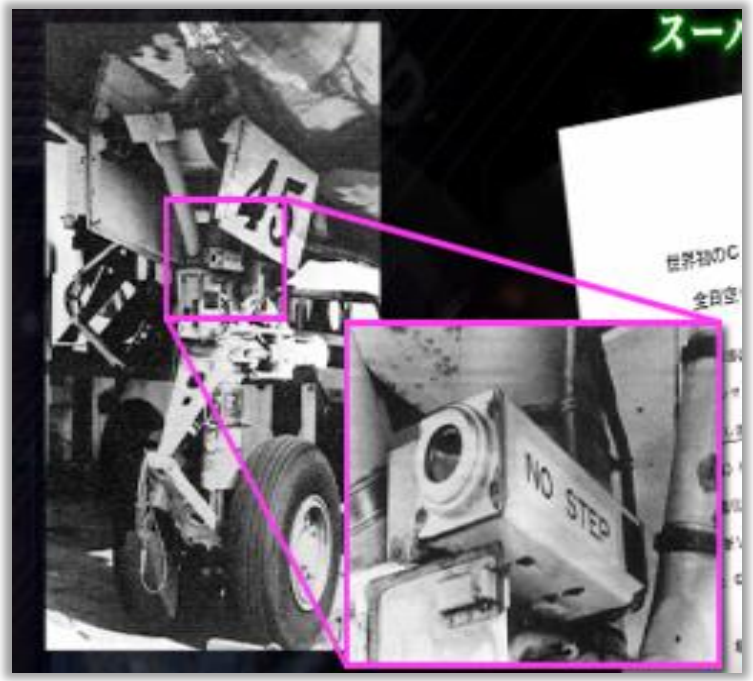


1969 AT&T Bell Lab.

1972 8x8

"We have to produce a camera using CCDs at a price under 50,000 yen within five years. We're not competing against other electronics manufacturers in this field. Our competition is Eastman Kodak."

CCD First Application



1980 Jumbo Jet camera

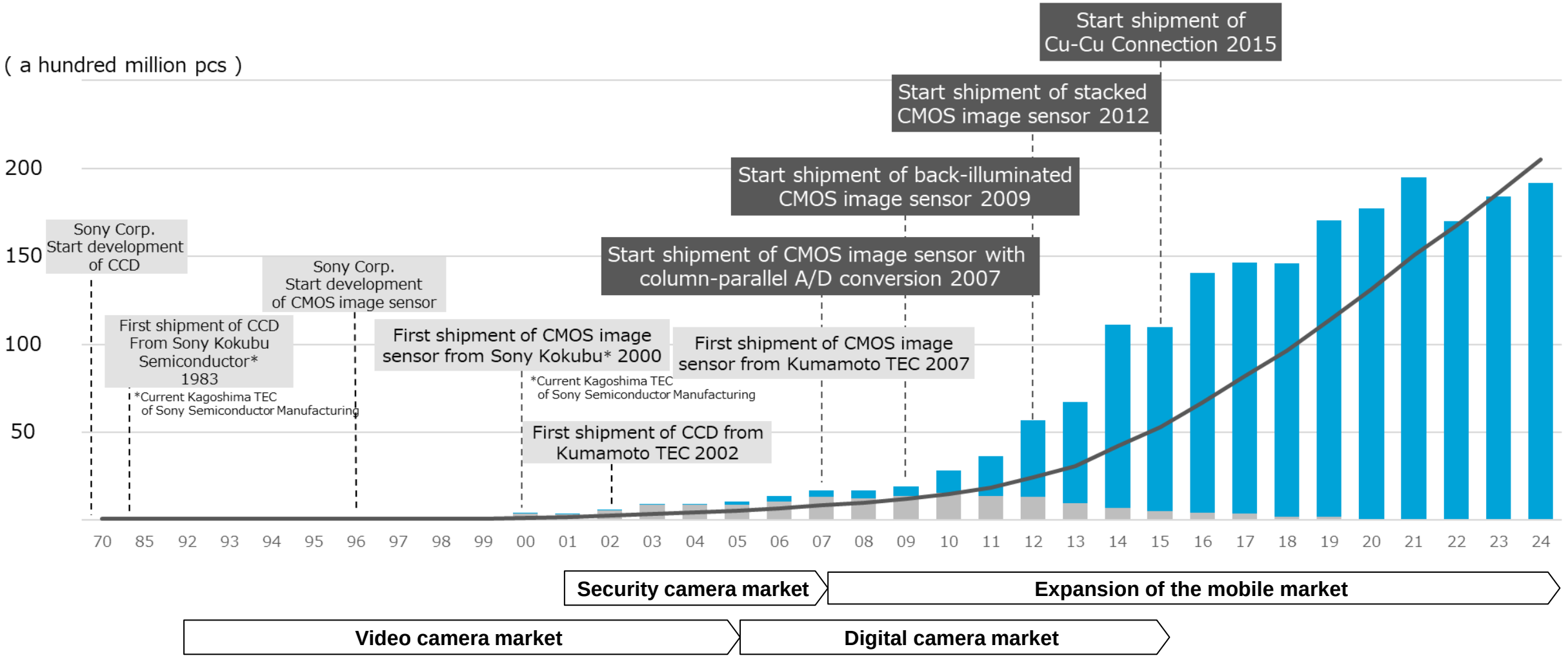
Small form factor
Vibration tolerance
No heat-up required

Sony Semiconductor Solutions Group's image sensor's shipment trends

Accumulated shipment(line graph) : left axis
Single-year shipment(bar graph) : right axis
＊Single-year shipment qty is not disclosed.

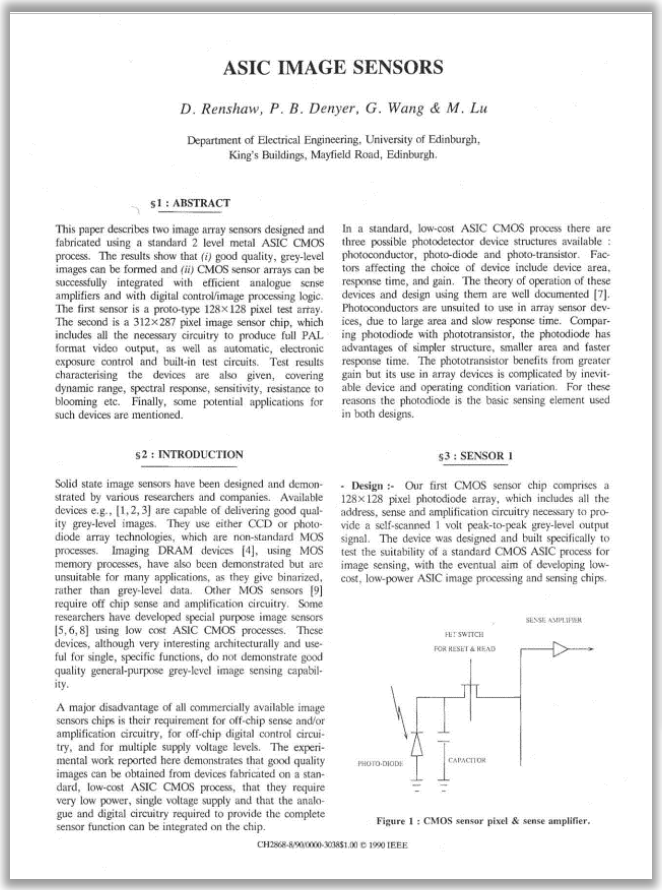
Increase in demand for CMOS image sensors due to mobile market growth

Cumulative shipments reached 20 bln pcs as of Dec. 2024



Motivation

CMOS Image Sensor



ASIC IMAGE SENSORS

D. Renshaw, P. B. Denyer, G. Wang & M. Lu

Department of Electrical Engineering, University of Edinburgh, King's Buildings, Mayfield Road, Edinburgh.

§1 : ABSTRACT

This paper describes two image array sensors designed and fabricated using a standard 2 level metal ASIC CMOS process. The results show that *(i)* good quality, grey-level images can be formed and *(ii)* CMOS sensor arrays can be successfully integrated with efficient analogue sense amplifiers and with digital control/image processing logic. The first sensor is a proto-type 128×128 pixel test array. The second is a 312×287 pixel image sensor chip, which includes all the necessary circuitry to produce full PAL format video output, as well as automatic, electronic exposure control and built-in test circuits. Test results characterising the devices are also given, covering dynamic range, spectral response, sensitivity, resistance to blooming etc. Finally, some potential applications for such devices are mentioned.

§2 : INTRODUCTION

Solid state image sensors have been designed and demonstrated by various researchers and companies. Available devices e.g., [1, 2, 3] are capable of delivering good quality grey-level images. They use either CCD or photodiode array technologies, which are non-standard MOS processes. Imaging DRAM devices [4], using MOS memory processes, have also been demonstrated but are unsuitable for many applications, as they give binarized, rather than grey-level data. Other MOS sensors [9] require off chip sense and amplification circuitry. Some researchers have developed special purpose image sensors [5, 6, 8] using low cost ASIC CMOS processes. These devices, although very interesting architecturally and useful for single, specific functions, do not demonstrate good quality general-purpose grey-level image sensing capability.

A major disadvantage of all commercially available image sensors chips is their requirement for off-chip sense and/or amplification circuitry, for off-chip digital control circuitry, and for multiple supply voltage levels. The experimental work reported here demonstrates that good quality images can be obtained from devices fabricated on a standard, low-cost ASIC CMOS process, that they require very low power, single voltage supply and that the analogue and digital circuitry required to provide the complete sensor function can be integrated on the chip.

In a standard, low-cost ASIC CMOS process there are three possible photodetector device structures available : photoconductor, photo-diode and photo-transistor. Factors affecting the choice of device include device area, response time, and gain. The theory of operation of these devices and design using them are well documented [7]. Photoconductors are unsuited to use in array sensor devices, due to large area and slow response time. Comparing photodiode with phototransistor, the photodiode has advantages of simpler structure, smaller area and faster response time. The phototransistor benefits from greater gain but its use in array devices is complicated by inevitable device and operating condition variation. For these reasons the photodiode is the basic sensing element used in both designs.

§3 : SENSOR 1

- **Design :-** Our first CMOS sensor chip comprises a 128×128 pixel photodiode array, which includes all the address, sense and amplification circuitry necessary to provide a self-scanned 1 volt peak-to-peak grey-level output signal. The device was designed and built specifically to test the suitability of a standard CMOS ASIC process for image sensing, with the eventual aim of developing low-cost, low-power ASIC image processing and sensing chips.

Figure 1 : CMOS sensor pixel & sense amplifier.

CH2868-8/90/0000-3038$1.00 © 1990 IEEE

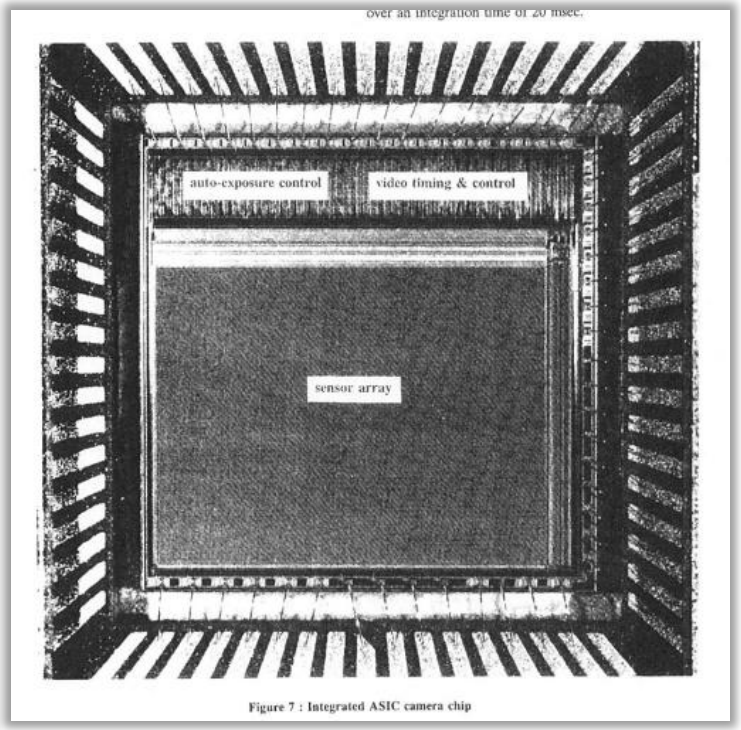
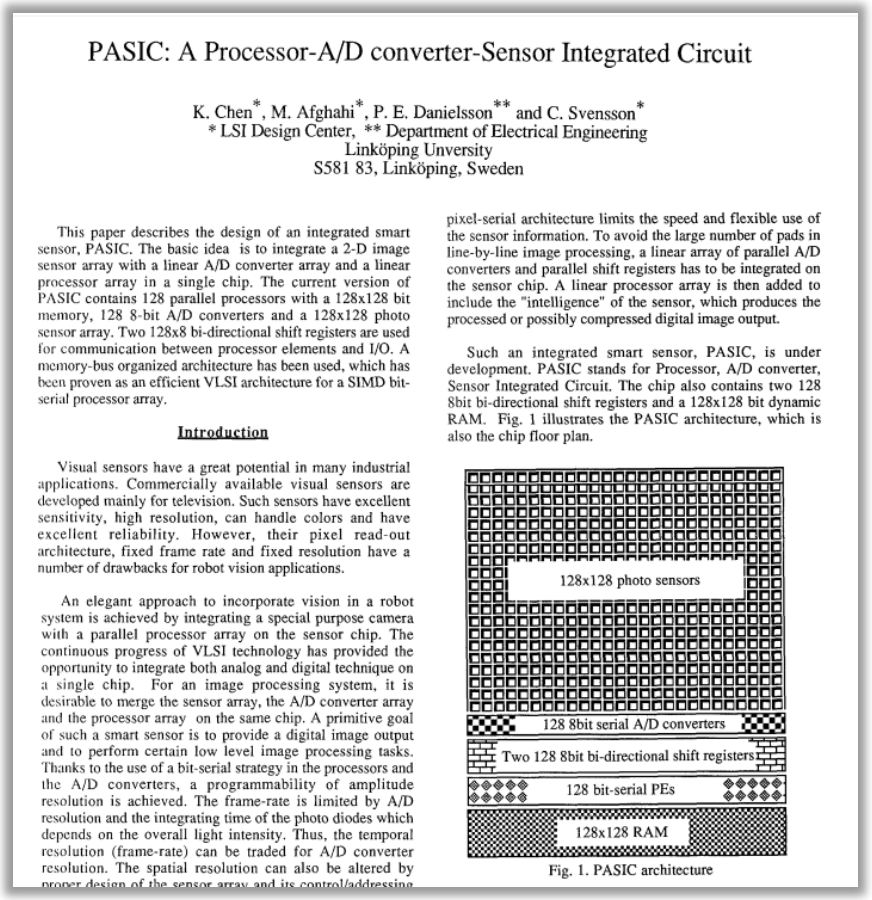


Figure 7 : Integrated ASIC camera chip



PASIC: A Processor-A/D converter-Sensor Integrated Circuit

K. Chen*, M. Afghahi*, P. E. Danielsson** and C. Svensson*
* LSI Design Center, ** Department of Electrical Engineering
Linköping Unversity
S581 83, Linköping, Sweden

This paper describes the design of an integrated smart sensor, PASIC. The basic idea is to integrate a 2-D image sensor array with a linear A/D converter array and a linear processor array in a single chip. The current version of PASIC contains 128 parallel processors with a 128x128 bit memory, 128 8-bit A/D converters and a 128x128 photo sensor array. Two 128x8 bi-directional shift registers are used for communication between processor elements and I/O. A memory-bus organized architecture has been used, which has been proven as an efficient VLSI architecture for a SIMD bit-serial processor array.

Introduction

Visual sensors have a great potential in many industrial applications. Commercially available visual sensors are developed mainly for television. Such sensors have excellent sensitivity, high resolution, can handle colors and have excellent reliability. However, their pixel read-out architecture, fixed frame rate and fixed resolution have a number of drawbacks for robot vision applications.

An elegant approach to incorporate vision in a robot system is achieved by integrating a special purpose camera with a parallel processor array on the sensor chip. The continuous progress of VLSI technology has provided the opportunity to integrate both analog and digital technique on a single chip. For an image processing system, it is desirable to merge the sensor array, the A/D converter array and the processor array on the same chip. A primitive goal of such a smart sensor is to provide a digital image output and to perform certain low level image processing tasks. Thanks to the use of a bit-serial strategy in the processors and the A/D converters, a programmability of amplitude resolution is achieved. The frame-rate is limited by A/D resolution and the integrating time of the photo diodes which depends on the overall light intensity. Thus, the temporal resolution (frame-rate) can be traded for A/D converter resolution. The spatial resolution can also be altered by proper design of the sensor array and its control/addressing

pixel-serial architecture limits the speed and flexible use of the sensor information. To avoid the large number of pads in line-by-line image processing, a linear array of parallel A/D converters and parallel shift registers has to be integrated on the sensor chip. A linear processor array is then added to include the "intelligence" of the sensor, which produces the processed or possibly compressed digital image output.

Such an integrated smart sensor, PASIC, is under development. PASIC stands for Processor, A/D converter, Sensor Integrated Circuit. The chip also contains two 128 8bit bi-directional shift registers and a 128x128 bit dynamic RAM. Fig. 1 illustrates the PASIC architecture, which is also the chip floor plan.

Fig. 1. PASIC architecture

D. Renshaw, *et al*., "ASIC image sensors," Proc. IEEE Proc. ISCA, pp.3038-3041, 1990

K. Chen, *et al*., "PASIC: A Processor-A/D converter-Sensor Integrated Circuit," Proc. IEEE ISCAS, 3, pp. 1705-1708, 1990

Motivation

Active Pixel Sensor

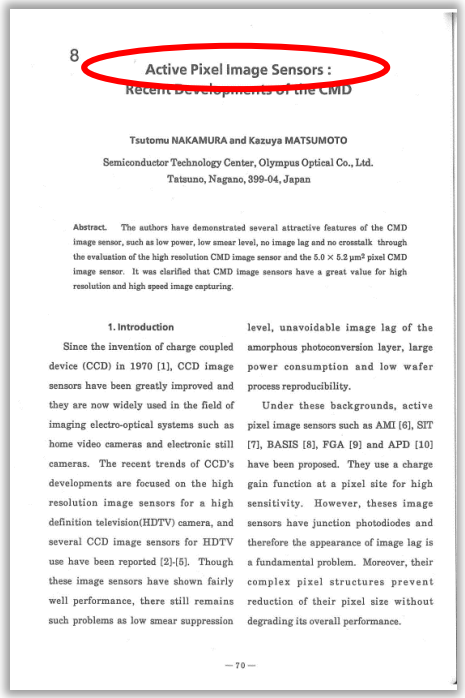
TECHNICAL DIGEST

SAIT' 91

INTERNATIONAL SYMPOSIUM
ON
ADVANCED IMAGE-ACQUISITION TECHNOLOGY

Cosponsored by
IIEEJ-The Institute of Image Electronic Engineers of Japan
ITE-The Institute of Television Engineers of Japan

12-13 November 1991
Kōgakuin-university, Shinjyuku Campus
Tokyo, Japan



8

Active Pixel Image Sensors :
Recent Developments of the CMD

Tsutomu NAKAMURA and Kazuya MATSUMOTO

Semiconductor Technology Center, Olympus Optical Co., Ltd.
Tatsuno, Nagano, 399-04, Japan

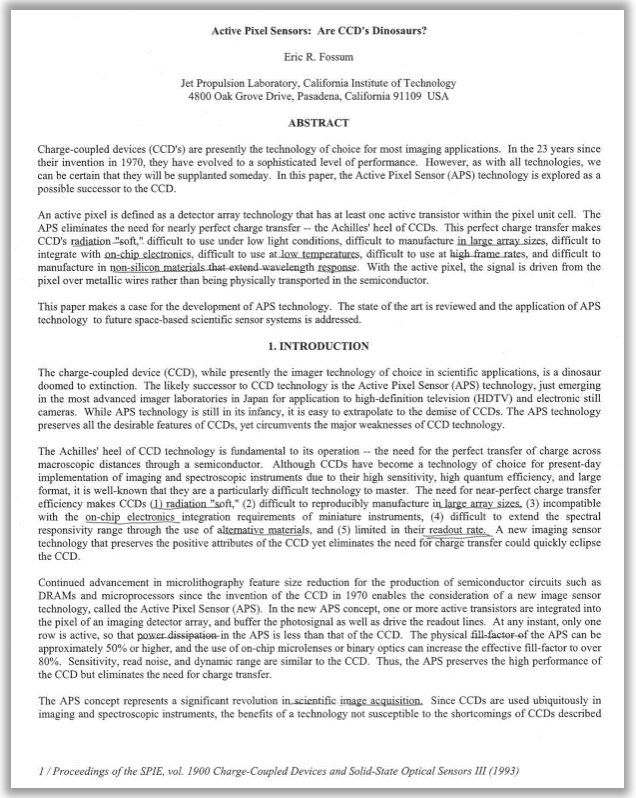
Abstract. The authors have demonstrated several attractive features of the CMD image sensor, such as low power, low smear level, no image lag and no crosstalk through the evaluation of the high resolution CMD image sensor and the 5.0 × 5.2 μm² pixel CMD image sensor. It was clarified that CMD image sensors have a great value for high resolution and high speed image capturing.

1. Introduction

Since the invention of charge coupled device (CCD) in 1970 [1], CCD image sensors have been greatly improved and they are now widely used in the field of imaging electro-optical systems such as home video cameras and electronic still cameras. The recent trends of CCD's developments are focused on the high resolution image sensors for a high definition television(HDTV) camera, and several CCD image sensors for HDTV use have been reported [2]-[5]. Though these image sensors have shown fairly well performance, there still remains such problems as low smear suppression level, unavoidable image lag of the amorphous photoconversion layer, large power consumption and low wafer process reproducibility.

Under these backgrounds, active pixel image sensors such as AMI [6], SIT [7], BASIS [8], FGA [9] and APD [10] have been proposed. They use a charge gain function at a pixel site for high sensitivity. However, theses image sensors have junction photodiodes and therefore the appearance of image lag is a fundamental problem. Moreover, their complex pixel structures prevent reduction of their pixel size without degrading its overall performance.

— 70 —



Active Pixel Sensors: Are CCD's Dinosaurs?

Eric R. Fossum

Jet Propulsion Laboratory, California Institute of Technology
4800 Oak Grove Drive, Pasadena, California 91109 USA

ABSTRACT

Charge-coupled devices (CCD's) are presently the technology of choice for most imaging applications. In the 23 years since their invention in 1970, they have evolved to a sophisticated level of performance. However, as with all technologies, we can be certain that they will be supplanted someday. In this paper, the Active Pixel Sensor (APS) technology is explored as a possible successor to the CCD.

An active pixel is defined as a detector array technology that has at least one active transistor within the pixel unit cell. The APS eliminates the need for nearly perfect charge transfer -- the Achilles' heel of CCDs. This perfect charge transfer makes CCD's radiation "soft," difficult to use under low light conditions, difficult to manufacture in large array sizes, difficult to integrate with on-chip electronics, difficult to use at low temperatures, difficult to use at high frame rates, and difficult to manufacture in non-silicon materials that extend wavelength response. With the active pixel, the signal is driven from the pixel over metallic wires rather than being physically transported in the semiconductor.

This paper makes a case for the development of APS technology. The state of the art is reviewed and the application of APS technology to future space-based scientific sensor systems is addressed.

1. INTRODUCTION

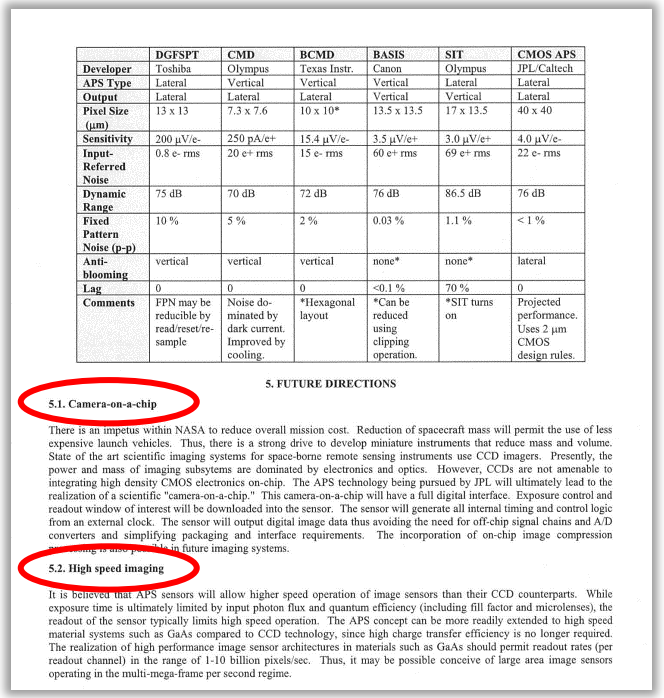
The charge-coupled device (CCD), while presently the imager technology of choice in scientific applications, is a dinosaur doomed to extinction. The likely successor to CCD technology is the Active Pixel Sensor (APS) technology, just emerging in the most advanced imager laboratories in Japan for application to high-definition television (HDTV) and electronic still cameras. While APS technology is still in its infancy, it is easy to extrapolate to the demise of CCDs. The APS technology preserves all the desirable features of CCDs, yet circumvents the major weaknesses of CCD technology.

The Achilles' heel of CCD technology is fundamental to its operation -- the need for the perfect transfer of charge across macroscopic distances through a semiconductor. Although CCDs have become a technology of choice for present-day implementation of imaging and spectroscopic instruments due to their high sensitivity, high quantum efficiency, and large format, it is well-known that they are a particularly difficult technology to master. The need for near-perfect charge transfer efficiency makes CCDs (1) radiation "soft," (2) difficult to reproducibly manufacture in large array sizes, (3) incompatible with the on-chip electronics integration requirements of miniature instruments, (4) difficult to extend the spectral responsivity range through the use of alternative materials, and (5) limited in their readout rate. A new imaging sensor technology that preserves the positive attributes of the CCD yet eliminates the need for charge transfer could quickly eclipse the CCD.

Continued advancement in microlithography feature size reduction for the production of semiconductor circuits such as DRAMs and microprocessors since the invention of the CCD in 1970 enables the consideration of a new image sensor technology, called the Active Pixel Sensor (APS). In the new APS concept, one or more active transistors are integrated into the pixel of an imaging detector array, and buffer the photosignal as well as drive the readout lines. At any instant, only one row is active, so that power dissipation in the APS is less than that of the CCD. The physical fill-factor of the APS can be approximately 50% or higher, and the use of on-chip microlenses or binary optics can increase the effective fill-factor to over 80%. Sensitivity, read noise, and dynamic range are similar to the CCD. Thus, the APS preserves the high performance of the CCD but eliminates the need for charge transfer.

The APS concept represents a significant revolution in scientific image acquisition. Since CCDs are used ubiquitously in imaging and spectroscopic instruments, the benefits of a technology not susceptible to the shortcomings of CCDs described

1 / Proceedings of the SPIE, vol. 1900 Charge-Coupled Devices and Solid-State Optical Sensors III (1993)



	DGFSPT	CMD	BCMD	BASIS	SIT	CMOS APS
Developer	Toshiba	Olympus	Texas Instr.	Canon	Olympus	JPL/Caltech
APS Type	Lateral	Vertical	Vertical	Vertical	Lateral	Lateral
Output	Lateral	Lateral	Lateral	Vertical	Vertical	Lateral
Pixel Size (μm)	13 x 13	7.3 x 7.6	10 x 10*	13.5 x 13.5	17 x 13.5	40 x 40
Sensitivity	200 μV/e-	250 pA/e+	15.4 μV/e-	3.5 μV/e+	3.0 μV/e+	4.0 μV/e-
Input-Referred Noise	0.8 e- rms	20 e+ rms	15 e- rms	60 e+ rms	69 e+ rms	22 e- rms
Dynamic Range	75 dB	70 dB	72 dB	76 dB	86.5 dB	76 dB
Fixed Pattern Noise (p-p)	10 %	5 %	2 %	0.03 %	1.1 %	< 1 %
Anti-blooming	vertical	vertical	vertical	none*	none*	lateral
Lag	0	0	0	<0.1 %	70 %	0
Comments	FPN may be reducible by read/reset/re-sample	Noise do-minated by dark current. Improved by cooling.	*Hexagonal layout	*Can be reduced using clipping operation.	*SIT turns on	Projected performance. Uses 2 μm CMOS design rules.

5. FUTURE DIRECTIONS

5.1. Camera-on-a-chip

There is an impetus within NASA to reduce overall mission cost. Reduction of spacecraft mass will permit the use of less expensive launch vehicles. Thus, there is a strong drive to develop miniature instruments that reduce mass and volume. State of the art scientific imaging systems for space-borne remote sensing instruments use CCD imagers. Presently, the power and mass of imaging subsystems are dominated by electronics and optics. However, CCDs are not amenable to integrating high density CMOS electronics on-chip. The APS technology being pursued by JPL will ultimately lead to the realization of a scientific "camera-on-a-chip." This camera-on-a-chip will have a full digital interface. Exposure control and readout window of interest will be downloaded into the sensor. The sensor will generate all internal timing and control logic from an external clock. The sensor will output digital image data thus avoiding the need for off-chip signal chains and A/D converters and simplifying packaging and interface requirements. The incorporation of on-chip image compression processing is also possible in future imaging systems.

5.2. High speed imaging

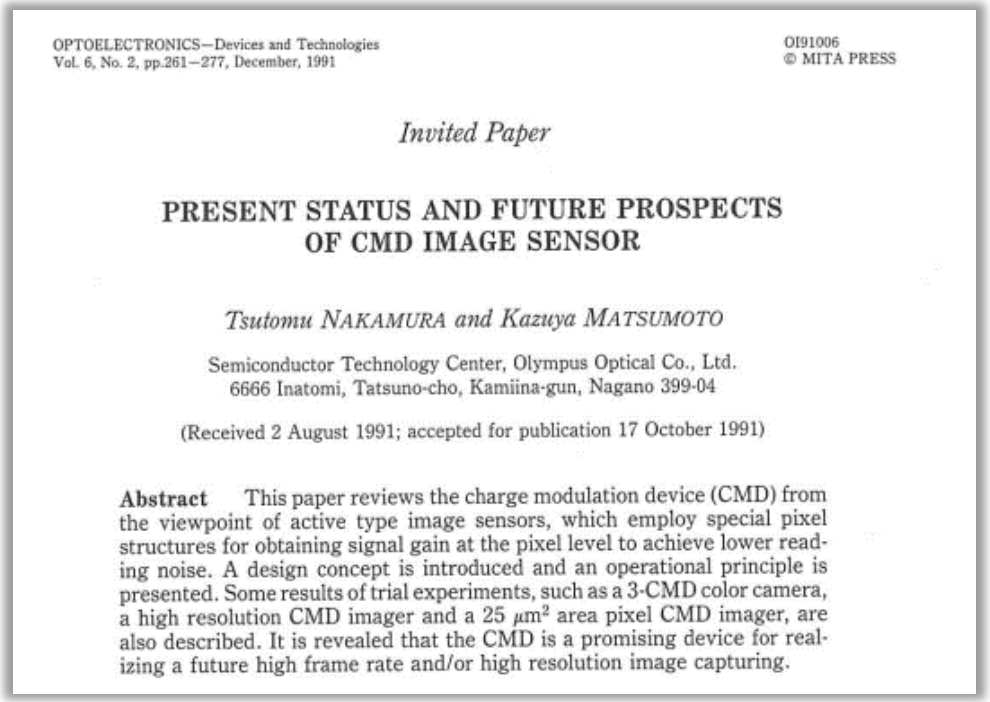
It is believed that APS sensors will allow higher speed operation of image sensors than their CCD counterparts. While exposure time is ultimately limited by input photon flux and quantum efficiency (including fill factor and microlenses), the readout of the sensor typically limits high speed operation. The APS concept can be more readily extended to high speed material systems such as GaAs compared to CCD technology, since high charge transfer efficiency is no longer required. The realization of high performance image sensor architectures in materials such as GaAs should permit readout rates (per readout channel) in the range of 1-10 billion pixels/sec. Thus, it may be possible conceive of large area image sensors operating in the multi-mega-frame per second regime.

T. Nakamura et al., "Active Pixel Image Sensors: Recent Development of the CMD", Tech Dig Int'l Symposium on Advanced Image-Acquisition Technology, pp.70-79, 1991

E. R. Fossum, "Active pixel sensors: Are CCD's Dinocaurs?," Proc. SPIE, Vol 1900, pp.2-14, 1993.

Motivation

Advantage against CCD



OPTOELECTRONICS—Devices and Technologies
Vol. 6, No. 2, pp.261–277, December, 1991

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Invited Paper

PRESENT STATUS AND FUTURE PROSPECTS OF CMD IMAGE SENSOR

Tsutomu NAKAMURA and Kazuya MATSUMOTO

Semiconductor Technology Center, Olympus Optical Co., Ltd.
6666 Inatomi, Tatsuno-cho, Kamiina-gun, Nagano 399-04

(Received 2 August 1991; accepted for publication 17 October 1991)

Abstract This paper reviews the charge modulation device (CMD) from the viewpoint of active type image sensors, which employ special pixel structures for obtaining signal gain at the pixel level to achieve lower reading noise. A design concept is introduced and an operational principle is presented. Some results of trial experiments, such as a 3-CMD color camera, a high resolution CMD imager and a 25 μm^2 area pixel CMD imager, are also described. It is revealed that the CMD is a promising device for realizing a future high frame rate and/or high resolution image capturing.

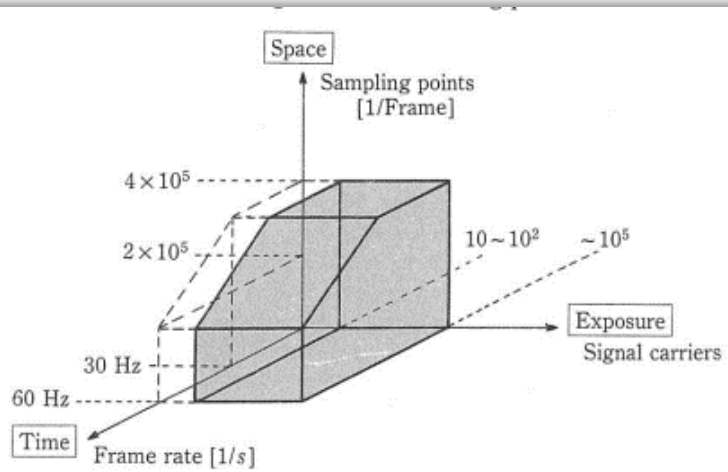
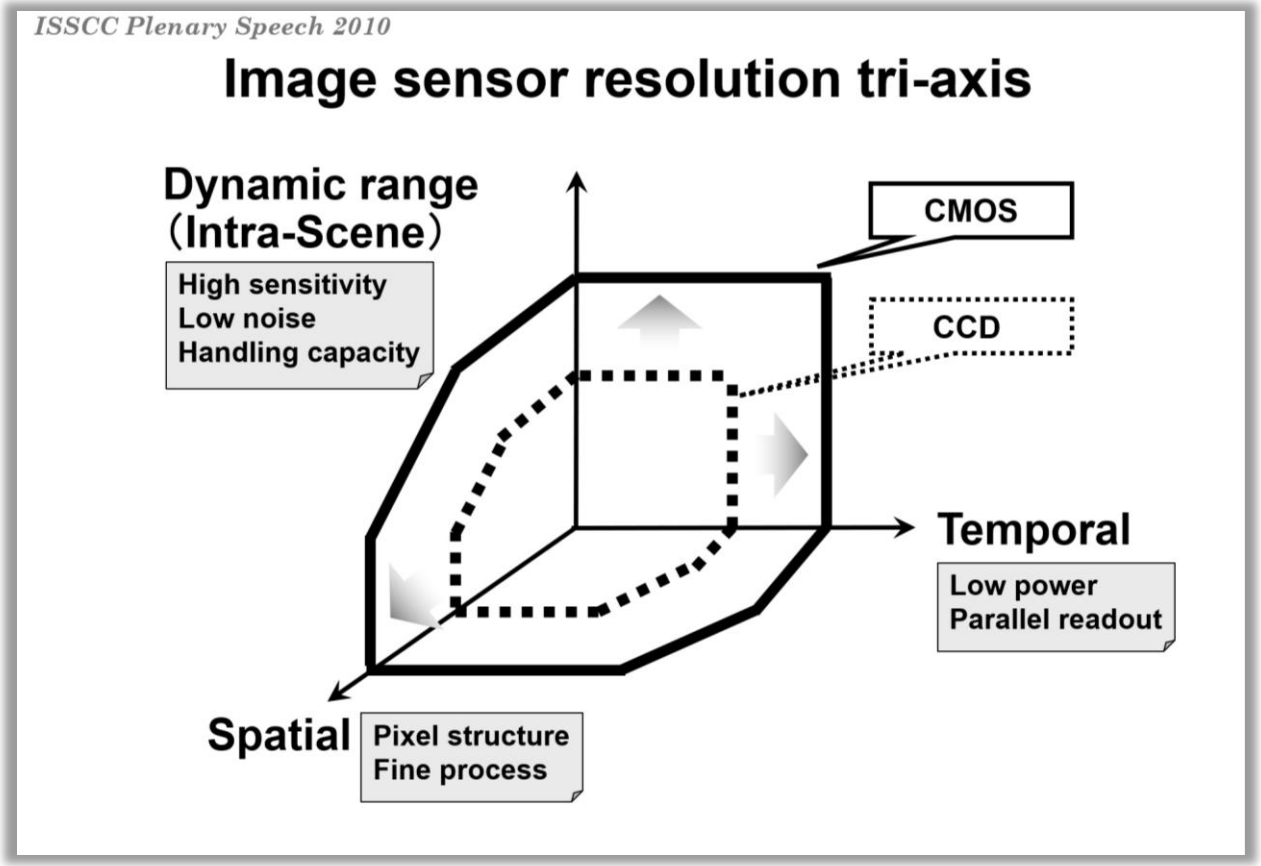


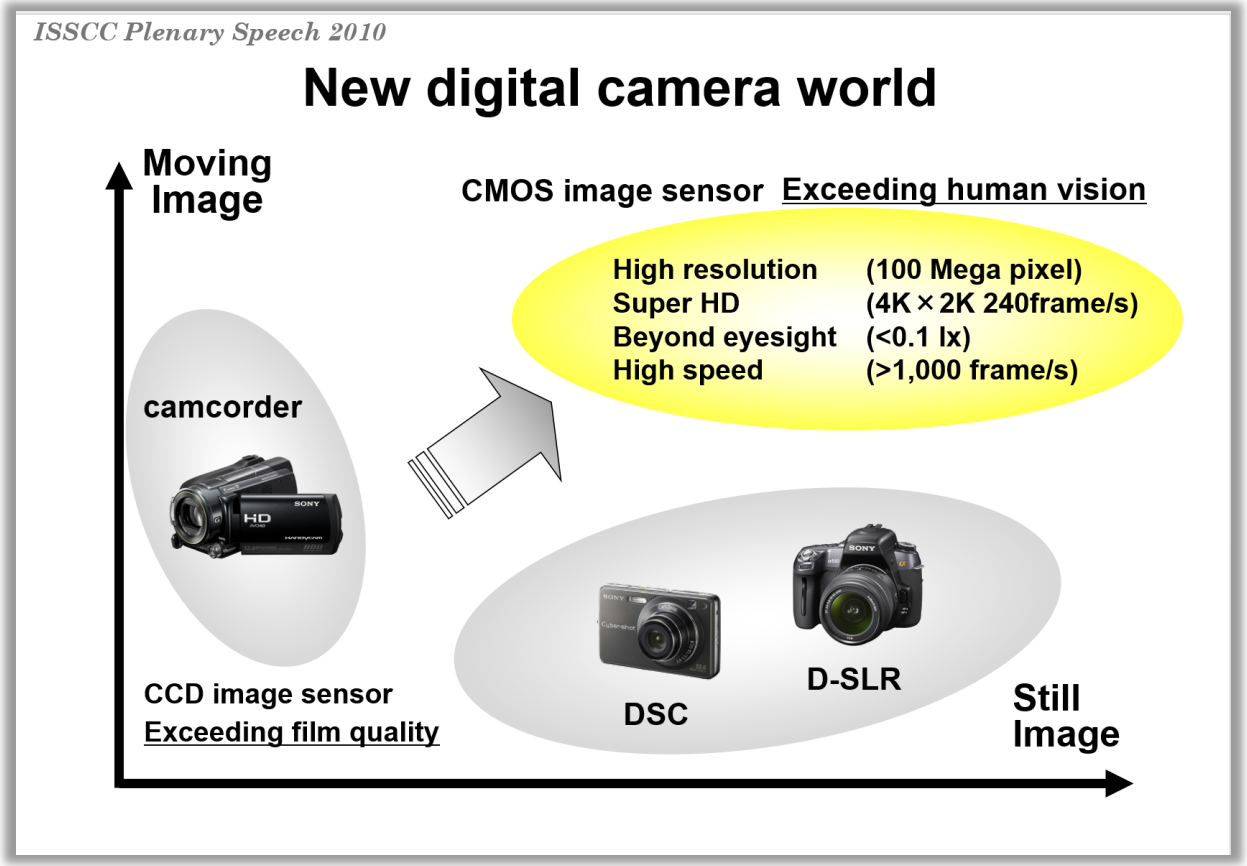
Fig. 1. The performance of conventional CCD imagers in three categories.

T. Nakamura et al., “Present Status and Future Prospects of CMD Image Sensor, OPTOELECTRONICS, pp.261-277, 1991

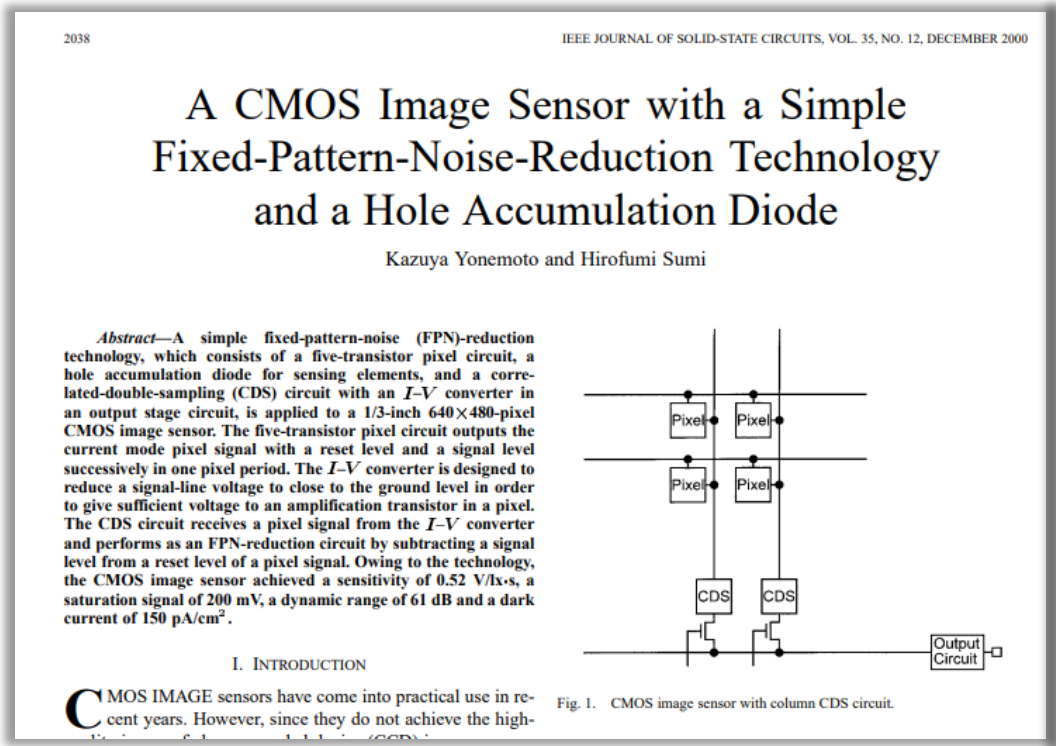
Motivation

Exceeding Human Vision





Readout DRSCAN



2038 IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 35, NO. 12, DECEMBER 2000

A CMOS Image Sensor with a Simple Fixed-Pattern-Noise-Reduction Technology and a Hole Accumulation Diode

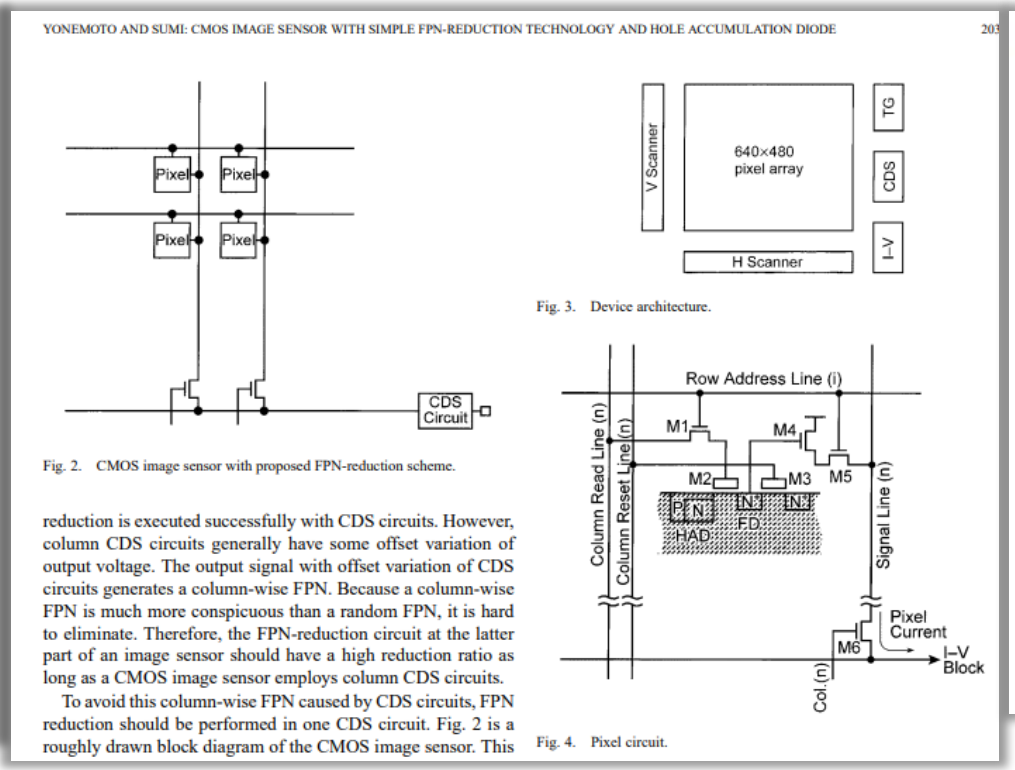
Kazuya Yonemoto and Hirofumi Sumi

Abstract—A simple fixed-pattern-noise (FPN)-reduction technology, which consists of a five-transistor pixel circuit, a hole accumulation diode for sensing elements, and a correlated-double-sampling (CDS) circuit with an I–V converter in an output stage circuit, is applied to a 1/3-inch 640×480-pixel CMOS image sensor. The five-transistor pixel circuit outputs the current mode pixel signal with a reset level and a signal level successively in one pixel period. The I–V converter is designed to reduce a signal-line voltage to close to the ground level in order to give sufficient voltage to an amplification transistor in a pixel. The CDS circuit receives a pixel signal from the I–V converter and performs as an FPN-reduction circuit by subtracting a signal level from a reset level of a pixel signal. Owing to the technology, the CMOS image sensor achieved a sensitivity of 0.52 V/lx·s, a saturation signal of 200 mV, a dynamic range of 61 dB and a dark current of 150 pA/cm^2.

I. Introduction

CMOS IMAGE sensors have come into practical use in recent years. However, since they do not achieve the high-

Fig. 1. CMOS image sensor with column CDS circuit.



YONEMOTO AND SUMI: CMOS IMAGE SENSOR WITH SIMPLE FPN-REDUCTION TECHNOLOGY AND HOLE ACCUMULATION DIODE 203

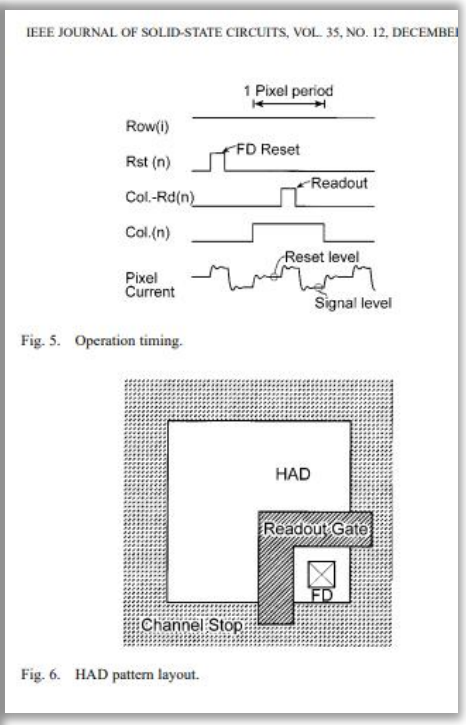
Fig. 2. CMOS image sensor with proposed FPN-reduction scheme.

reduction is executed successfully with CDS circuits. However, column CDS circuits generally have some offset variation of output voltage. The output signal with offset variation of CDS circuits generates a column-wise FPN. Because a column-wise FPN is much more conspicuous than a random FPN, it is hard to eliminate. Therefore, the FPN-reduction circuit at the latter part of an image sensor should have a high reduction ratio as long as a CMOS image sensor employs column CDS circuits.

To avoid this column-wise FPN caused by CDS circuits, FPN reduction should be performed in one CDS circuit. Fig. 2 is a roughly drawn block diagram of the CMOS image sensor. This

Fig. 3. Device architecture.

Fig. 4. Pixel circuit.



IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 35, NO. 12, DECEMBER

Fig. 5. Operation timing.

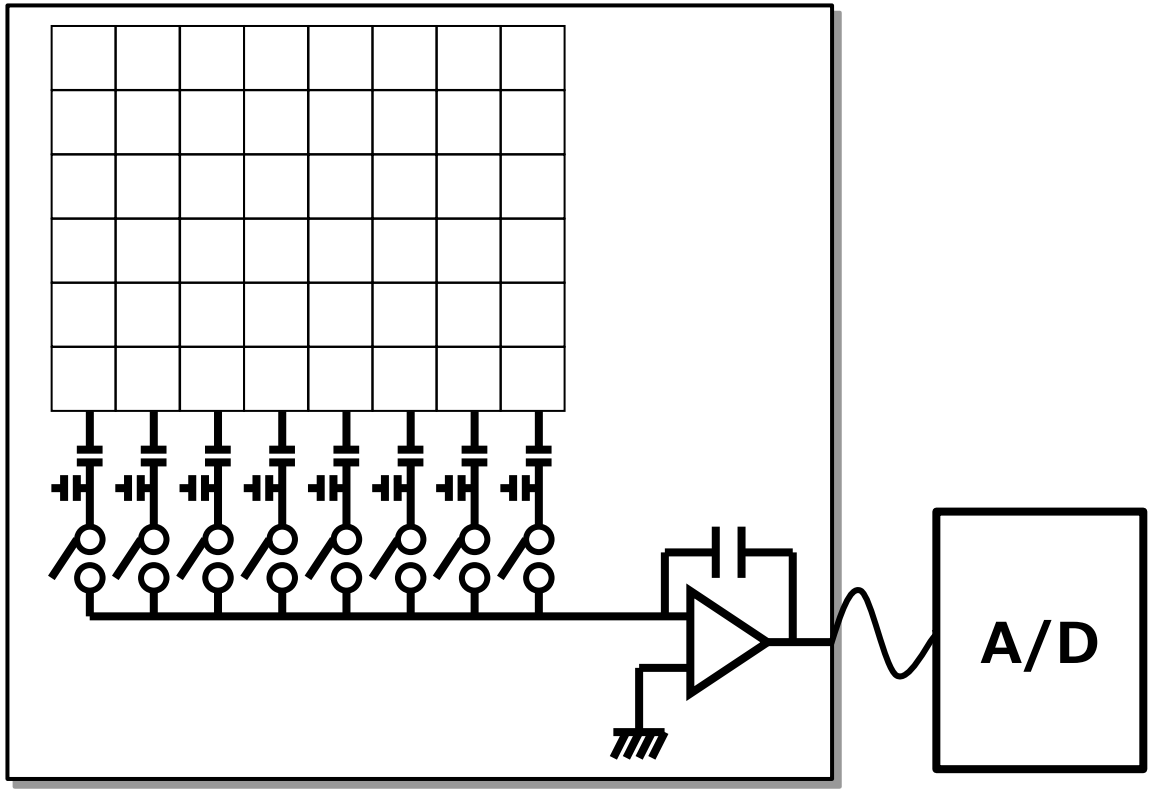
Fig. 6. HAD pattern layout.

K. Yonemoto *et al*., "A CMOS Image Sensor with a Simple Fixed-Pattern-Noise-Reduction Technology and a Hole Accumulation Diode," IEEE J. Solid-State Circuits, Vol. 35, No. 12, Dec. 2000.

DRSCAN: Dot sequential Readout System with Current Amplified signal output Noise reduction circuit

Robot, PDA, Cellular phone : 100k-300k pixel
5Tr Sequential readout : FPN free
Analog output : Utilize CCD-based camera system

Readout Column CDS

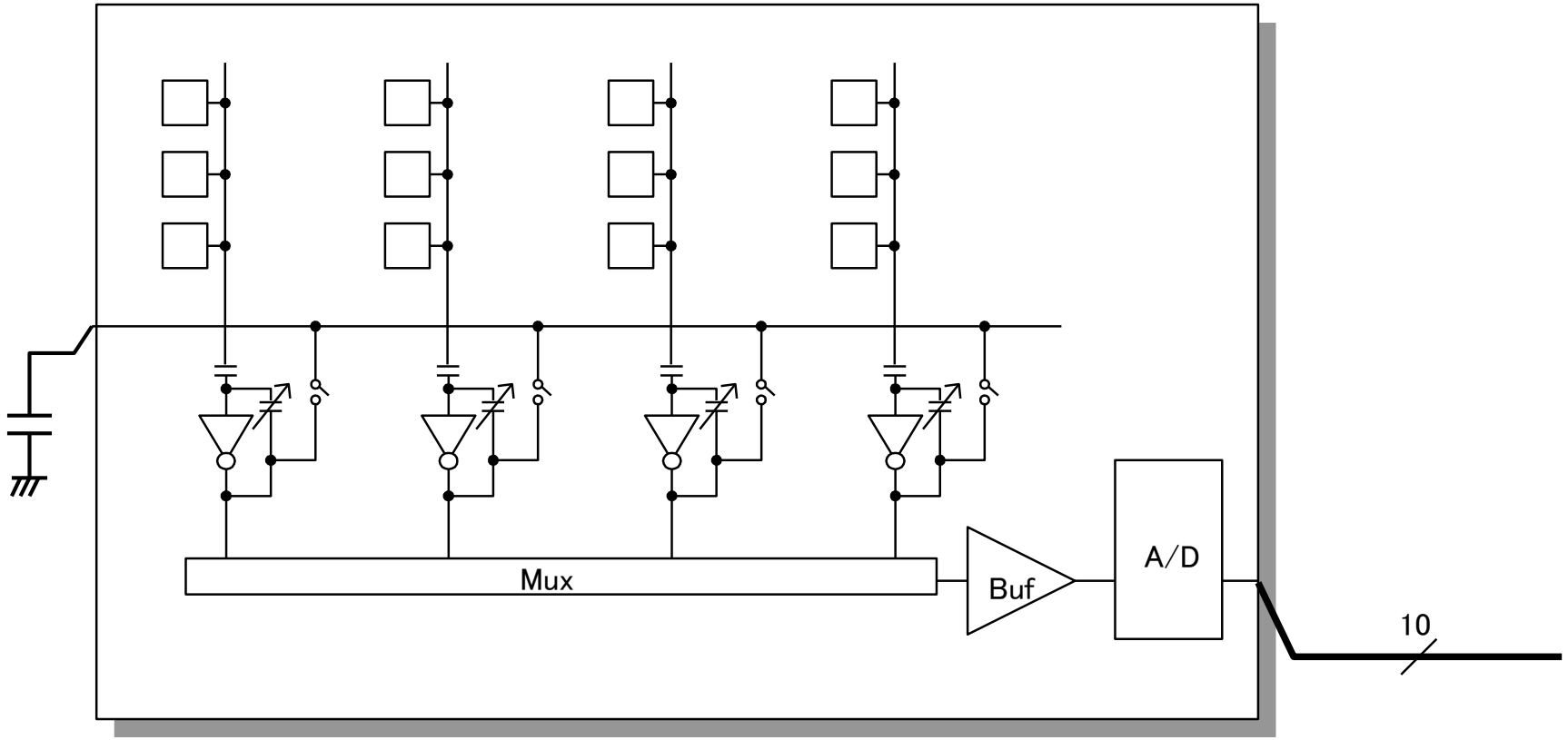


Camcorder : Low power & High-speed readout (parallel readout)
= Low heat generation to avoid Low-temperature burn

DSLR : Low power & High-speed readout = Large format

Analog output : Utilize CCD-based camera system

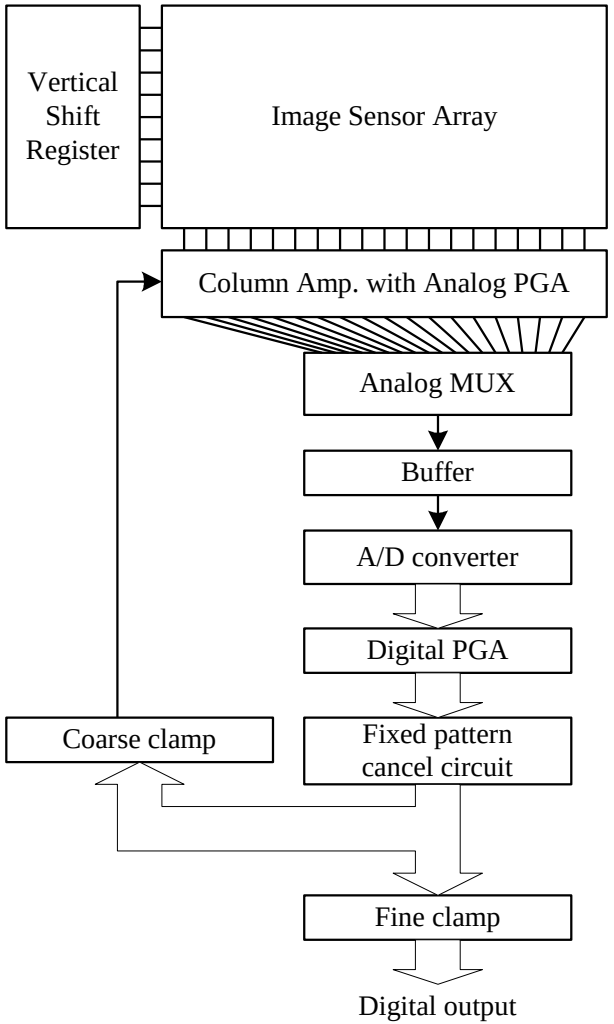
Readout Column QV



Mobile application
Compact camera system :

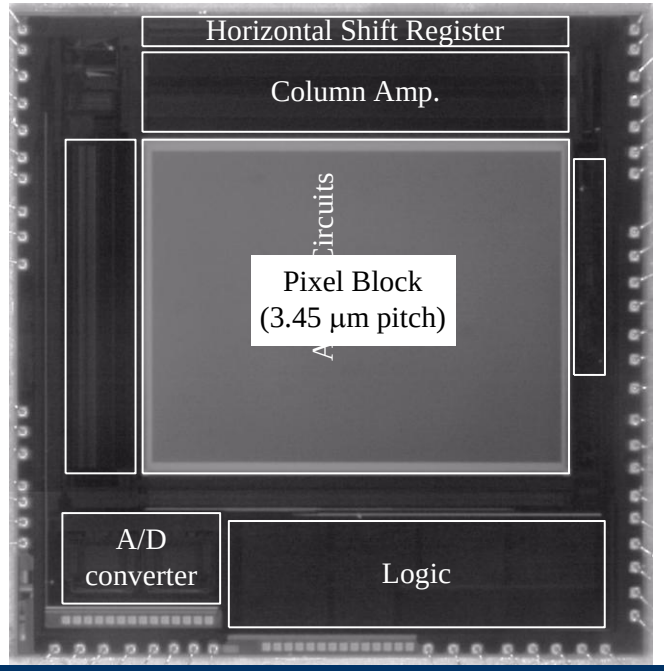
On-chip ADC
Digital Signal Processing

Readout Column QV FPN cancel



FPN +/- 6 LSB

FPN +/- 0.5 LSB

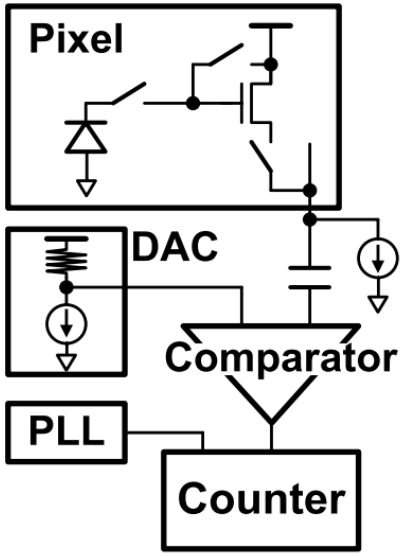


T. Haruta *et al*., "A 1/3.2 Type 1.28M pixel Low Power Consumption CMOS Image Sensor For Mobile Application," ITE Technical Report Vol. 28, No. 72, pp. 5-8, Nov. 2004.

Readout Column ADC Analog & Digital CDS

Column-Inline Dual CDS

- Operate Dual CDS in Analog & Digital Regions



Analog Operations
(1)Pixel Reset
(2)Comparator Reset
(3)Reset Readout
(4)Charge Transfer
(5)Signal Readout

Digital Operations
(1)Down Count
(2)Up Count

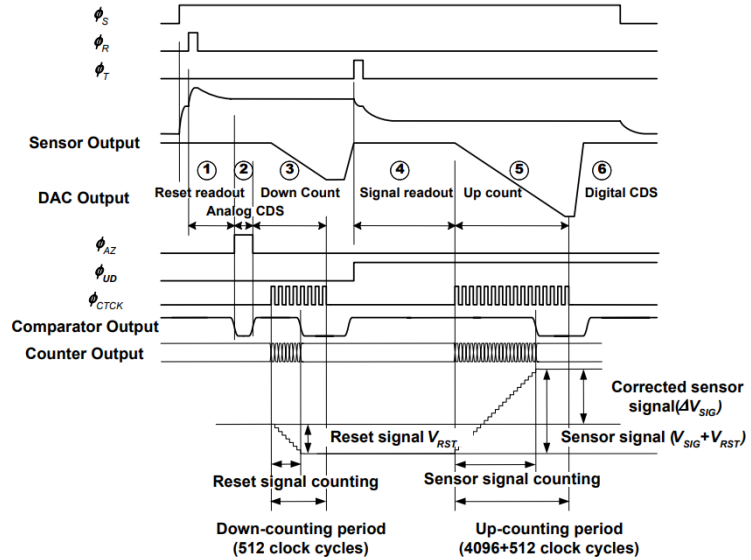


Figure 27.5.3: Timing diagram.

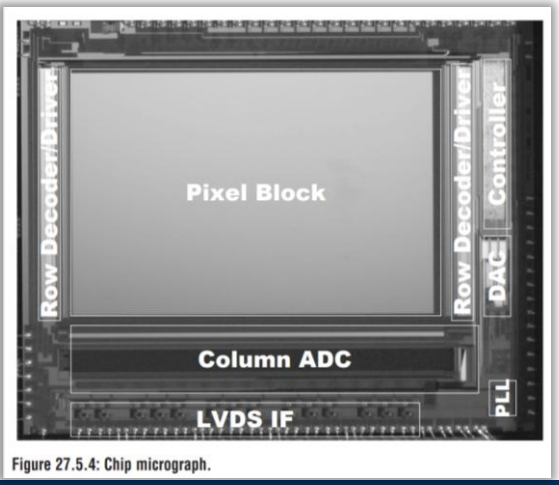


Figure 27.5.4: Chip micrograph.

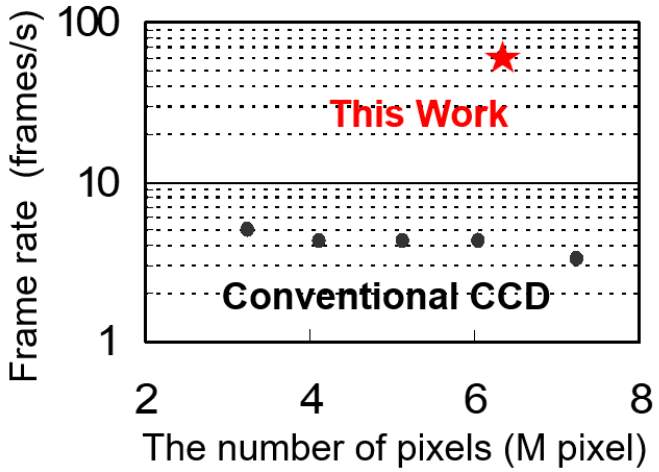
Y. Nitta *et al*., "High-speed digital double sampling with analog CDS on low-noise active pixel sensor," ISSCC Dig. Tech. Papers, pp500-502, 2006.

HD High Speed Camera

Small die size

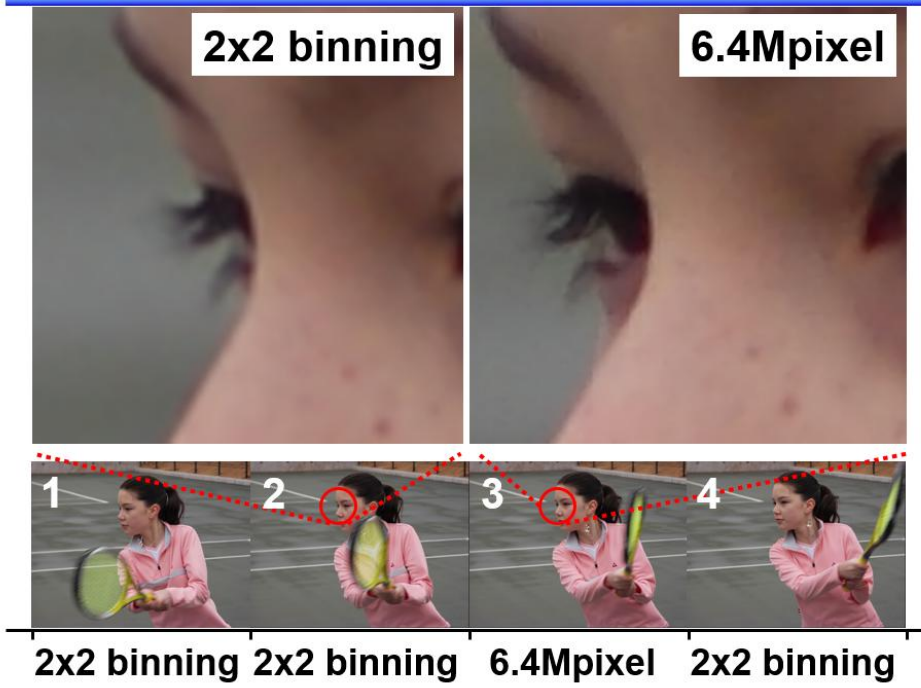
Readout Column ADC Hybrid Camera

Background



High-speed CMOS image sensor
for the coming new digital camera world

Reproduced Image
Seamless Mode Change



Y. Yoshihara *et al*., "A 1/1.8-inch 6.4Mpixel 60 frames/s CMOS image sensor with seamless mode change,"
IEEE J. Solid-State Circuits, Vol. 41, No. 12, pp. 2998-3006, 2006.

Hybrid Camera (Still and Movie)

Pixel Technology　Light pipe

Figure 5: Light Pipes (Sony), M

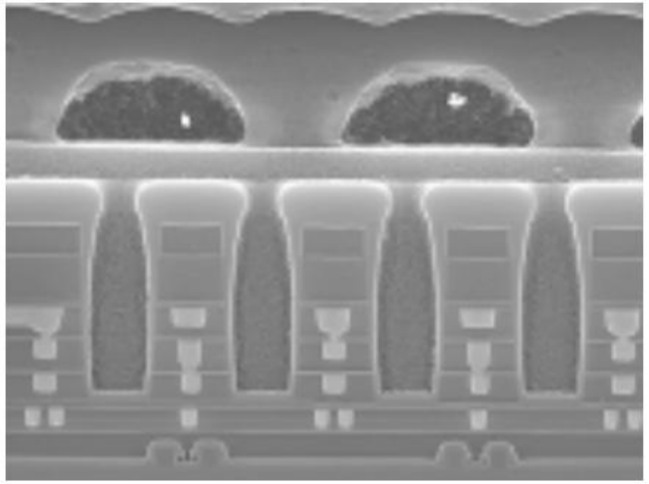


Figure 6: Sony 1.4 µm pixels (L

R. Fontaine, “Trends in Consumer CMOS Image Sensor Manufacturing,”
Proc. Int. Image Sensor Workshop, June 2009.

Mobile Application

Angular response

Cu wiring

Pixel Technology　Back Illuminated Sensor

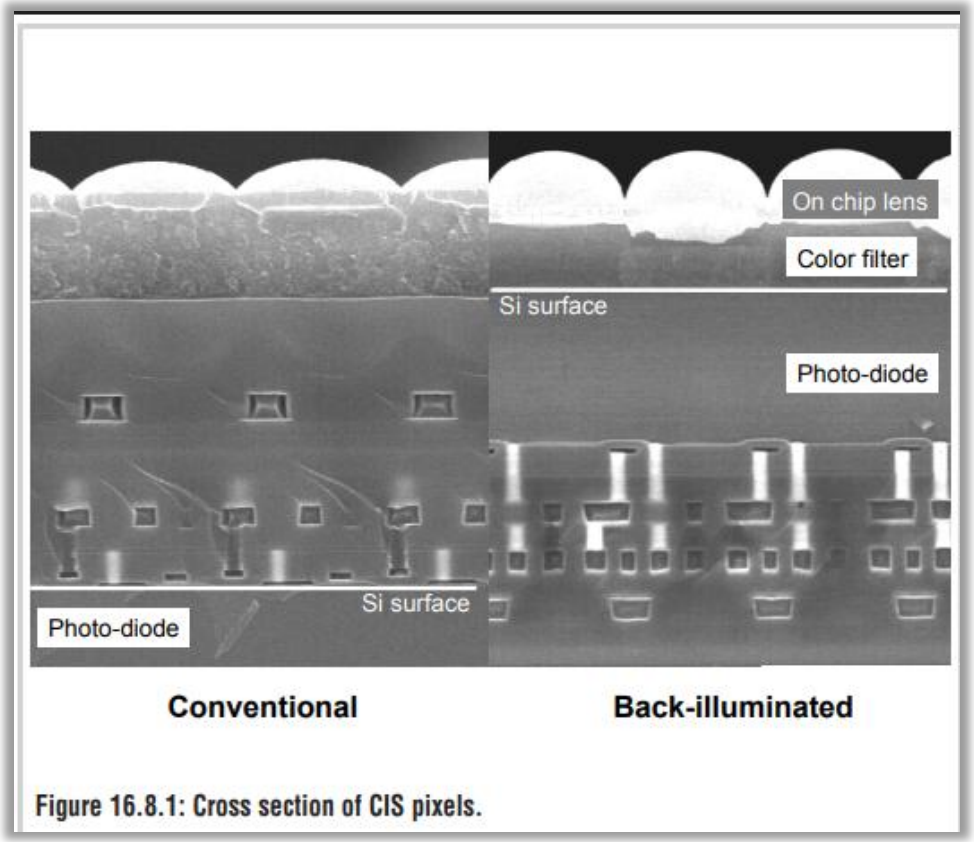
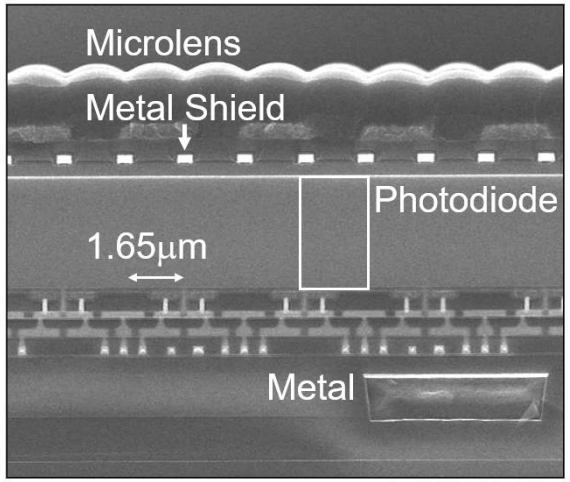


Figure 16.8.1: Cross section of CIS pixels.

S. Iwabuchi *et al*., "A Back-Illuminated High-Sensitivity Small-Pixel Color CMOS Image Sensor with Flexible Layout of Metal Wiring," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp. 302-303, Feb. 2006.

Pixel Cross-Section

Back-Illuminated Structure (0.14μm 1P 4Metal)



Key Process

Metal Shield
Microlens
Photodiode
Pixel Wiring

6

H. Wakabayashi *et al*., "A 1/2.3-inch 10.3Mpixel 50frams/s Back-Illuminated CMOS Image Sensor," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp. 410-412, Feb. 2010.

Camcorder : High Sensitivity
DSC : Small Pixel
Mobile : High Image Quality

Back Illuminated Sensor　First Product

2009年1月15日

新商品

HANDYCAM

世界初※1、裏面照射型CMOSセンサーを採用
約2倍※2の感度向上で暗所でもノイズの少ない高画質撮影が可能
AVCHD HDDデジタルハイビジョン“ハンディカム”2機種発売
－ 歩き撮りでもブレにくい新開発「光学式手ブレ補正※3」機能、世界初※1となるGPS機能搭載 －

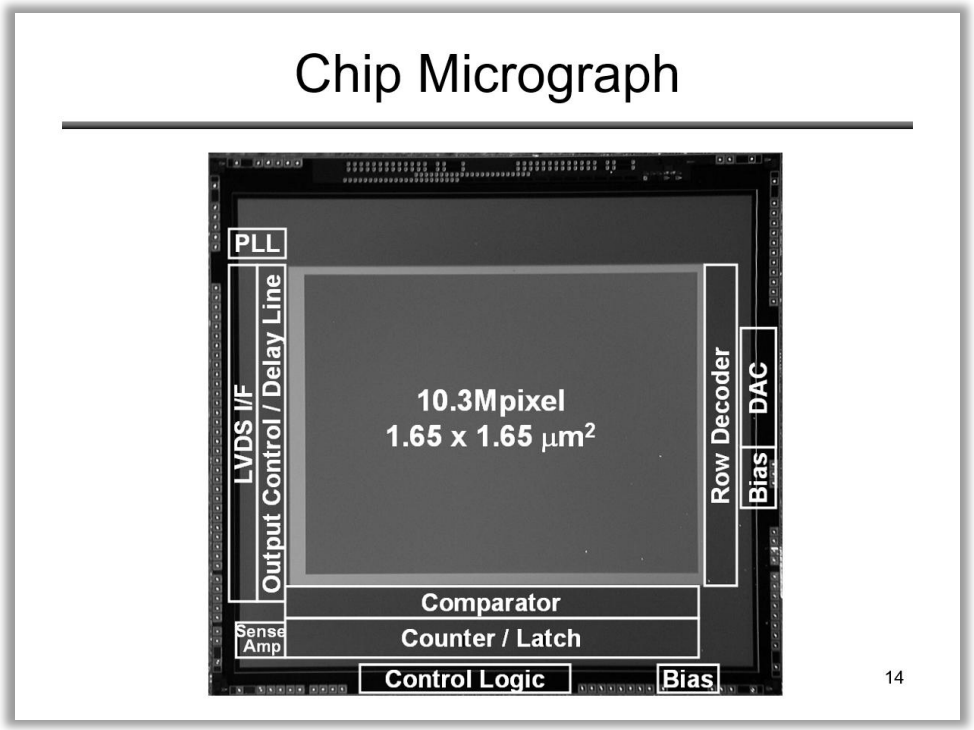
Exmor R CMOS Sensor

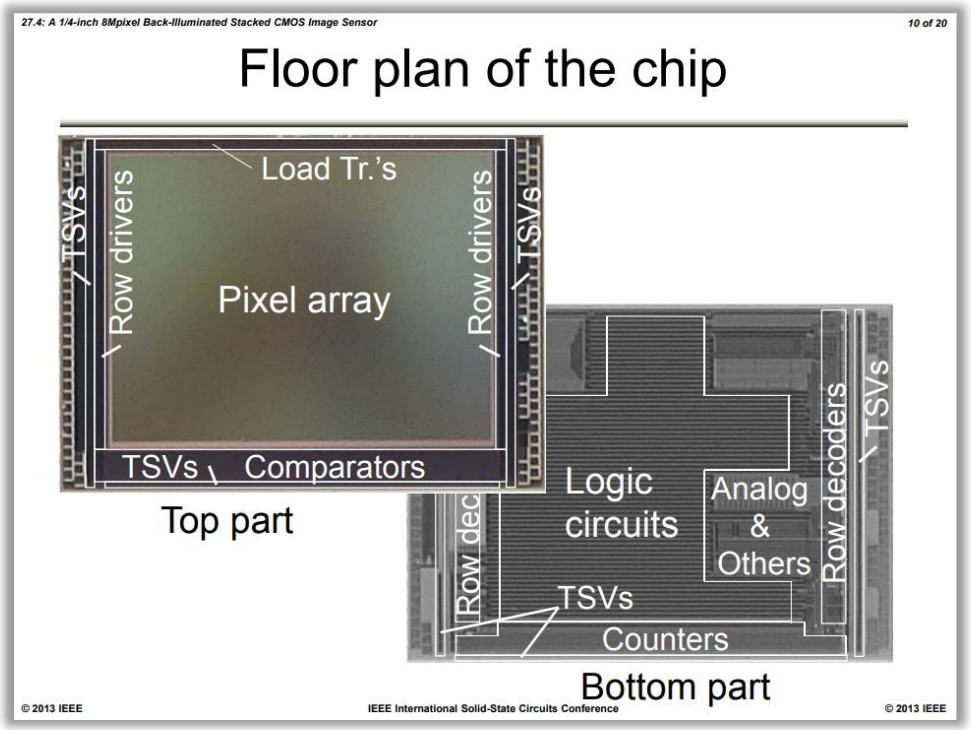
G

Full HD 1080

SONY 左：AVCHD HDDデジタルハイビジョン“ハンディカム”『HDR-XR520V』(240GB)(ブラック)
右：AVCHD HDDデジタルハイビジョン“ハンディカム”『HDR-XR500V』(120GB)(シルバー)

Back Illuminated Sensor　Stacked Structure





H. Wakabayashi *et al*., "A 1/2.3-inch 10.3Mpixel 50frams/s Back-Illuminated CMOS Image Sensor," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp. 410-412, Feb. 2010.

S. Sukegawa *et al*., "A 1/4-inch 8Mpixel back-illuminated stacked CMOS image sensor," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp. 484-485, Feb. 2013.

Mobile　: Additional Functionality
Small Die size
Process optimization
Production capacity

Back Illuminated Sensor　3 Stacked Structure

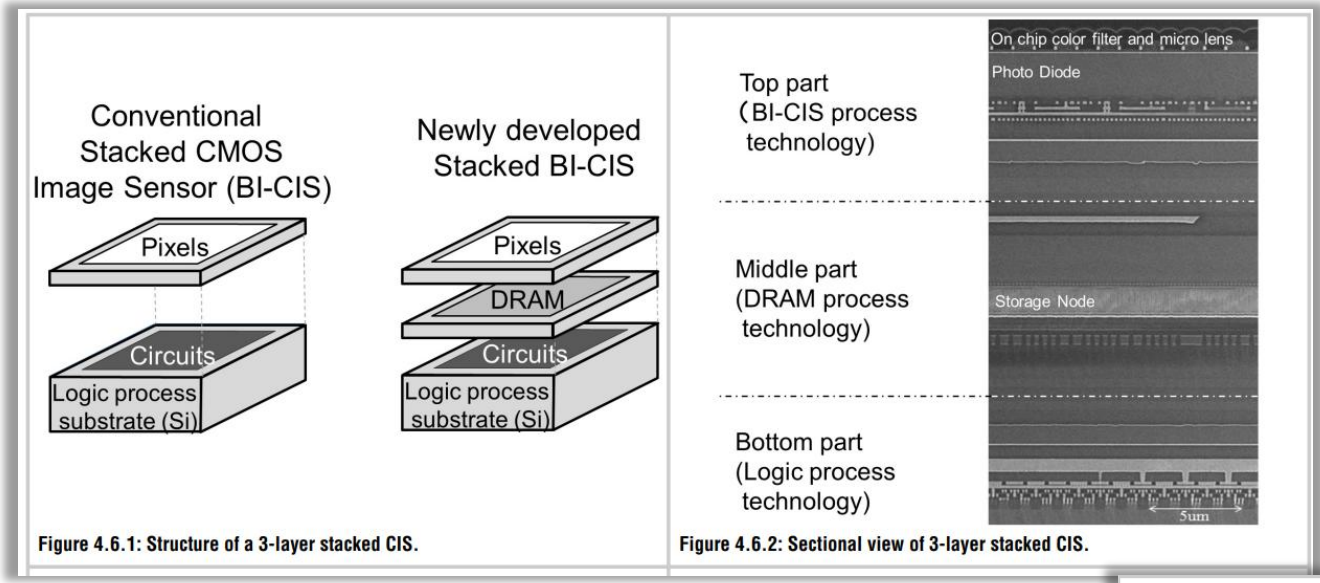


Figure 4.6.1: Structure of a 3-layer stacked CIS.

Figure 4.6.2: Sectional view of 3-layer stacked CIS.

T. Haruta *et al*., "A 1.2.3inch 20Mpixel 3-Layer Stacked CMOS Image Sensor with DRAM," IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, pp. 76-78, Feb. 2017.

Mobile　: Super High-Speed Readout
I/F limitation

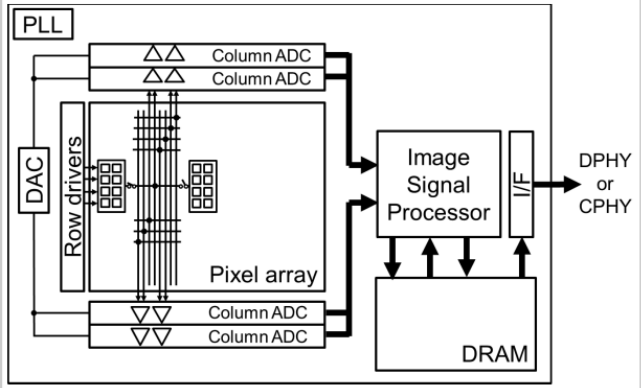


Figure 4.6.3: System block diagram.

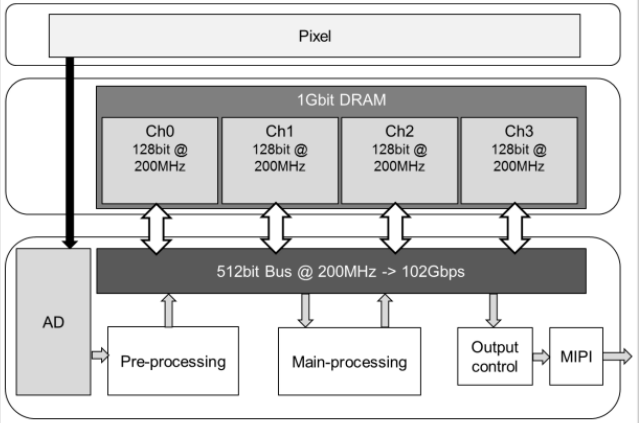


Figure 4.6.4: Block diagram for logic and bus.

Conclusion

Evolution of the Readout architecture

Functional parallelization

Evolution of the Pixel / Structure

Process and production parallelization

Each evolution followed application demands
or
Each evolution accelerates application markets