A 0.5μm Pixel-Pitch 200-Megapixel CMOS Image Sensor with Partially Removed Front Deep Trench Isolation for Enhanced Noise Performance and Sensitivity.

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Outline

- **Introduction**
- **Proposed 0.5μm-pixel sensor**
- **Key Technologies :**
  - DTI-Cut applied FDTI Structure
  - Low-loss FDTI & Optical Structure
  - Contact Wall & Metal/Gate Vertical Stack Down
- **Sensor Characteristics**
- **Summary**

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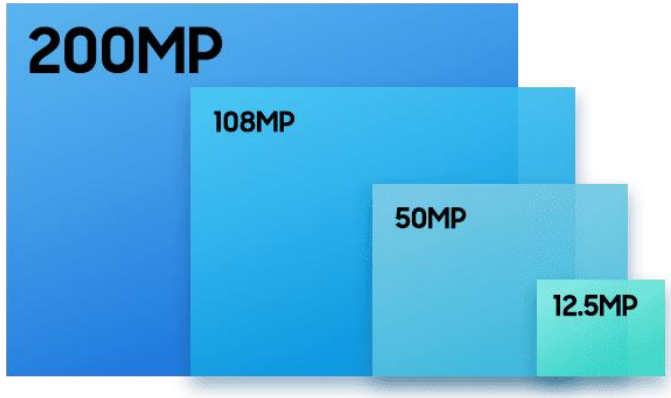
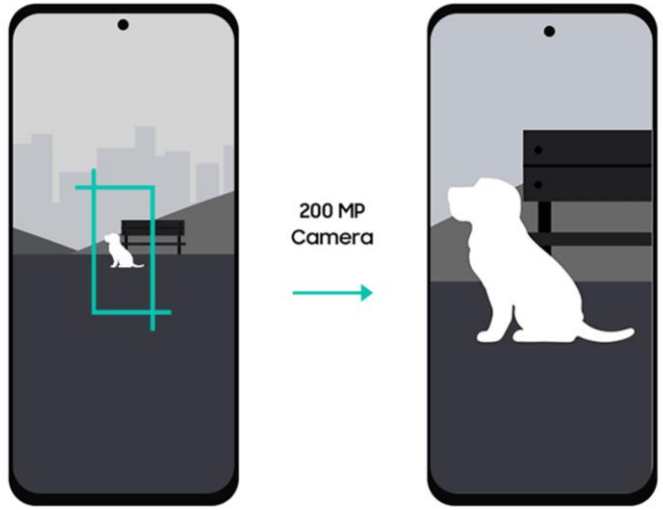
Introduction

- **A high resolution image sensor enables**
  - ✓ The capture of more information for more details
  - ✓ The more details of the cropped image
  - ✓ Superior image quality under various zoom conditions



- **For a high pixel-count image sensor,**
  - ✓ Smaller pixels are needed to be packed into the limited space of mobile devices
  - ➔ Several challenges as increased metal density, decreased SF area and weaker light focusing



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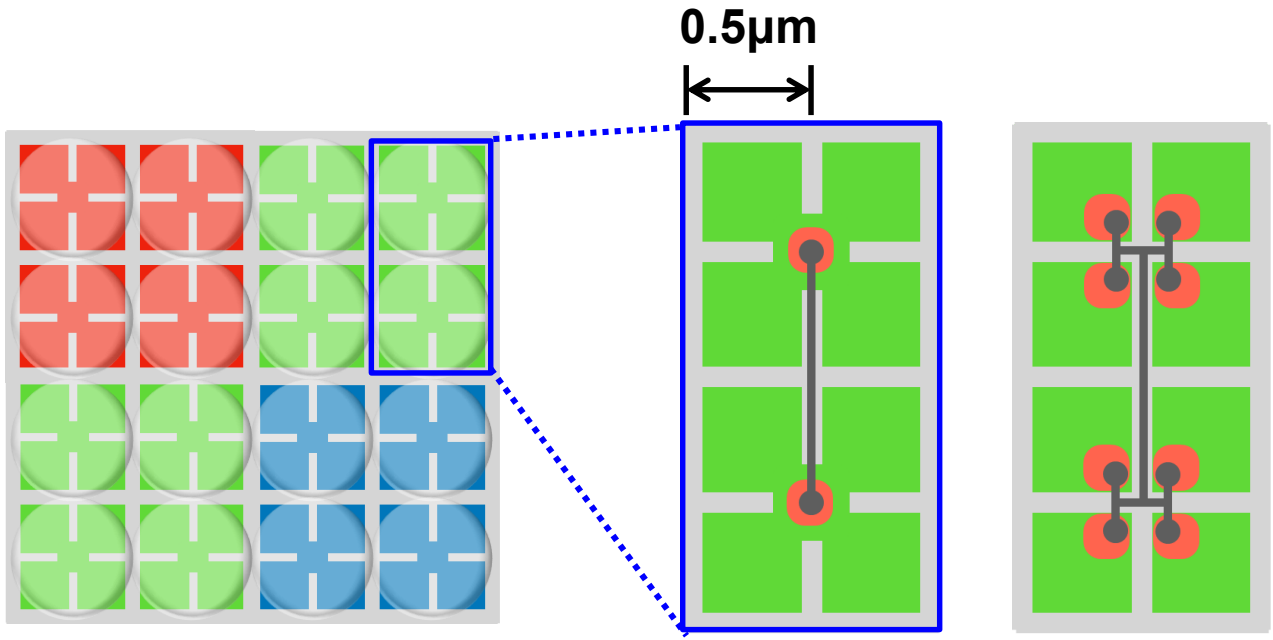
Proposed 0.5µm-pixel sensor

- 0.5µm Pixel-Pitch 200Mp CMOS Image Sensor
- 2x4 FD-Shared Pixel Unit with DTI-Cut Structure



Low FD Junction/Metal Cap
➔ Low RN(e-) w/ High CG

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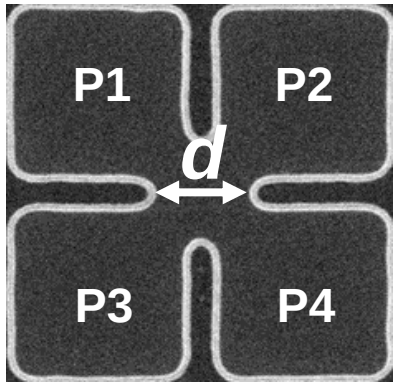
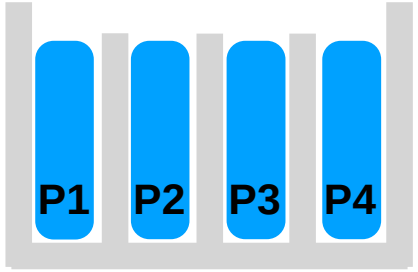
DTI-Cut applied FDTI Structure

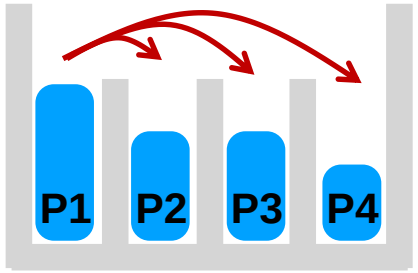
■ Signal Linearity w/ DTI-Center-Cut Width



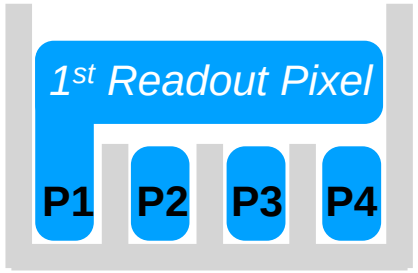
High Potential Barriers
➔ Good Linearity



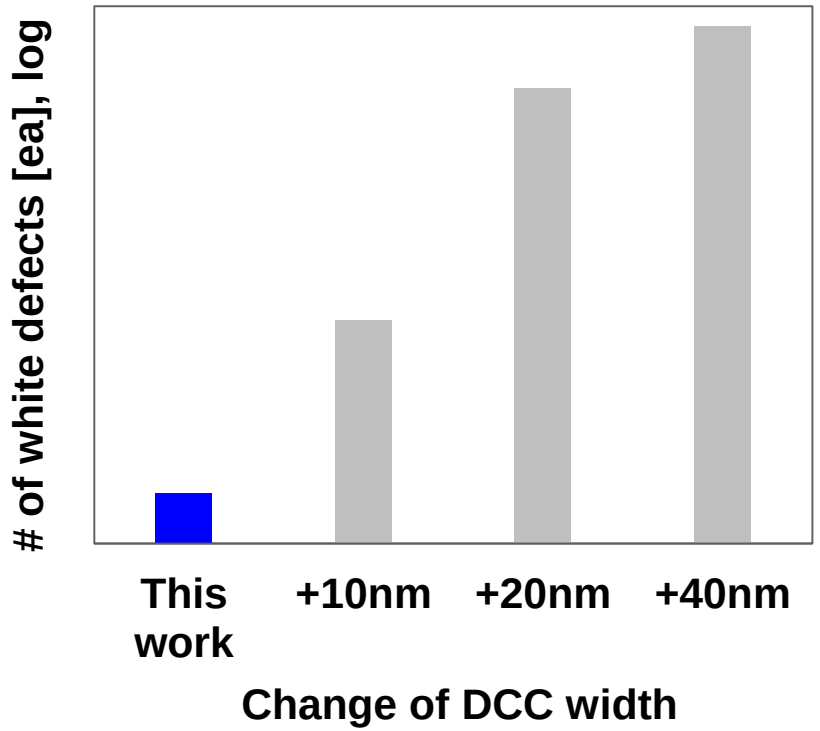
Low Potential Barriers
➔ Inter-pixel Overflow



Poor Potential Barriers
➔ White Defect Noise

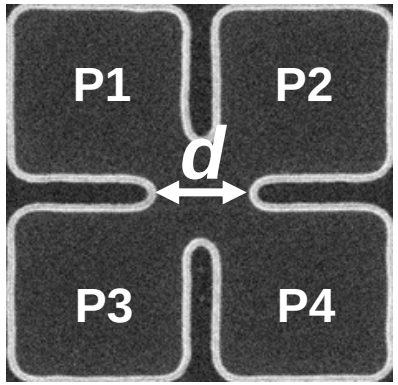


Decrease of White Defects as DCC Width Narrows

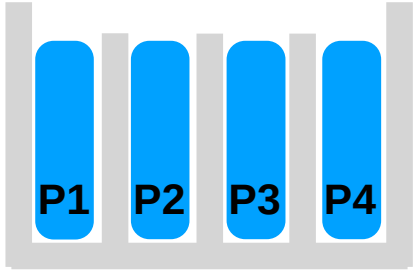


DTI-Cut applied FDTI Structure

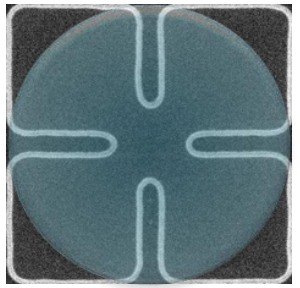
■ Signal Linearity w/ DTI-Center-Cut Width

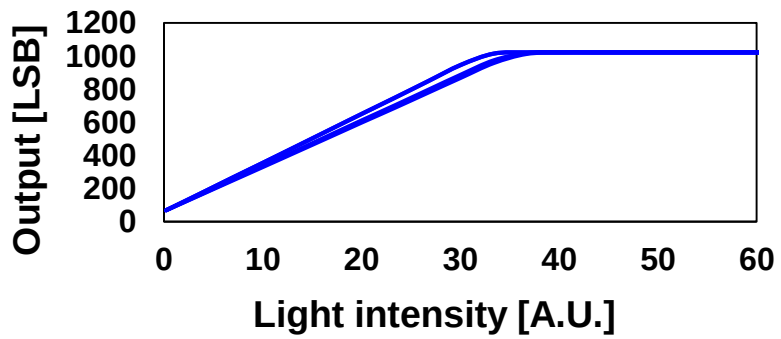


High Potential Barriers
➔ Good Linearity

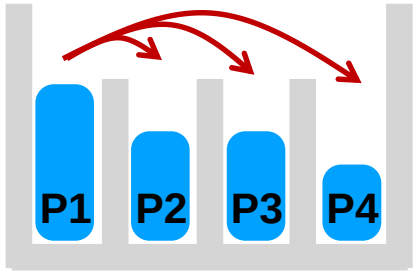


Linear Output w/ Symmetric Light Incidence

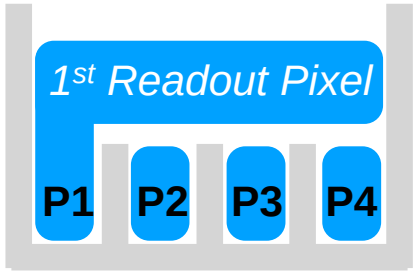




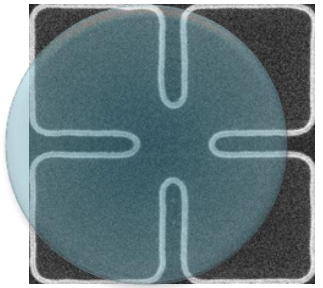
Low Potential Barriers
➔ Inter-pixel Overflow

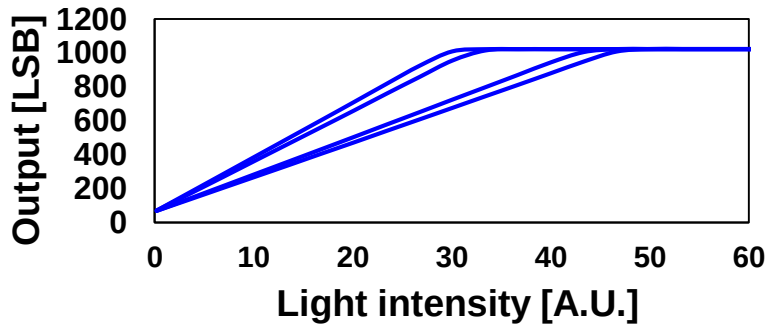


Poor Potential Barriers
➔ White Dot Noise



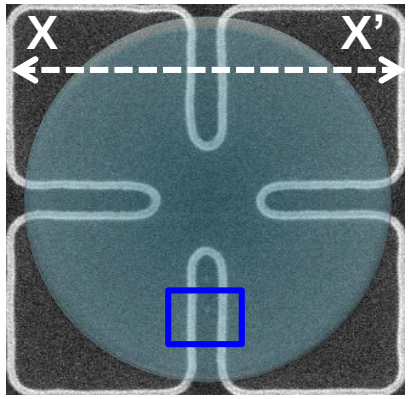
Linear Output w/ Asymmetric Light Incidence

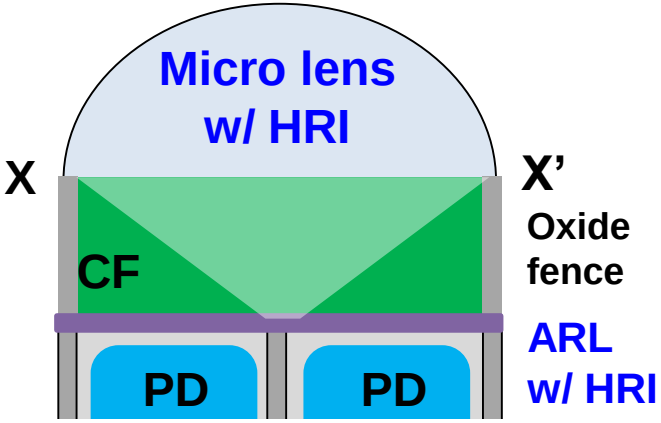




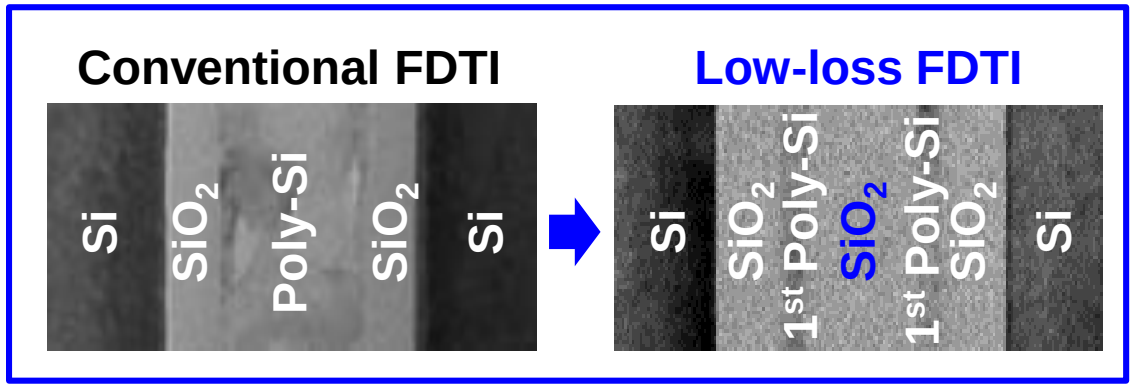
Optical Performance

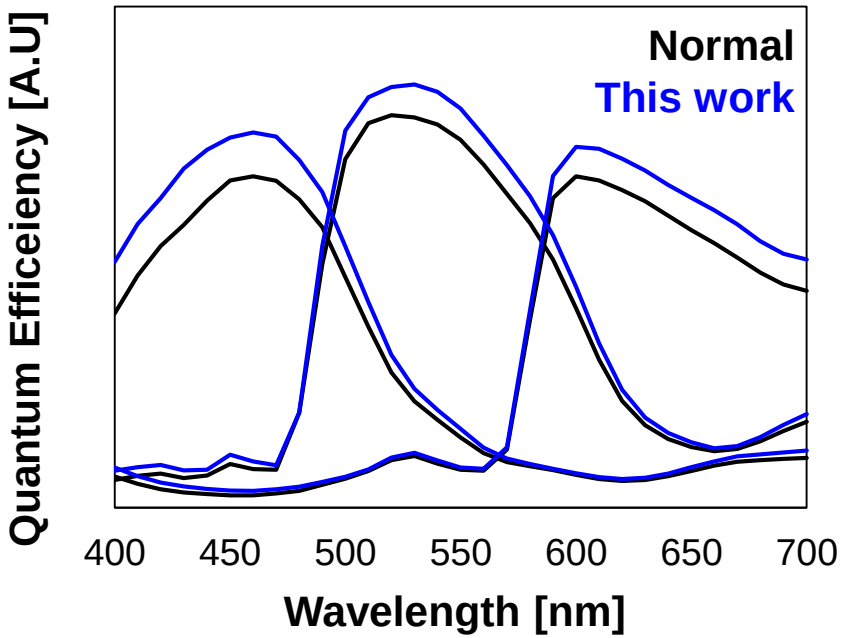
■ Low-loss FDTI & HRI Lens/ARL





Quantum Efficiency	6%▲
Crosstalk	1%▼
Sensitivity	8%▲





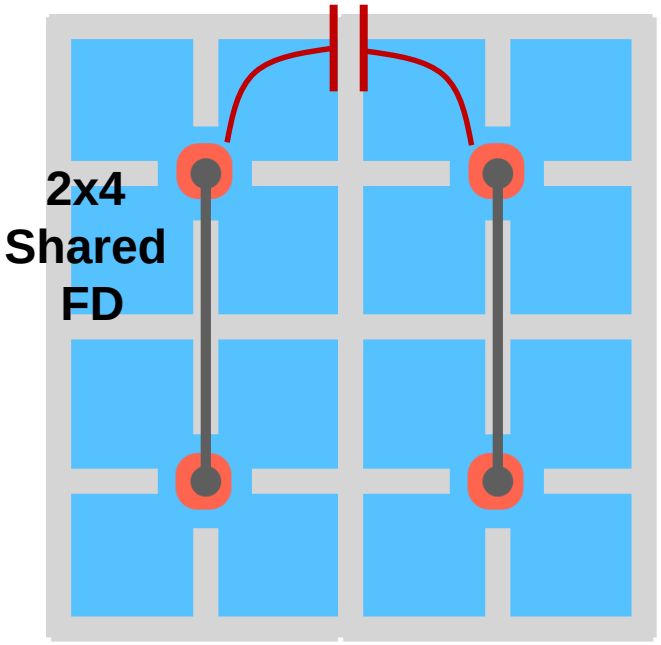
Noise Performance

■ Contact Wall

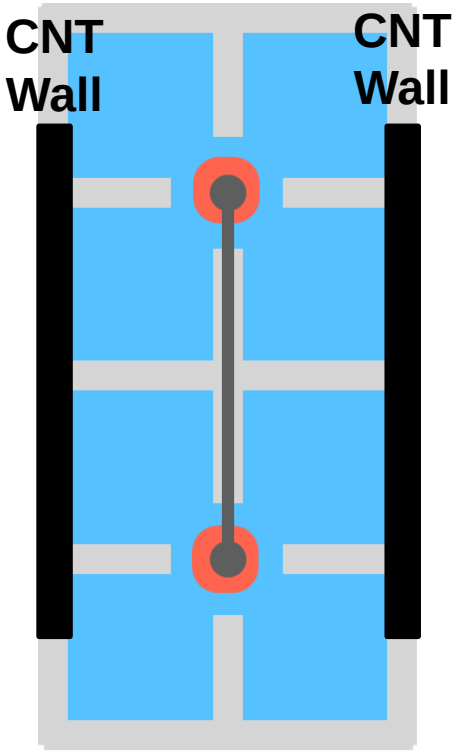
Inter-Pixel Coupling [%]

= $Cap[(FD, JMP, Vout)_{center}\text{-to-}FD_{left/right}] / Cap\_FD_{center}$

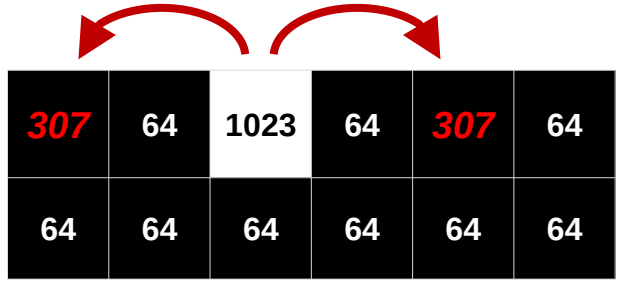
Small Pixel-Pitch
➔ **Parastic Cap. between FDs ▲**
➔ **Coupling Noise ▲**



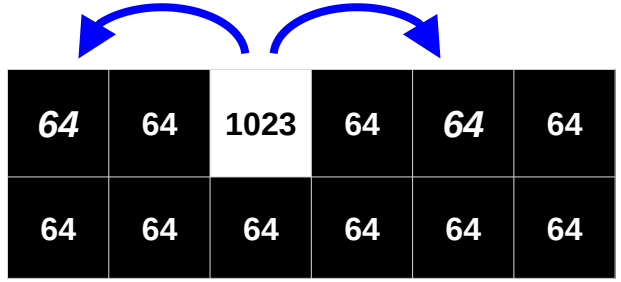
De-Coupled FDs by CNT Wall



Coupling Ratio 2.0% w/o CNT Wall



Coupling Ratio <0.01% w/ CNT Wall

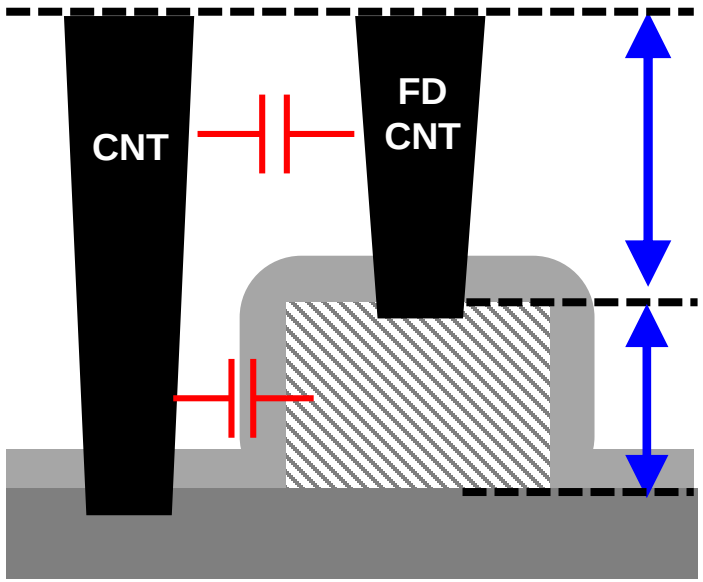


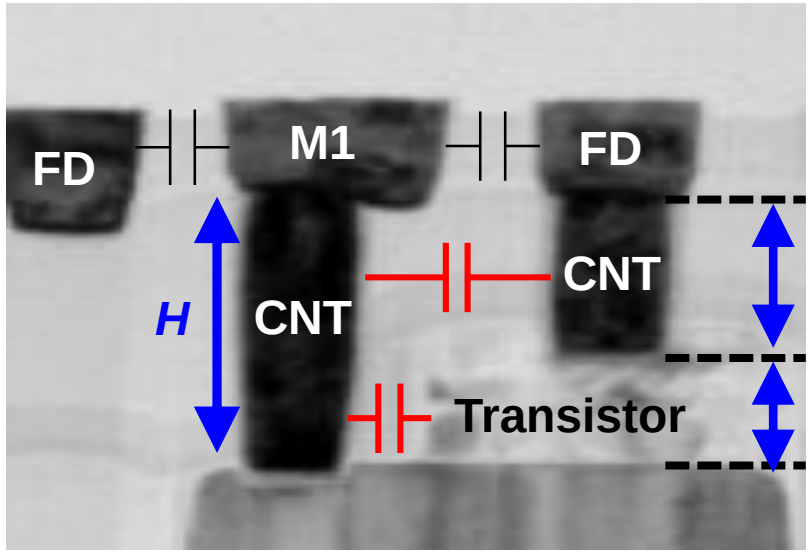
with assumption of ADCsat 1000mV and Gain x16

Noise Performance

■ Metal/Gate Vertical Stack Down

Reduced CNT/Gate-Poly Stack Height
➔ Low RN(e-) w/ High CG

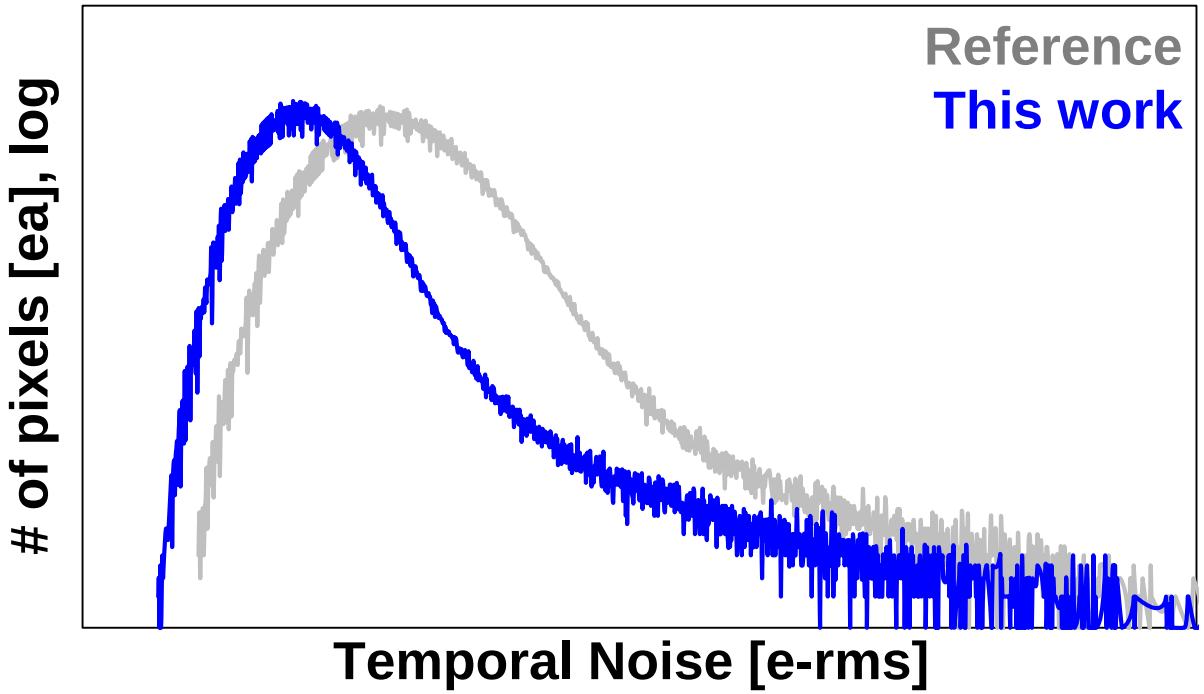




	Stack Height(H)	FD Capacitance
Vertical Stack Down	▼40%	▼15%

Noise Performance

- DCC-applied FDTI (FD Cap.▼)
- 3-SF connected in parallel (Effective SF-Area ▲)
- Metal/Gate Vertical Stack Down (FD Cap.▼)



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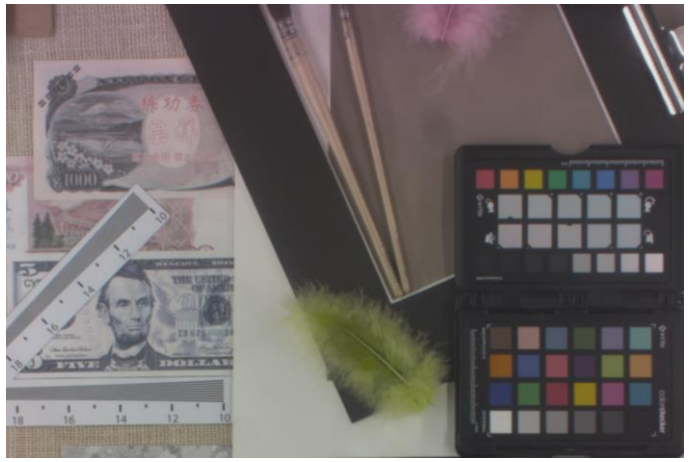
Sensor Characteristics

Items	unit	0.56㎛ Pixel	This Work
Unit pixel size	㎛	0.56 × 0.56	0.5 × 0.5
FWC (full/binning)	e-	4,700 / 75,000	3,700 / 59,000
Temporal noise†	e-	2.3	1.6
Random telegraph signal†	ppm	< 1	1
Pixel dynamic range†	dB	90.3	91.3
Sensitivity / Area	e-/lux.sec/ ㎛^{2}	3746	3750

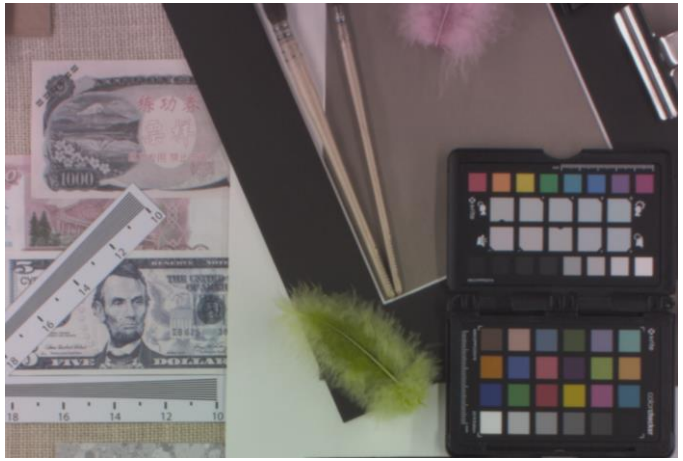
† Pixel Binning Mode

Dynamic Range[dB] = 20 × log(FWC[e-]/TN[e-])

Previous 0.56㎛ Pixel



This Work



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- **A 200Mp CMOS image sensor with a unit pixel size of 0.5μm based on the quad-cell FDTI structure**

- **The developed sensor has**
  - **Competitive CG and noise characteristics** by appling DTI-Cut structre and Meta/Gate stack down technology,
  - **Good linearity of the unit pixel** by designing a sufficiently narraw DCC width,
  - **Enhanced Optical performance** with low loss FDTI and HRI ARL/micro-lens.