A CMOS Image Sensor with Pixelwise Triple-CG Modulation and Gain-Regulating Pre-ISP for Single-Frame Adaptive TCG-HDR Imaging

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Agenda

- **Background and Motivation**: Low-Power Single-Frame HDR Imaging
- **Key Technologies**: Pixelwise TCG Modulation and Gain Regulations
- **Chip Design and Operation**: On-chip TCG Modulation and Pre-ISP
- **Experimental Results**: Adaptive TCG-HDR Imaging
- **Conclusion**

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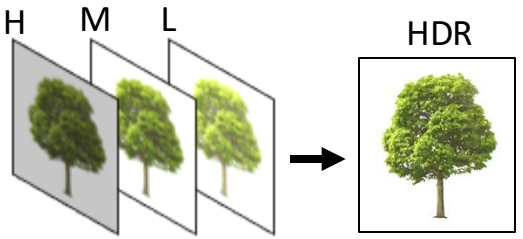
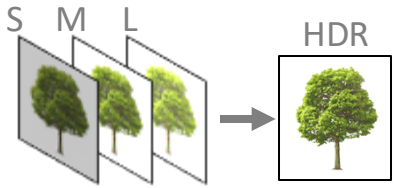
Background: Single-Frame HDR Imaging

Image Frame w/o HDR



Single-Frame HDR
(Merge Multiple Readouts)

- Dual-CG (DCG) HDR Imaging
- **Triple-CG (TCG) HDR Imaging**
- Dual-AG[1] (DAG) HDR Imaging
- LOFIC-HDR Imaging[2]
- Split-Pixel HDR Imaging
- Coded-Exposure HDR Imaging
- ……



Multi-Frame HDR
(Merge Multiple Frames)

- Staggered-HDR Imaging
- QBC-HDR Imaging[4]
- ……

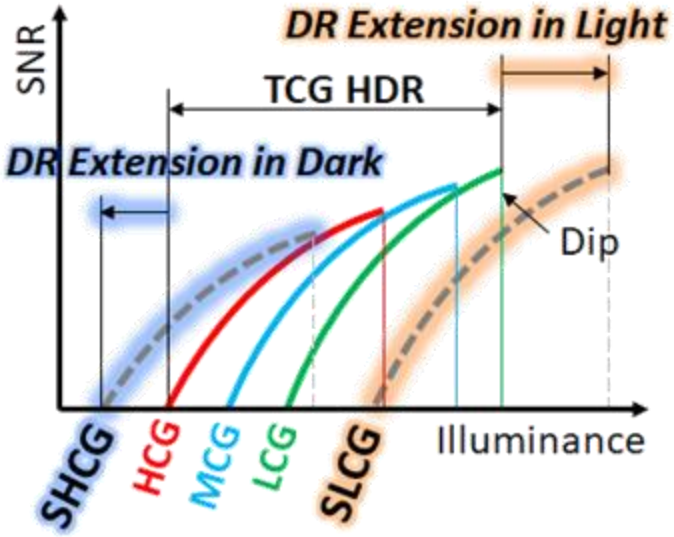
- ☺ **Good Image Quality**
- ☺ **No Motion Ghost**
- ☺ **Native Resolution**

- ☹ **Limited DR[3] Extension**
- ☹ **Frame Rate ↓**
- ☹ **Power Consumption ↑**

1. Dual AG: Dual Analog Gain
2. LOFIC: Lateral Overflow Integration Capacitor
3. DR: Dynamic Range
4. QBC: Quad-Bayer Coding

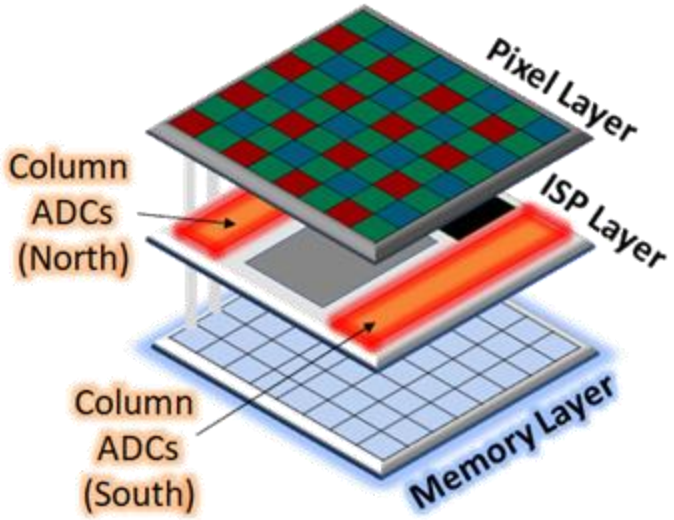
Background: Single-Frame HDR Imaging

Limited DR Extension



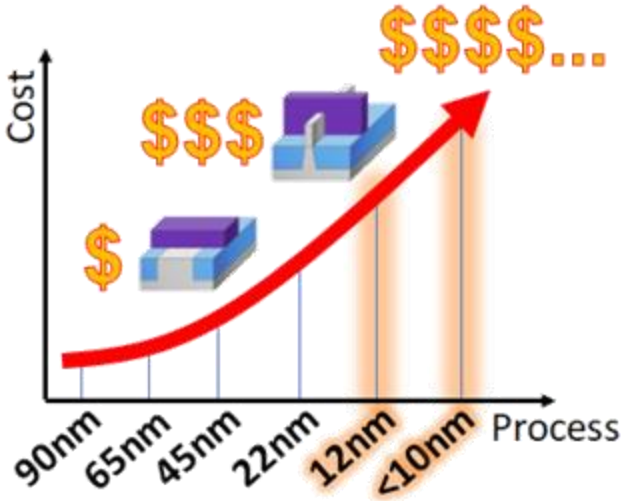
- **Solution**: adding **SHCG**[1] or **SLCG**[2]
- More readouts in a frame
- Could induce SNR dips

Frame Rate ↓



- **Solution:** adding more **ADC**s
- **Solution:** stacking a **memory layer**
- Power consumption ↑↑

Power Consumption ↑

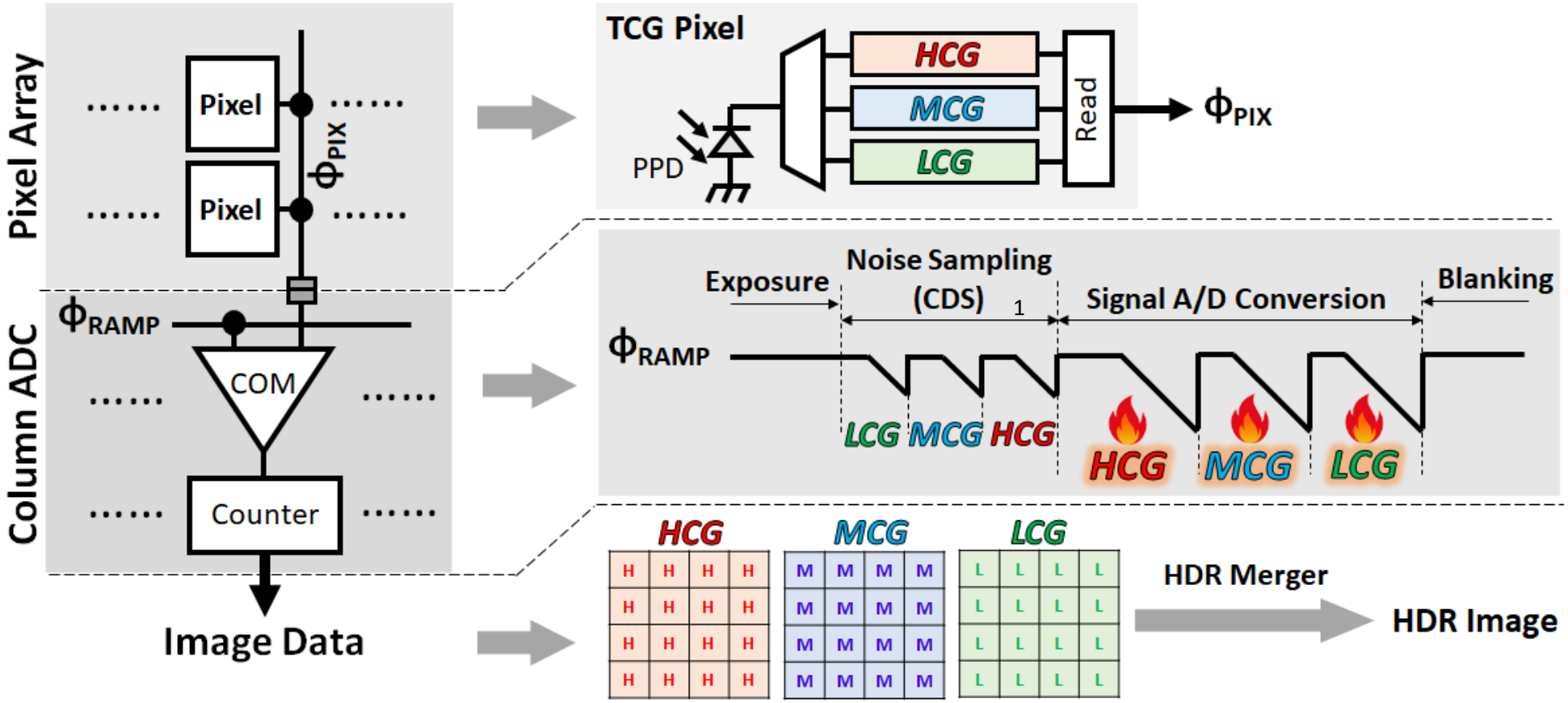


- **Solution:** using **advanced process**
- Fabrication costs ↑↑↑
- Design costs ↑↑

1. SHCG: Super-High Conversion Gain (e.g. using super small FD)
2. SLCG: Super-Low Conversion Gain (e.g. using LOFIC)

Background: Single-Frame HDR Imaging

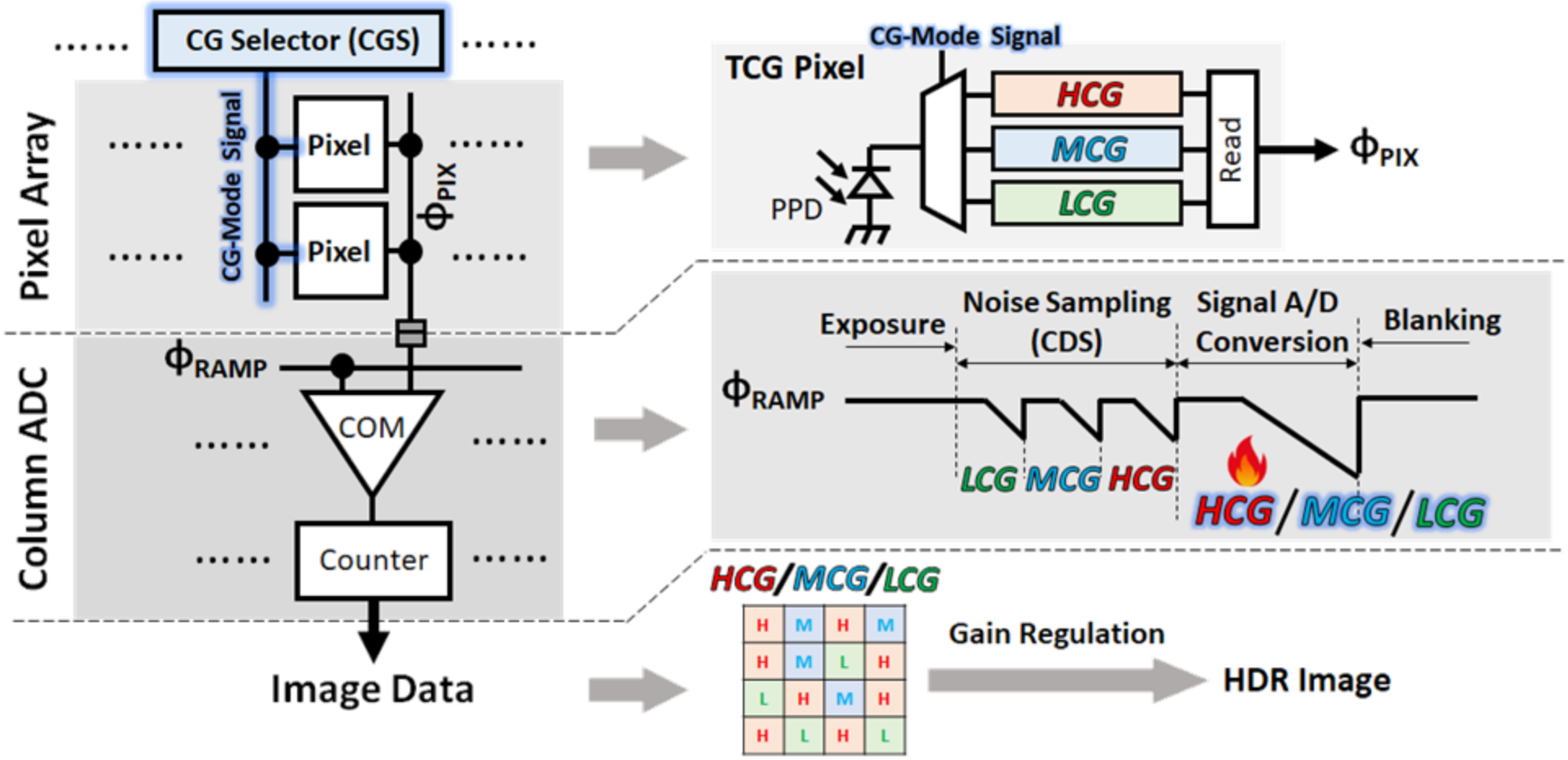
Root Cause: Too many pixel readouts and A/D conversions in a frame period



1. CDS: Correlated Double Sampling

Motivation: Low-Power Single-Frame HDR Imaging

Idea: Reduce # of pixel readouts and A/D conversions → single-frame **LPTG-HDR**[1] **imaging solution**



1. LPTG: Low-Power Triple Gain

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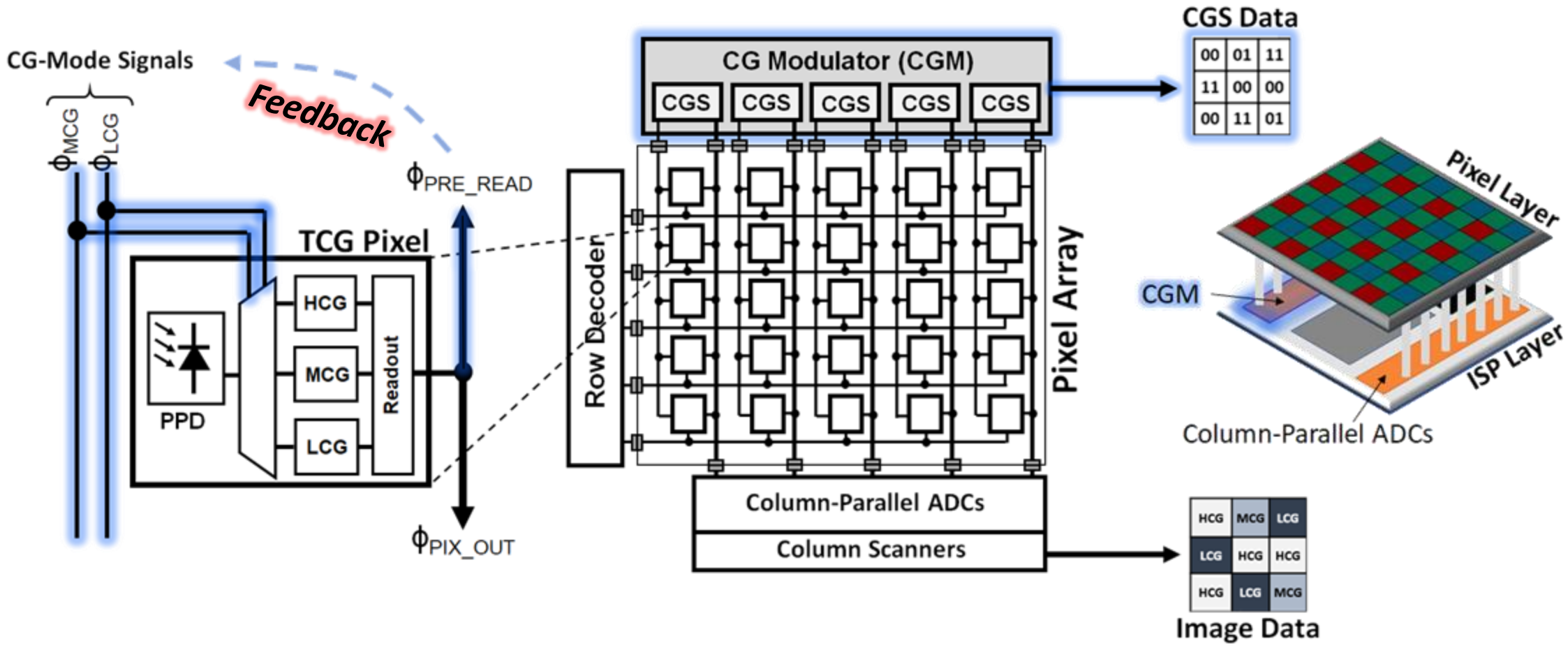
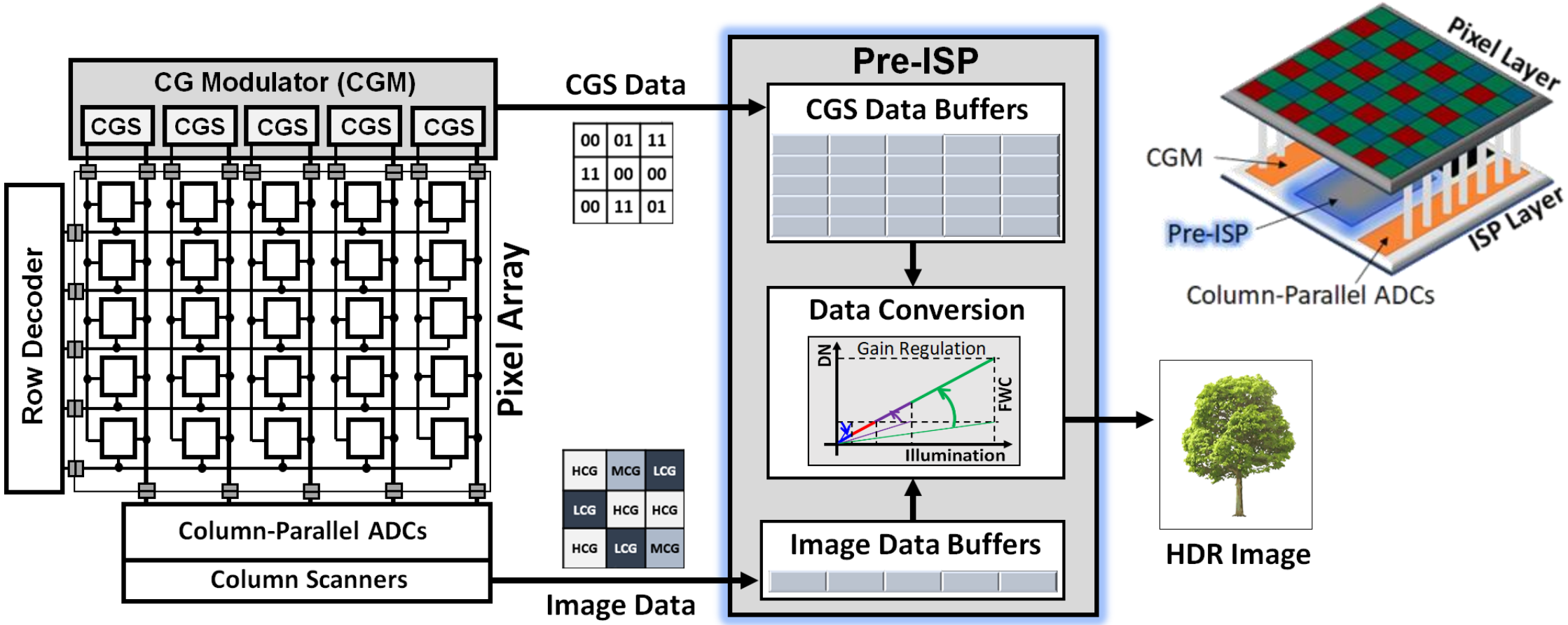
Key Technology: Pixelwise CG Modulation

By providing ϕ_{PRE_READ}, pixels receive their own CG-mode signals from the column CGS.



Key Technology: On-Chip Pre-ISP for Gain Regulations

Both CGS data and image data are buffered in a pre-ISP for HDR image synthesis.



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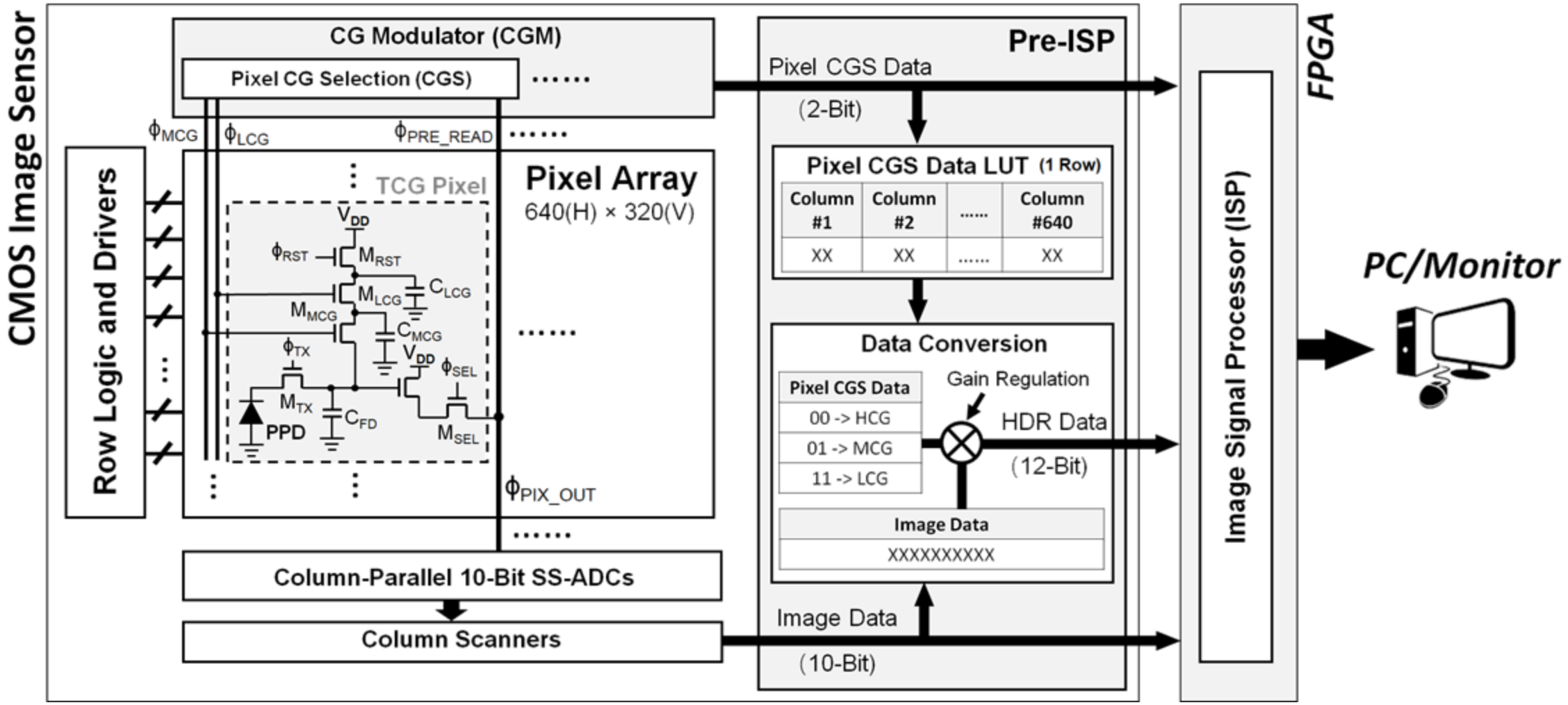
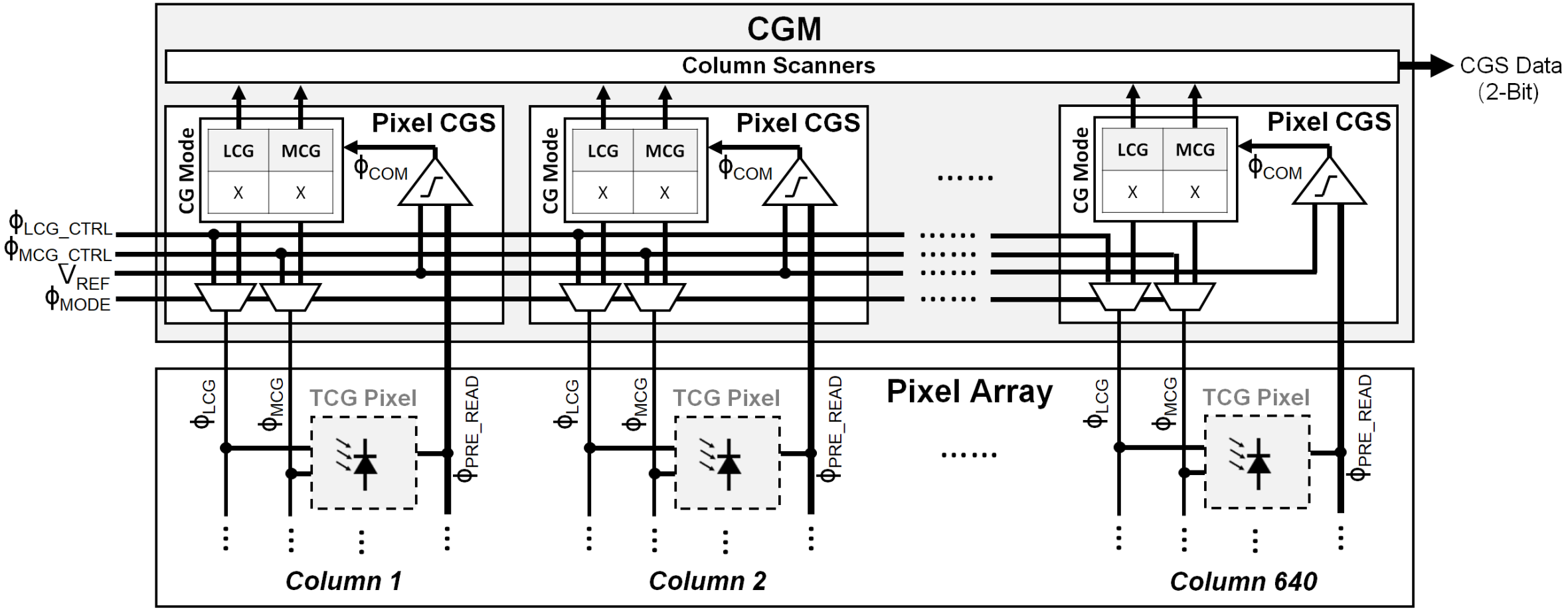
Chip Design: Overall Chip Architecture



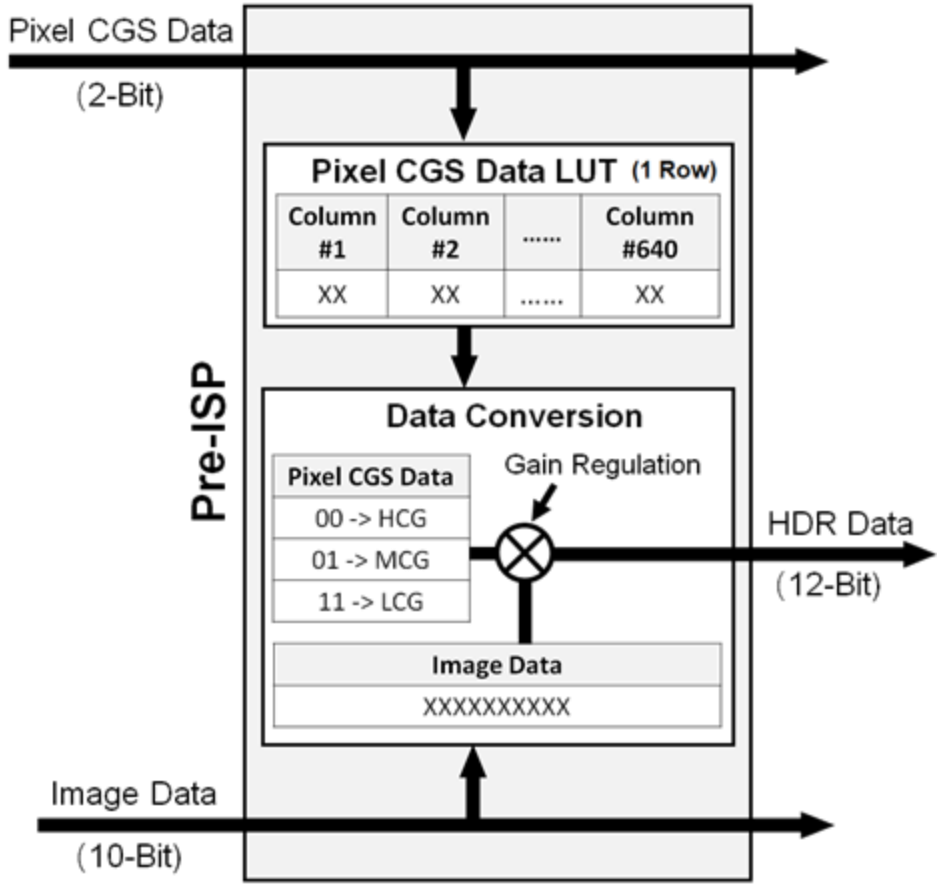
Chip Design: On-Chip Pixelwise TCG Modulation

CG-Mode signals are determined by comparisons and can be override with user-defined values.

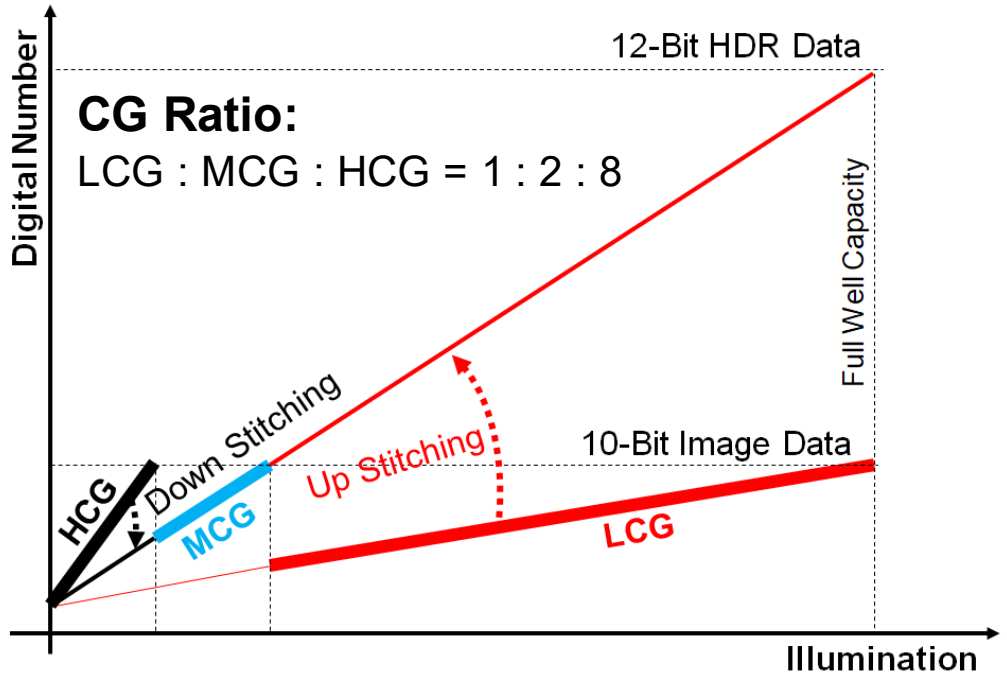


Chip Design: On-Chip Pre-ISP

All image data are regulated according to the CGS data stored in the LUT[1].



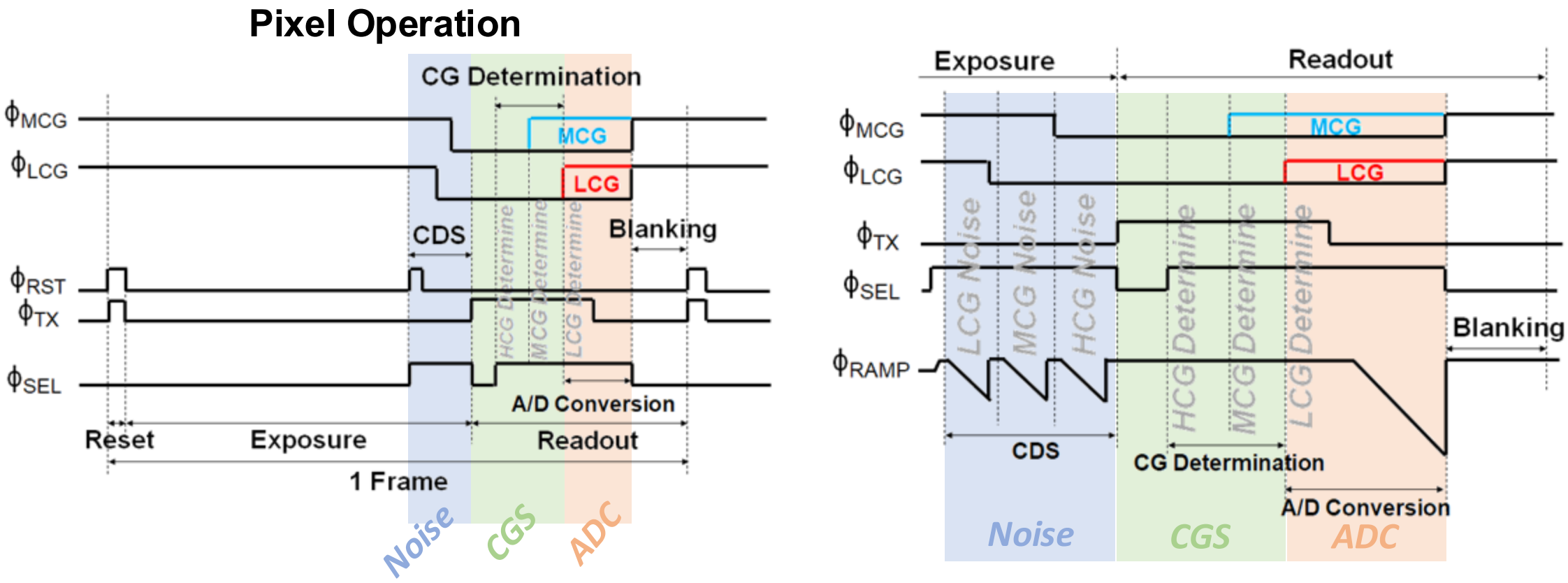
- **Down stitching** image data in HCG[2]
- **Up stitching** image data in LCG
- Output HDR image data are in 12 bits



1. LUT: Look-up Table
2. To save HDR data bandwidth

Operation: Pixelwise TCG Modulation in Rolling Shuttering

Each pixel experiences CDS and a single full-bit-depth A/D conversion.



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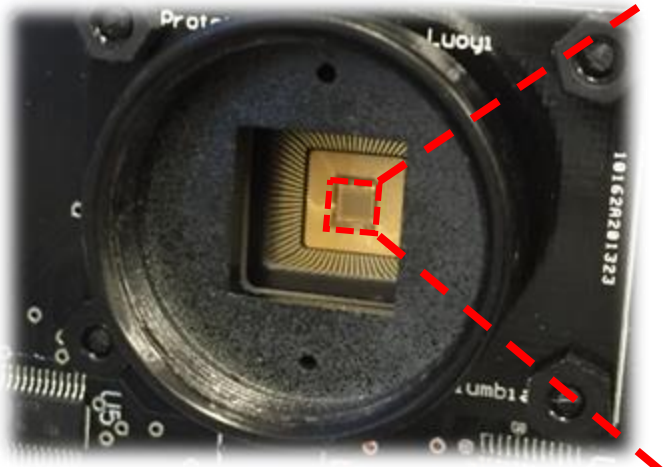
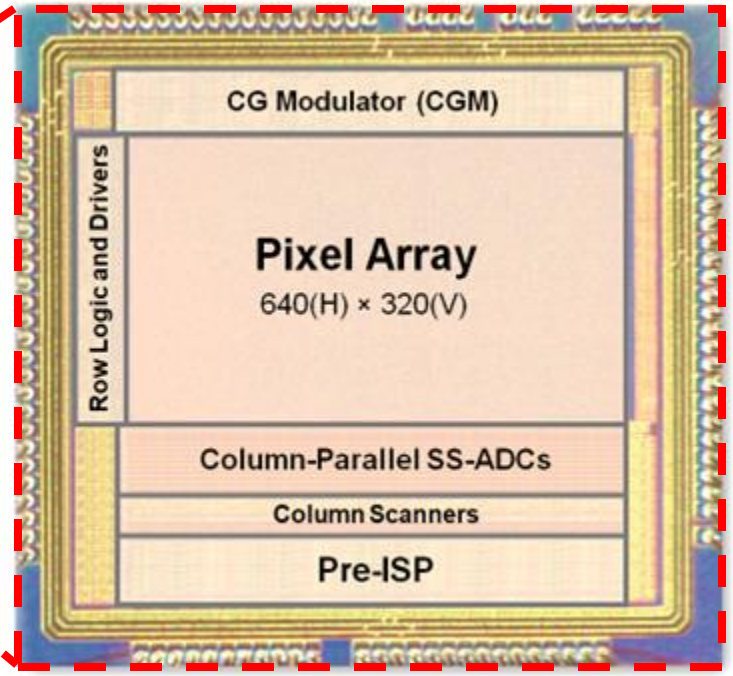
Experimental Results: Prototype CIS Chip

Camera Module

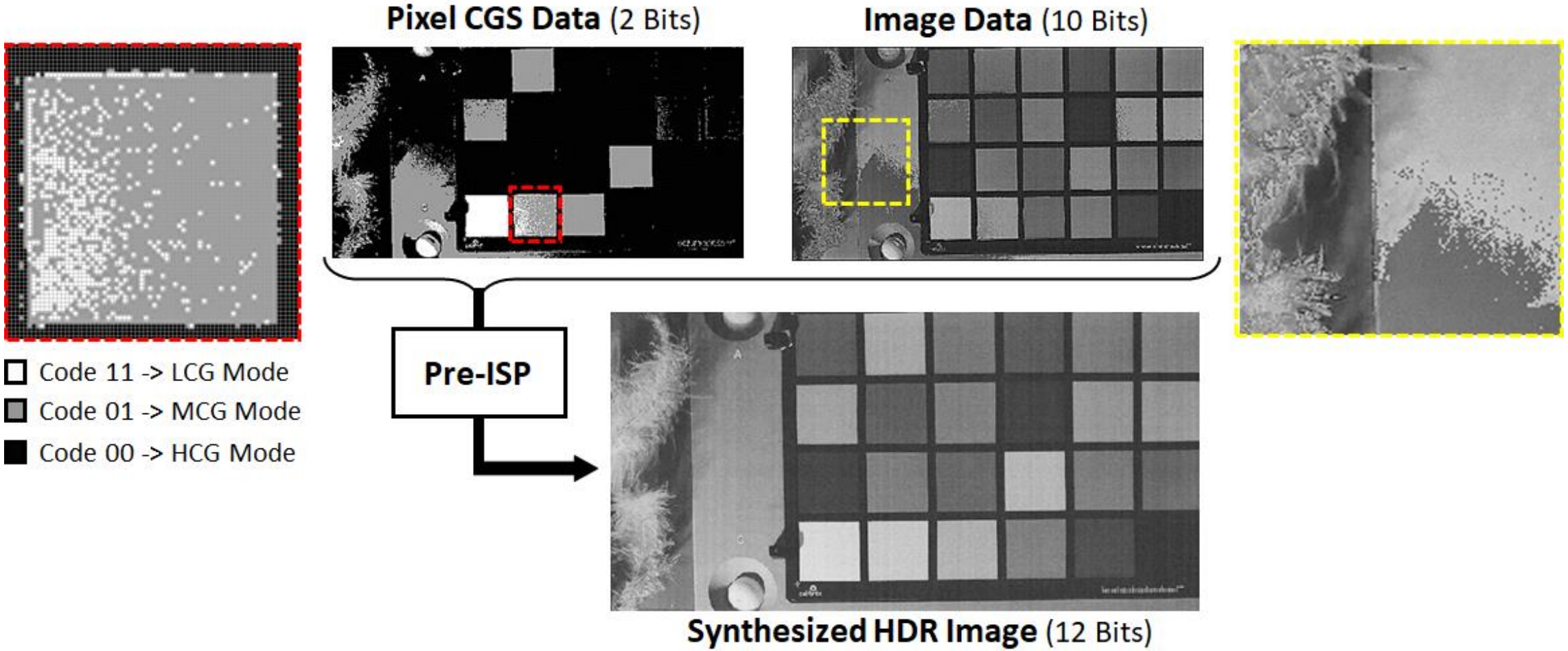


Die Micrograph



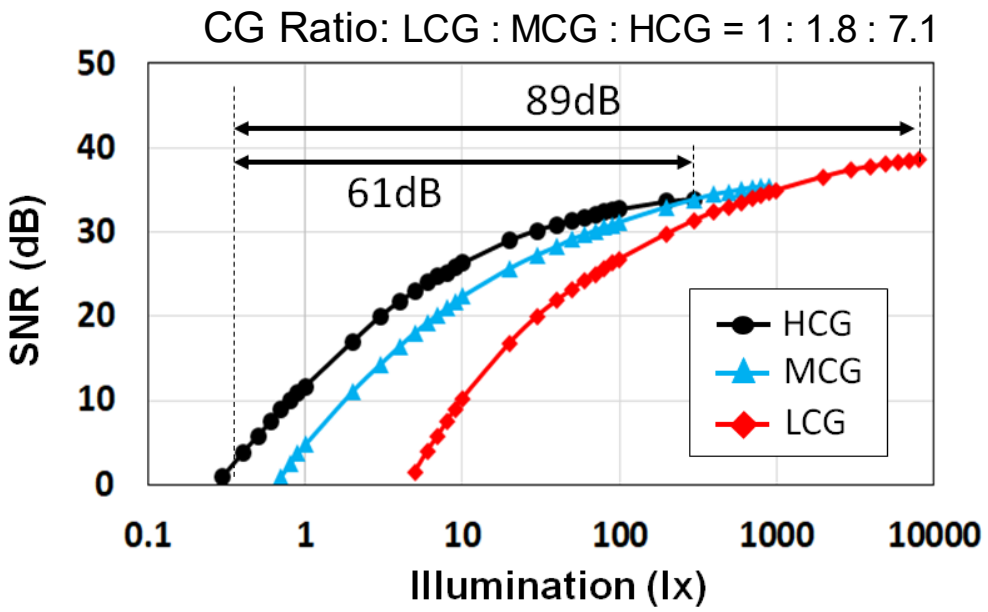
Chip Size	4.5mm × 4.0mm
Process	110nm CMOS FSI
Resolution	640 × 320
Pixel Size	5.0μm × 5.0μm
Shutter Type	Rolling Shutter
HDR Frame Rate	60fps
Conversion Gain	LCG: 23μV/e-
	MCG: 42μV/e-
	HCG: 164μV/e-
Supported HDR Technologies	TCG-HDR Imaging
	Adaptive TCG-HDR Imaging

Experimental Results: Sample Images

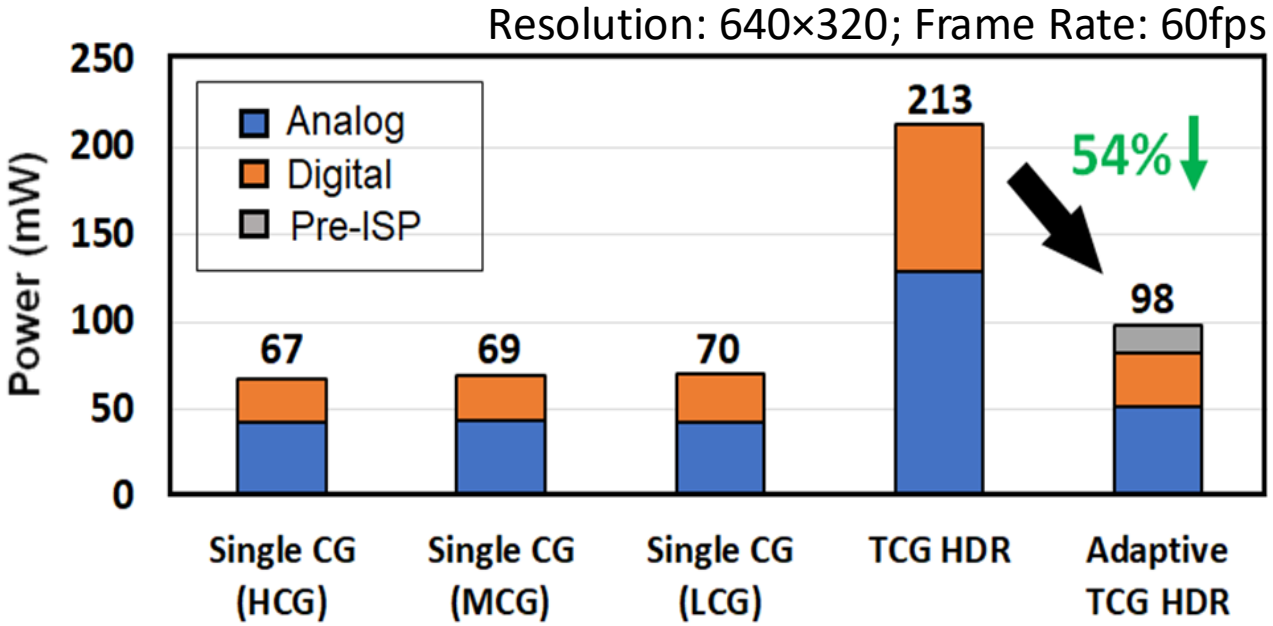


Experimental Results: Measurement Results

SNR Curves in Single CGs



Power Consumption



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Conclusion: Comparison Table

	This work			JSSC 2025 [1]		VLSI 2022 [2]	IISW 2019 [3]	
Process	110nm CIS			350nm CIS		110nm CIS	65nm BSI	
Pixel Pitch (µm)	5.0			7.2		7.0	2.8	
Pixel Array	640 × 320			512 × 320		320 × 320	1280 × 514	
HDR Frame Rate (fps)	60			60		100	30	
HDR Power FoM (nJ/frame·pixel)	**7.9 (Adaptive TCG HDR)**			9.9 (Adaptive DCG HDR)		11 (Coded Exposure HDR)	N/A	
CG (µV/e-)	**164 (HCG)**	**42 (MCG)**	**23 (LCG)**	228 (HCG)	46 (LCG)	N/A	160 (HCG)	10 (LCG)
CG Ratio	1:1.8:7.1			1:5		N/A	1:16	
Dynamic Range (dB)	HDR: 89			HDR: 90.5		HDR: 101.5	HDR: >100	
Adaptive Tuning	**Yes (Pixelwise)**			Yes (Pixelwise)		Yes (Pixelwise)	No	
In-Pixel Buffer	**No[1]**			Yes (DRAM Signal Buffer)		Yes (Charge Storage Diode)	No	
Charge Modulation	**No**			No		Yes (2 Tap)	No	
On-Chip ISP	**Yes**			No		No[2]	Yes	
Imaging Application	**Adaptive TCG-HDR Imaging**			Adaptive DCG-HDR Imaging		Adaptive Temporal HDR Imaging	DCG-HDR Imaging	

1. Use a typical TCG pixel design.
2. CIS and ISP are in different non-stacked chips.

Conclusion: Remarks and Future Outlooks

Introducing Adaptive TCG-HDR Imaging as a single-frame LPTG-HDR imaging solution

- Enabled by per-frame pixelwise TCG modulation
- Reducing # of pixel readouts and A/D conversions to save power

Presenting a CMOS Imager Design for adaptive TCG-HDR imaging

- Using a typical TCG pixel design (no in-pixel memory)
- On-chip CGM for pixelwise TCG modulation and on-chip pre-ISP for HDR data synthesis

Adaptive TCG-HDR imaging offers **better power efficiency** for mobile HDR applications.

Dynamic range can be extended by **adding extra CG channels**.

Reference:

[1] Y. Luo *et al*., "A 60-frames/s CMOS image sensor with pixelwise conversion gain modulation and self-triggered ADCs for per-frame adaptive DCG-HDR imaging," *IEEE Journal of Solid-State Circuits*, Vol. 60, no.2, pp. 568 – 578, 2025.

[2] R. Gulve *et al*., "A 39,000 subexposures/s CMOS image sensor with dual-tap coded-exposure data-memory pixel for adaptive single-shot computational imaging," in *Proc. IEEE Symp. VLSI Technol. Circuits*, Jun. 2022, pp. 78–79.

[3] K. Miyauchi *et al*., "A high optical performance 2.8µm BSI LOFIC pixel with 120ke- FWC and 160µV/e- conversion gain," in *Proc. Int. Image Sensor Workshop*, Jun. 2019, pp. 1–4.