Recovery of Random Telegraph Noises in a Stacked CMOS Image Sensor by High-Temperature Annealing after Hot-Carrier Stress

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Outline

- Motivation of this study
- Test chip architecture and hot carrier stress
- Proposed RTN metrology
- Hot carrier stress and high-temperature anneal
- Key results and observations
- Discussions
- Conclusions

Motivation

- Aging & reliability are important issues for all semiconductor devices, including CIS
- Hot carrier injection (HCI) is one of the aging mechanisms, as well as:
  - Bias temperature instability (BTI)
  - Time dependent dielectric breakdown (TDDB)
  - Electron migration (EM)
- Reliability testing are typically performed at elevated temperature and supply voltage
  - Speed up the aging: rely on 1000-hour data to predict 10-year lifetime
- Threshold voltage shift and mobility degradation are commonly monitored
- Reliability related to random telegraph noise is not well-known
- Statistics of large number of samples (>1M) is seldom reported
- Recovery of RTN after hot carrier stress (HCS) is less studied

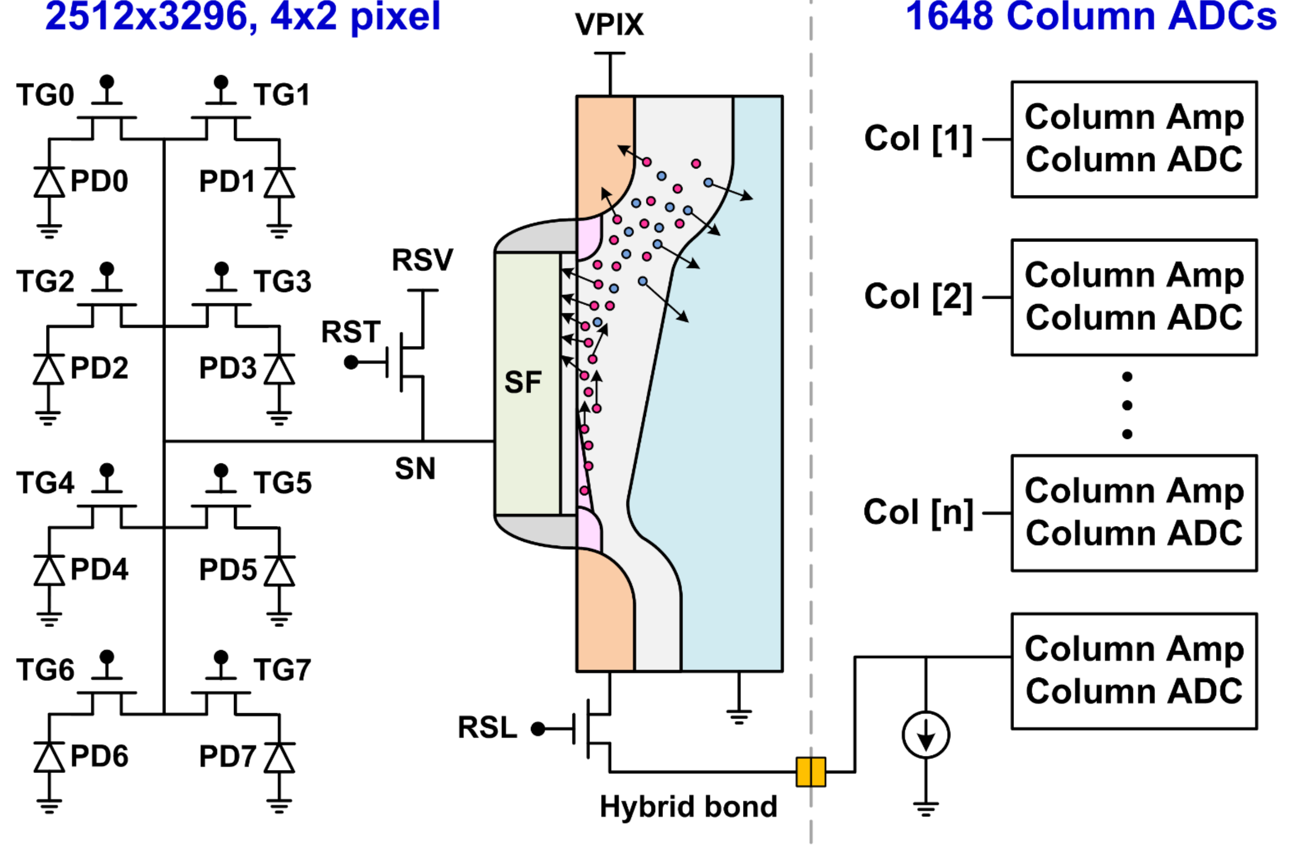
→ This work

Test Chip and Hot Carrier Stress

- 8.3MP CIS test chip architecture

2512x3296, 4x2 pixel

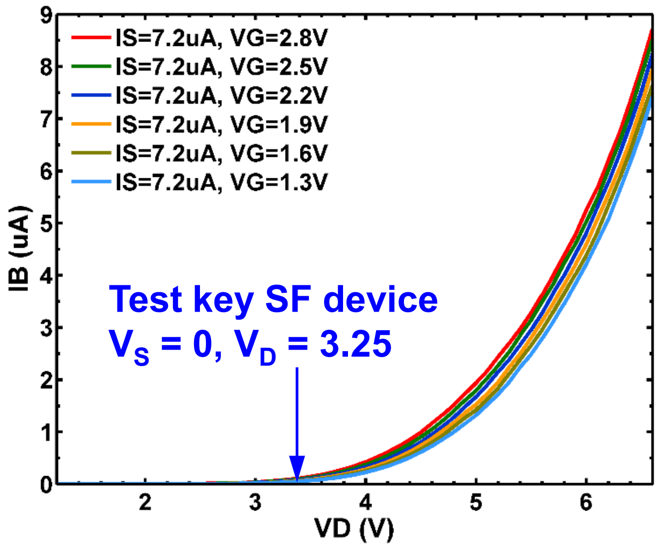
1648 Column ADCs



Top layer pixel array

Bottom readout circuits

- SF is the device under stress
- Amount of hot carrier injection is roughly ∝ substrate current I_B
- Si-SiO$_2$ energy barrier is ~3.25 eV
- Source voltage of SF is ~1.5 V when RSL is high (rolling readout)
- Hot electrons can also tunnel through the barrier

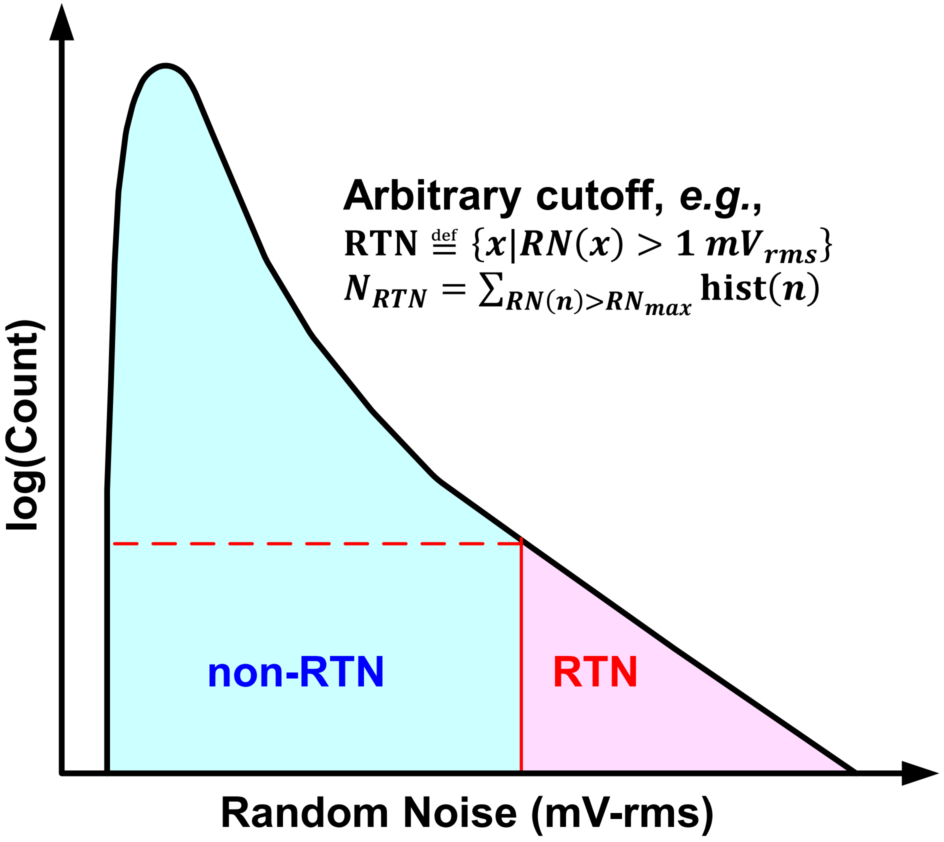


Test key SF device

$V_S = 0$, $V_D = 3.25$

RTN Metrology

- Pixels with $RN > RN_{max} \overset{\text{def}}{=}$ RTN pixels
  - Easy to specify an empirical cutoff RN_{max}
  - Convenient for process monitoring
  - Con: cutoff is arbitrary w/o physical meaning

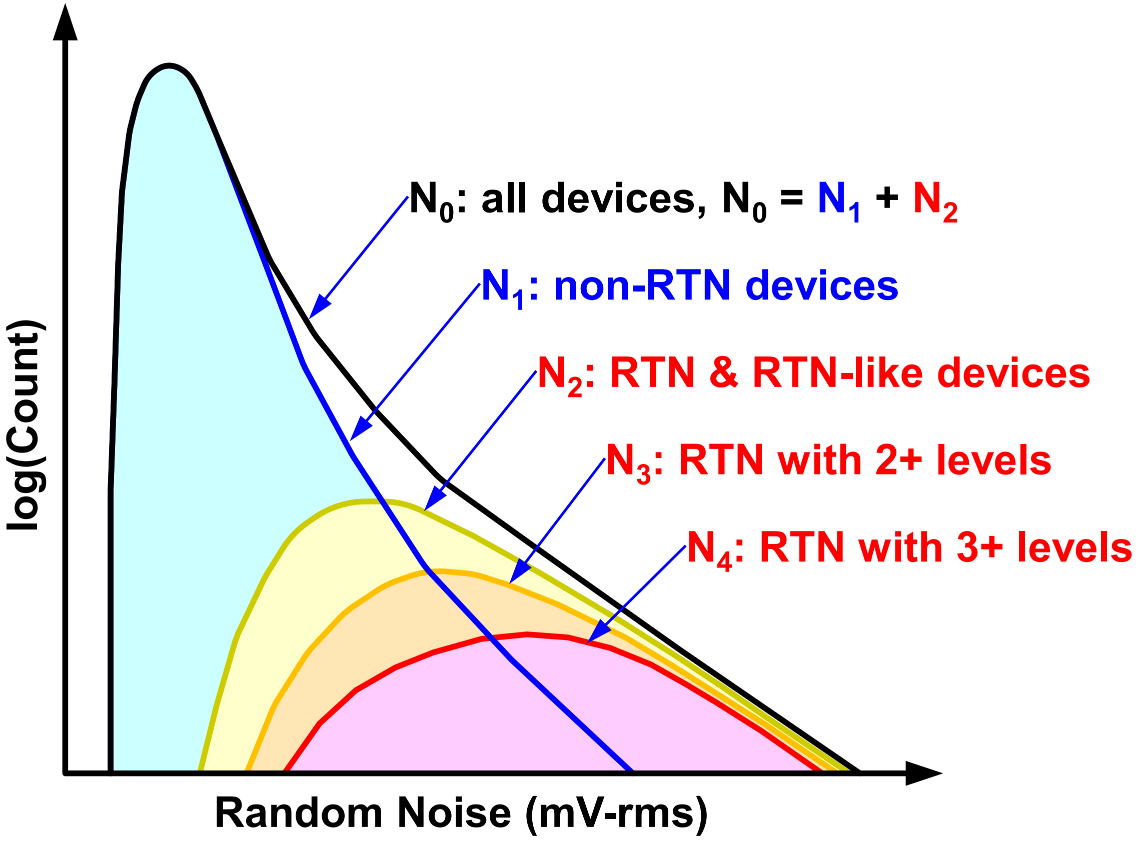


Arbitrary cutoff, *e.g.*,

$\mathrm{RTN} \overset{\text{def}}{=} \{x|RN(x) > 1\ mV_{rms}\}$

$N_{RTN} = \sum_{RN(n)>RN_{max}} \mathrm{hist}(n)$

- Pixels showing RTN behavior $\overset{\text{def}}{=}$ RTN pixels
  - The count is physically meaningful
  - Can trace the change of individual pixels
  - Con: requiring large amount of data & calculation



N_0: all devices, $N_0 = N_1 + N_2$

N_1: non-RTN devices

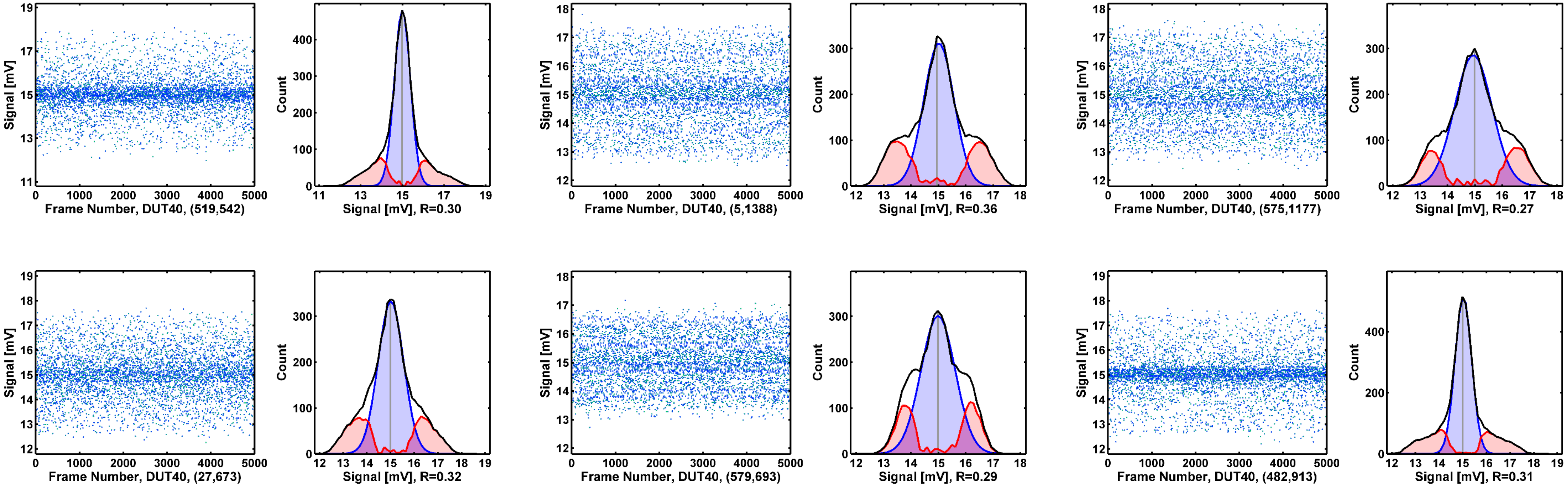
N_2: RTN & RTN-like devices

N_3: RTN with 2+ levels

N_4: RTN with 3+ levels

RTN-Like Behavior

- Noise waveforms of many devices do not show identifiable discrete levels
- If the noise histograms deviate significantly from Gaussian, we call them RTN-like
- They are likely RTN devices; several examples are shown below



Stress and Anneal

- Experimental conditions
  - Stress voltage (Vpix): 6.0 ~ 6.6V (6.0V for this report)
  - Stress: temperature = –35°C ~ 120°C, stress time = 10 ~ 780 min (–35°C for this report)
  - Anneal: temperature = 60°C ~ 240°C, anneal time = 10 ~ 360 min (240°C for this report)
  - Measure: room temperature (22°C) and nominal operation voltages
  - Sequence: measure → stress → measure; measure → anneal → measure
- Temperature effect of HCS
  - Long channel devices (L > 0.1um): more damage at lower temperature (SF W/L = 0.16u/0.87u)
  - Short channel devices (L < 0.1um): more damage at higher temperature

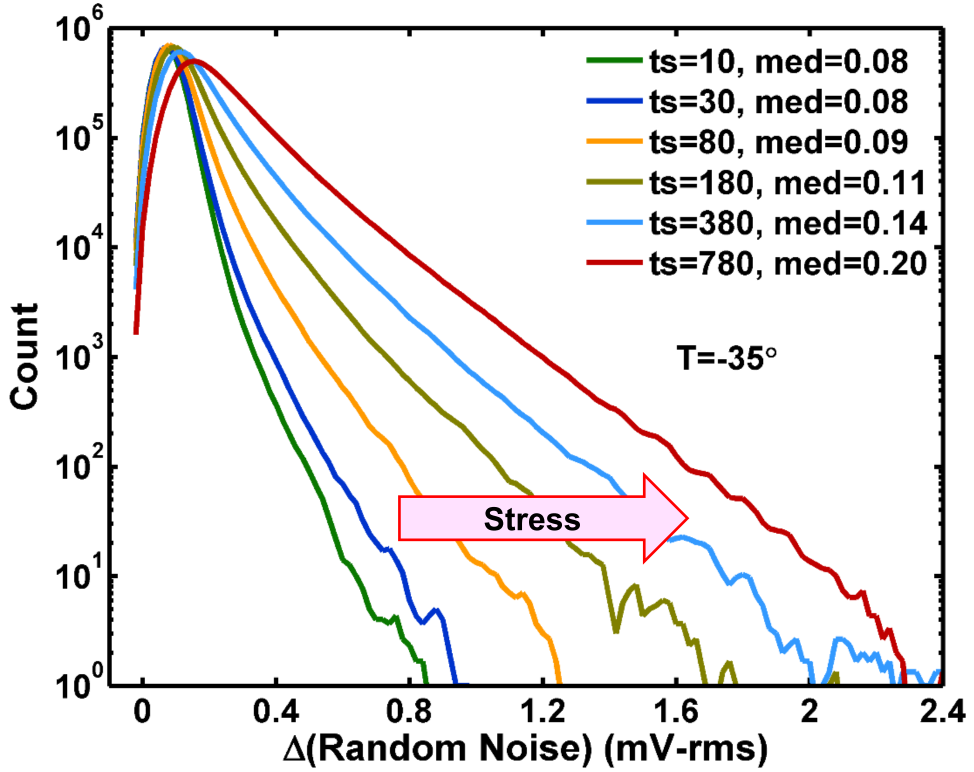
22°C Measure
–35°C, 10' Stress
22°C Measure
–35°C, 20' Stress
22°C Measure
•••
–35°C, 200' Stress
22°C Measure
–35°C, 400' Stress
22°C Measure

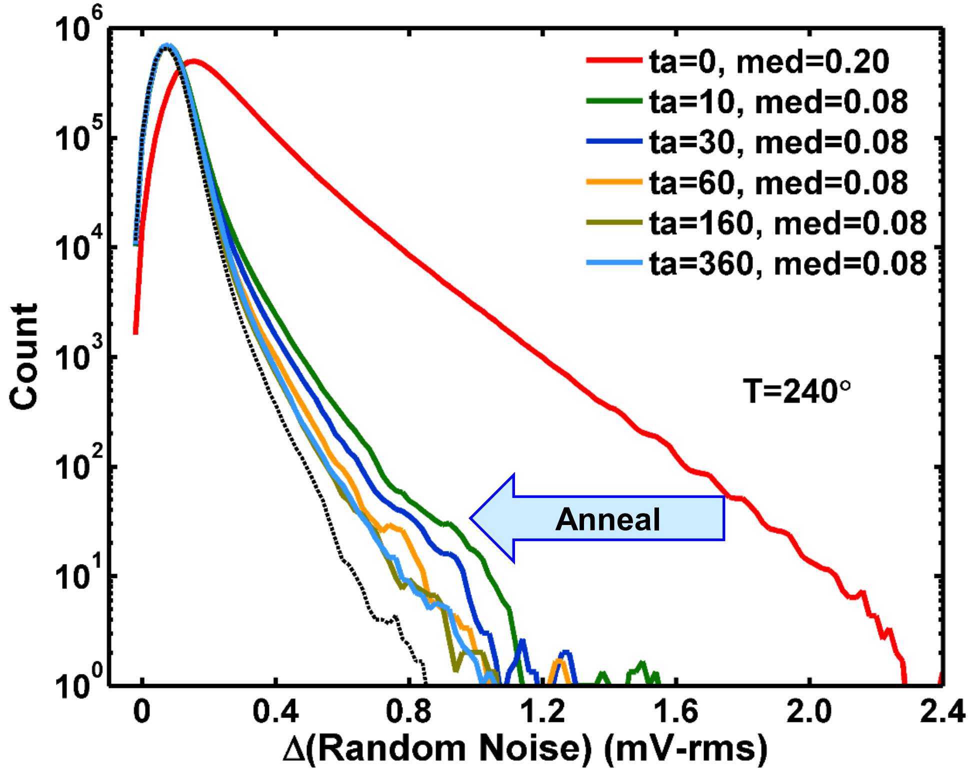
22°C Measure
240°C, 10' Anneal
22°C Measure
240°C, 10' Anneal
22°C Measure
•••
240°C, 100' Anneal
22°C Measure
240°C, 200' Anneal
22°C Measure

Power off during anneal

Changes of RN: Stress & Anneal (1)

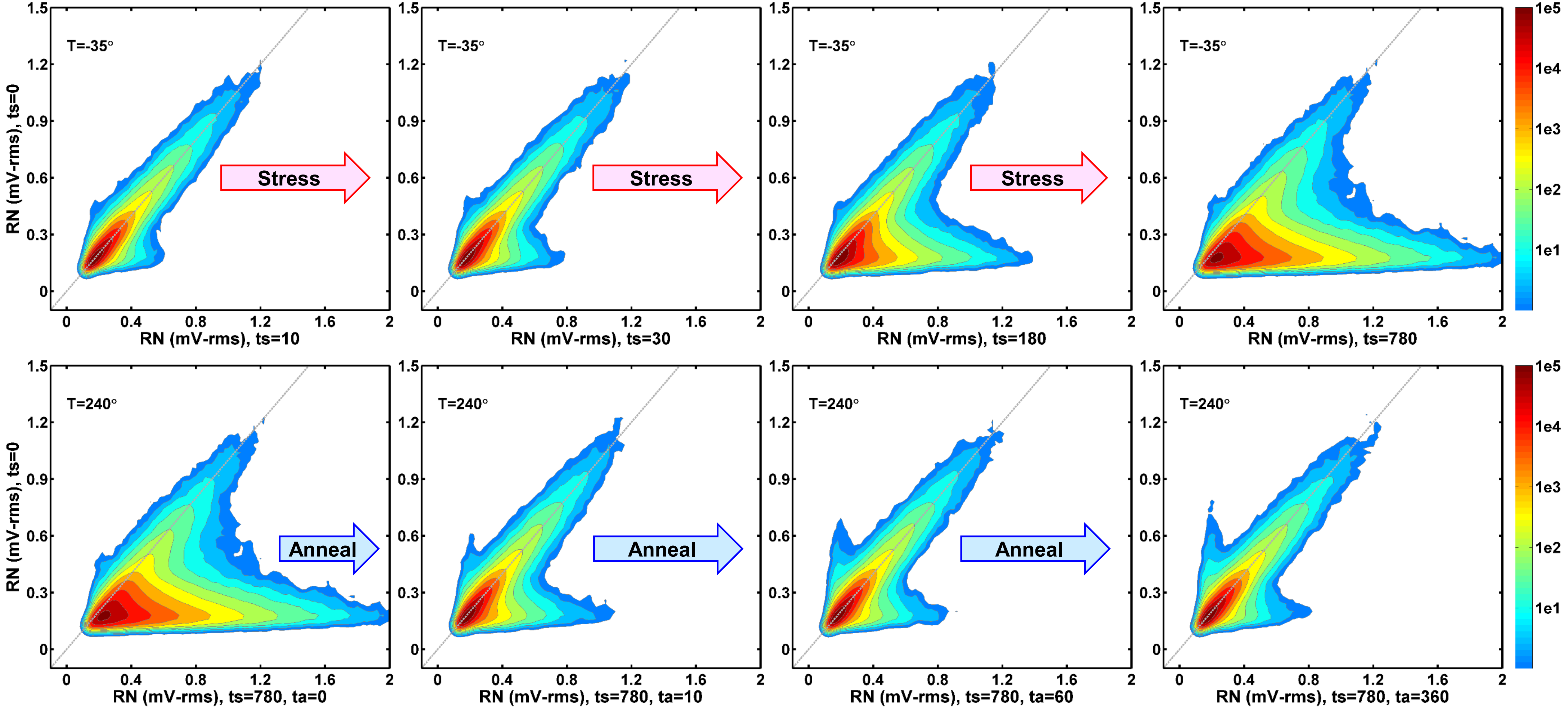
- **The increase of RN by hot-carrier stress is almost reversible by high-temperature anneal**
- **At 240°C anneal, the RN recovery in the first 10 min is substantial**
- **The Vt shift shows similar histograms, but different in details (Cf. IISW23, *Chao et al.*)**





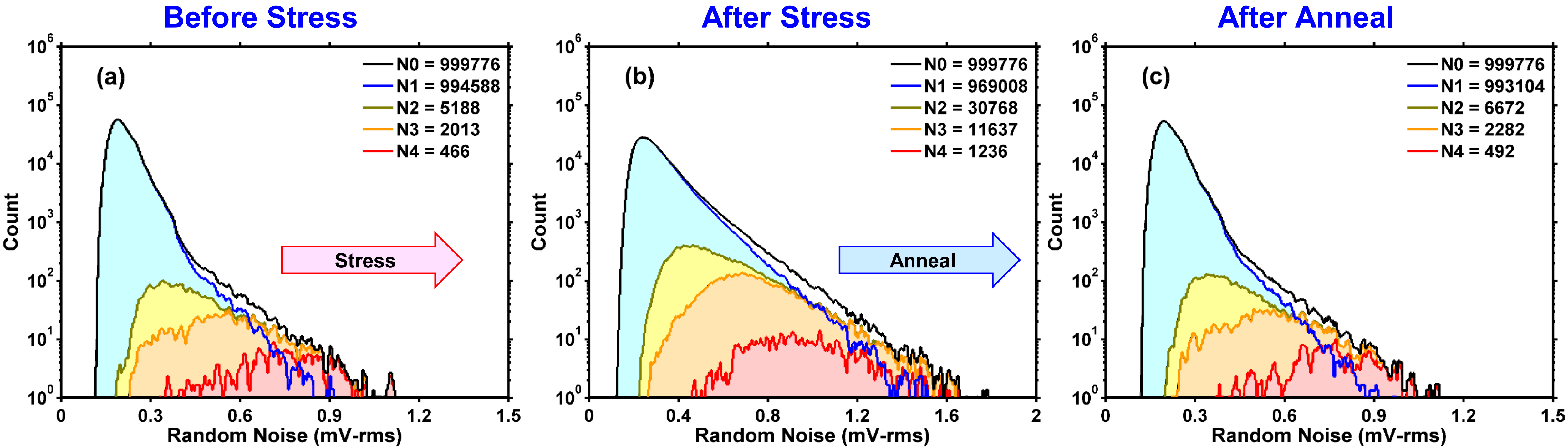
Changes of RN: Stress & Anneal (2)

- **The change of RN is not uniform, while the change of Vt shift is more uniform**



Changes of RN: Stress & Anneal (3)

- To see more details, we need to sort all pixels according to their noise waveforms
- RTN pixels are mostly located on the distribution tails
- Number of RTN & RTN-like pixels (N_2): 5,188 ➡ 30,768 (~6X increase) ➡ 6,672



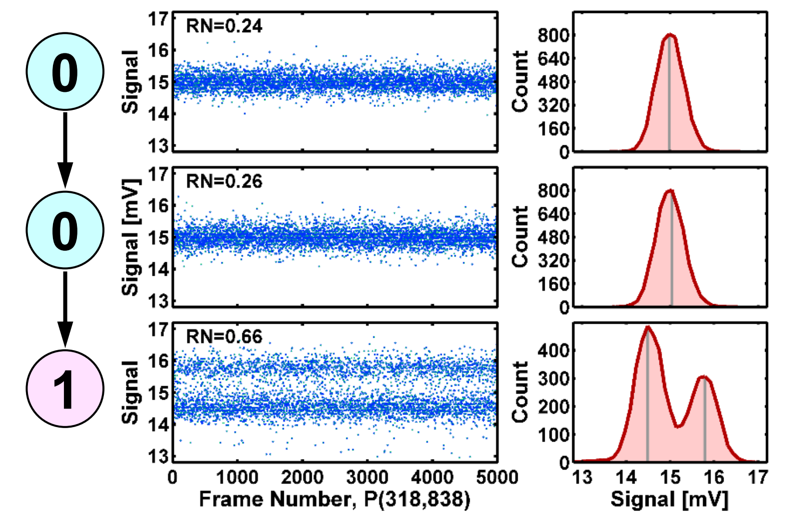
Observation 1

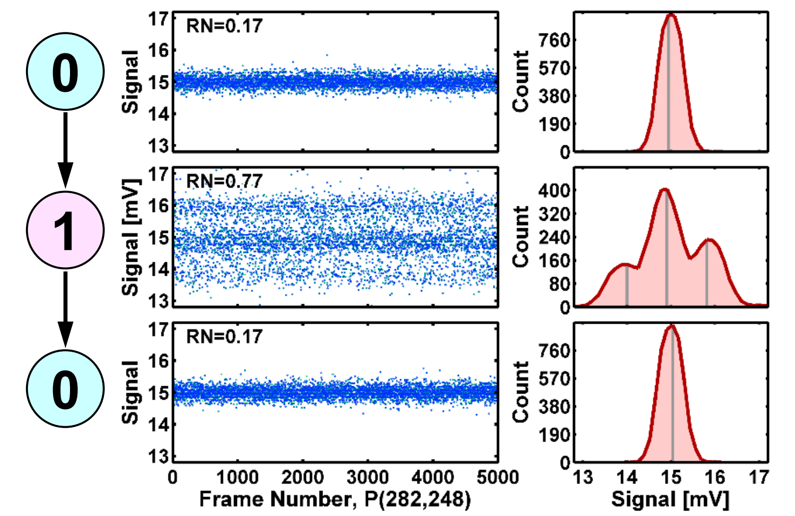
- **Real data are more complicated than expected**
  - **Stress can not only turn non-RTN devices into RTN devices but also turn RTN into non-RTN**
  - **Anneal can not only turn RTN devices into non-RTN devices but also turn non-RTN into RTN**
- **We can find examples for each of the 8 combinations**
  - **Cases 111 & 000 are not interesting (no change) but the other 6 cases are interesting**

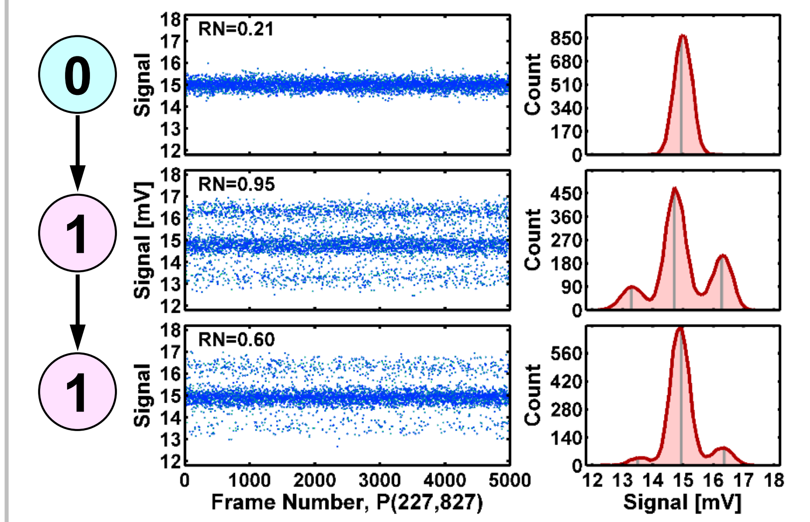
1 ➡ RTN
0 ➡ non-RTN

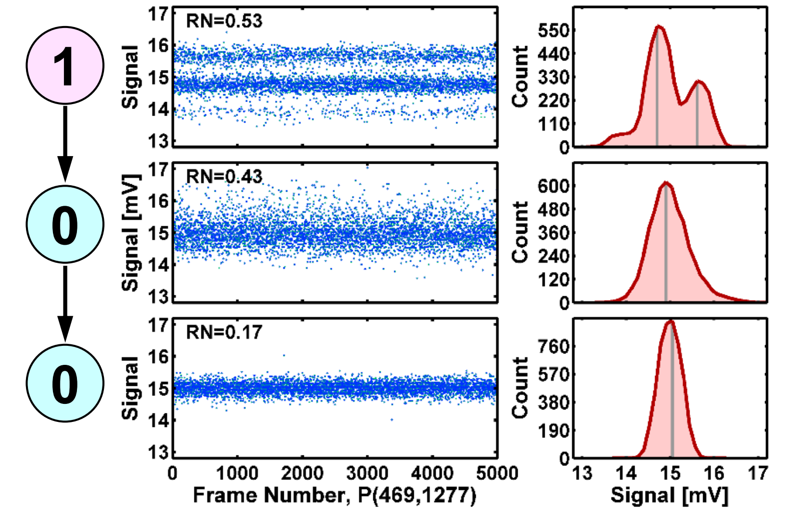
Case	Before Stress	After Stress	After Anneal
111	RTN	RTN	RTN
110	RTN	RTN	Non-RTN
101	RTN	Non-RTN	RTN
100	RTN	Non-RTN	Non-RTN
011	Non-RTN	RTN	RTN
010	Non-RTN	RTN	Non-RTN
001	Non-RTN	Non-RTN	RTN
000	Non-RTN	Non-RTN	Non-RTN

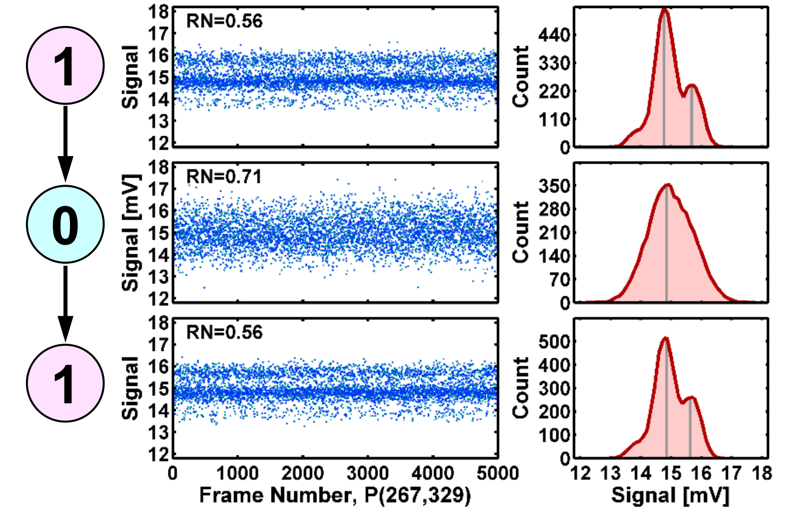
Examples of Each Case

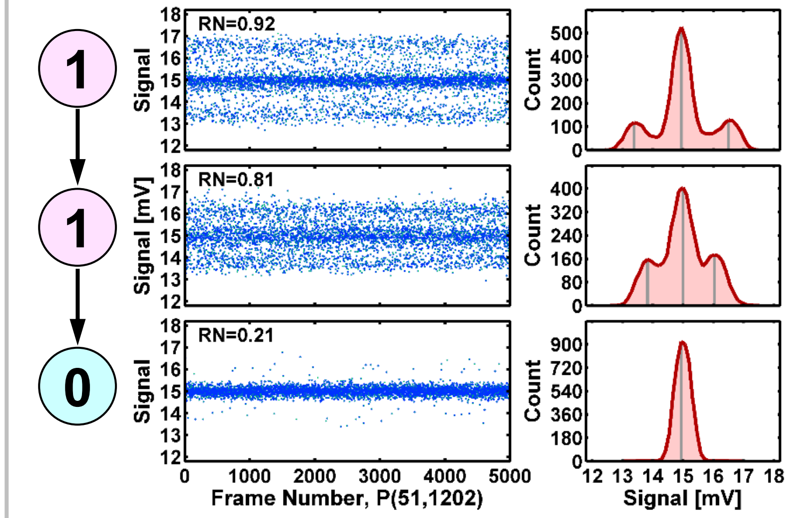












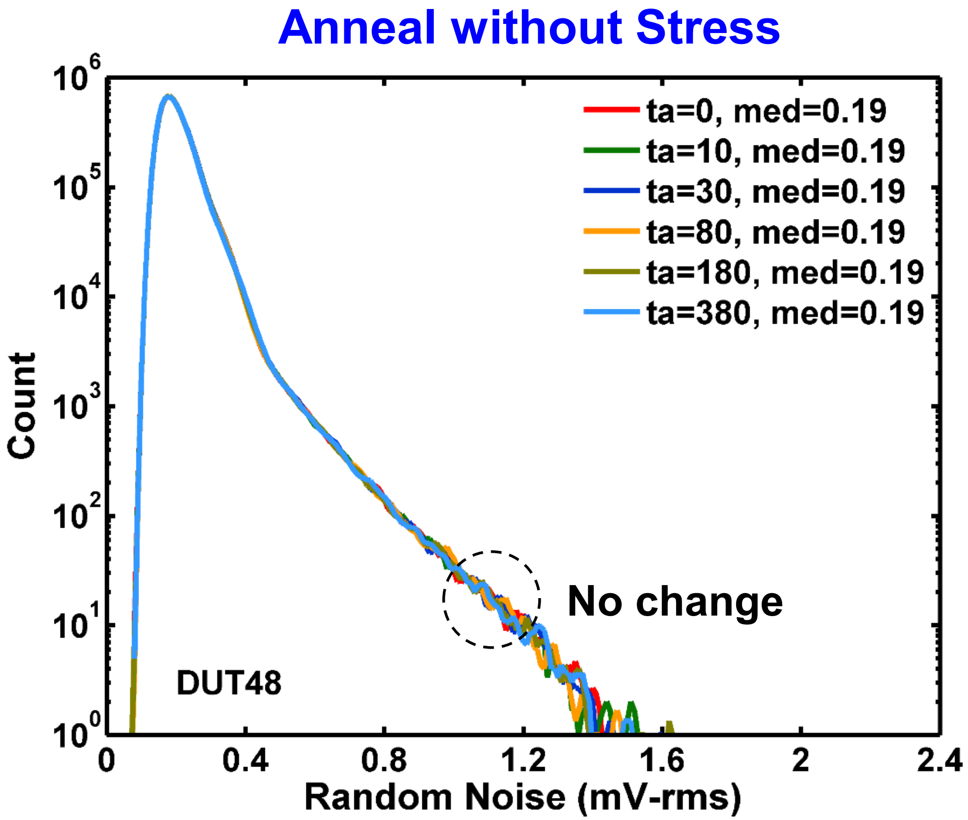
Observation 2

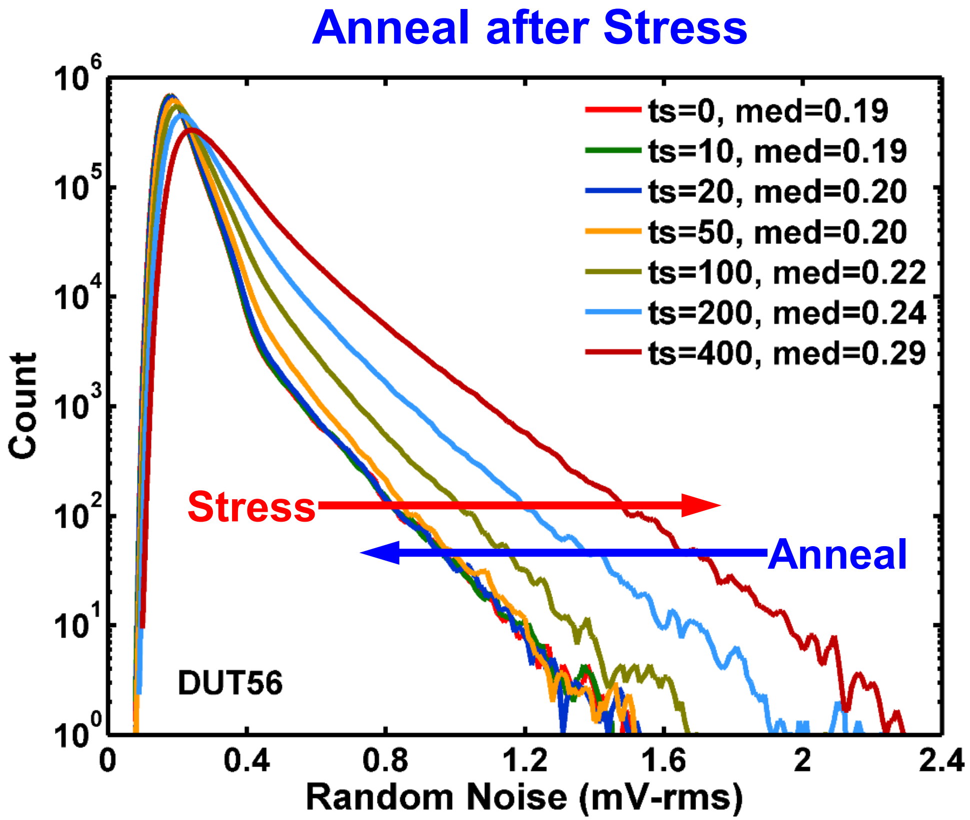
- The most interesting and dominant case is Case 010: RTN generation & recovery
- The HC stress turned a large number (28,388) of non-RTN devices into RTN devices
- After high temperature anneal, 98% of these RTN devices recovered back to non-RTN

Before Stress		After Stress		After Anneal	
RTN-like, K_1	5,188	RTN-like, K_{11}	2,380	RTN-like, K_{111}	2,314
				Non-RTN, K_{110}	66
		Non-RTN, K_{10}	2,808	RTN-like, K_{101}	2,047
				Non-RTN, K_{100}	761
Non-RTN, K_0	994,588	RTN-like, K_{01}	28,388	RTN-like, K_{011}	532
				Non-RTN, K_{010}	27,856
		Non-RTN, K_{00}	966,200	RTN-like, K_{001}	1,779
				Non-RTN, K_{000}	964,421

Observation 3

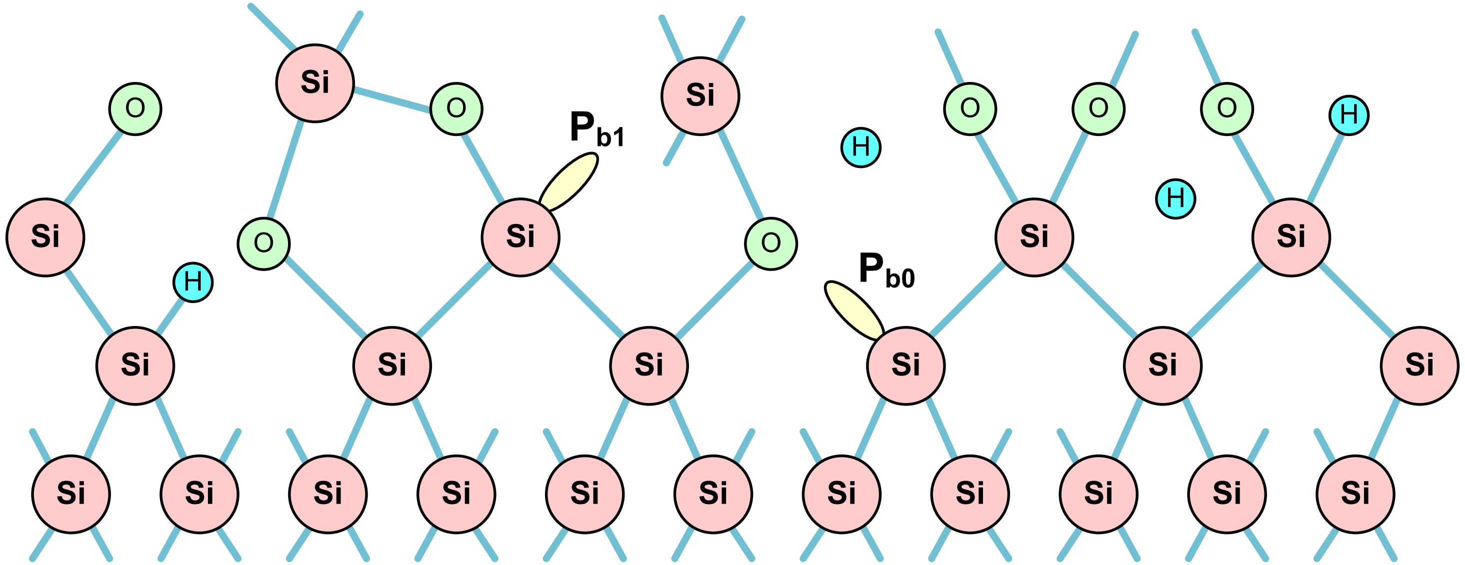
- **Anneal w/o stress**: RN distribution and RTN tailing almost unchanged ➡ **Hard RTN traps**
  - Wafers were high-temperature annealed in BEOL process ➡ many soft RTN traps already recovered
- **Anneal after stress**: stress generated RTN traps can recover after anneal ➡ **Soft RTN traps**
- Implication: the hard and soft RTN traps are physically different





Discussion

- One theory on generation-annealing of RTN traps
  - Hydrogen-related chemicals are abundant in semiconductor fabrication processes
  - Generation of RTN may be due to the breaking of a Si-H bond & creating a Si dangling bond
  - Annealing of RTN may be due to passivation of a dangling bond by hydrogen
- Many other possibilities …
  - Subtle change in trap atomic structure may activate or deactivate the trap
- Not clear why some RTN traps can be annealed easily but others cannot be



Si dangling bonds

P_{b0} center: Si bonded to 3 Si atoms

P_{b1} center: Si bonded to 1 O & 2 Si atoms

Si-H bond dissociation energy ~3.6 eV

Conclusions

- RTN degradation can be a good device aging monitor
  - In addition to Vt shift and mobility degradation
- RTN may be generated by process-induced damage (PID) or hot carrier stress (HCS)
- HCS induces worse damage at lower temperature for long-channel devices
  - Longer carrier lifetime at lower temperature for long-channel devices
  - Opposite trend for short-channel devices
- The HCS generated RTN traps can recover by high-temperature anneal (“Soft RTN”)
- The PID induced RTN traps are not affected by high-temperature anneal (“Hard RTN”)
- The nature of the differences between soft and hard RTN is unclear
- Physics of generation & recovery of RTN trap is not completely understood
- Any study on RTN must be statistical over large sample sizes