R9.2

THE UNIVERSITY of EDINBURGH
Institute for Integrated Micro and Nano Systems

Over 2 Million Frames per Second 128×128 Macropixel 3D-Stacked Burst SPAD-Based Image Sensor

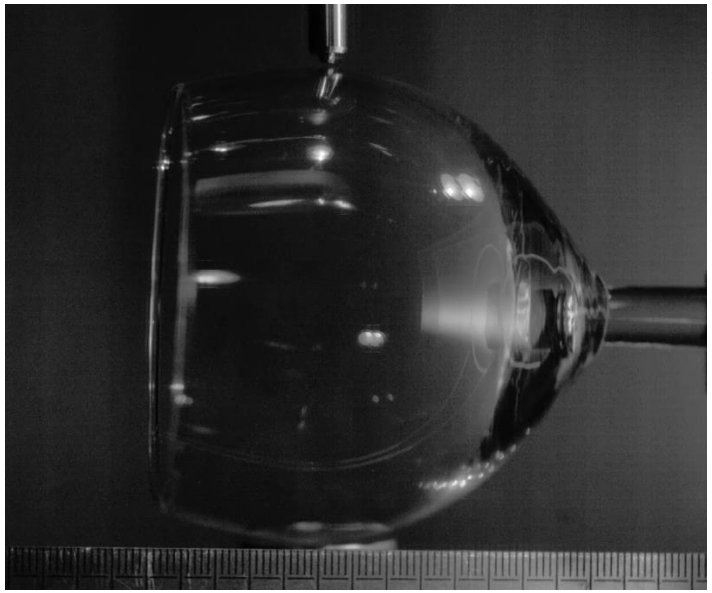
Yuanyuan Hua[1], Maciej Wojtkiewicz[1,2], Francescopaolo Mattioli Della Rocca[1,3], Ahmet T Erdogan[1], Lars Fisher[1], Robert K Henderson[1]

[1] The University of Edinburgh, Edinburgh, United Kingdom
[2] Now with Photon Force, Edinburgh, United Kingdom
[3] Now with Sony EUTDC, Trento, Italy

Engineering and Physical Sciences Research Council

Transient phenomena occurring at extremely short timescales

33k fps



G. Cai et al, A 1.3M Pixel 34,700fps Global-Shutter BSI Imager with HDR and Motion Blur Suppression Capability, IISW, 2021

76k fps

D. Van Blerkom et al, A 1Mpixel, 80k fps Global Shutter CMOS Image Sensor for High Speed Imaging, IISW, 2021

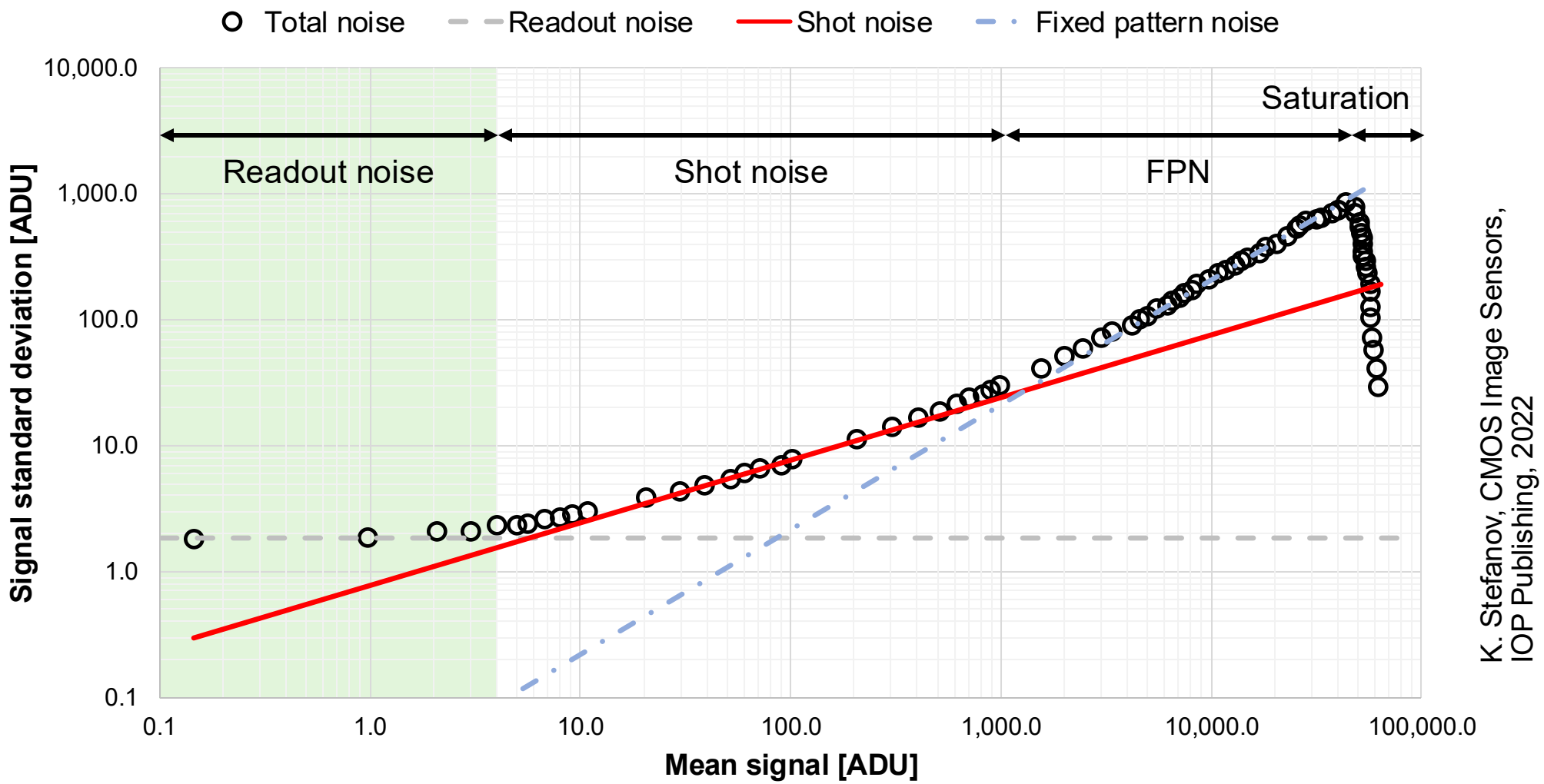
5M fps

https://www.youtube.com/watch?v=DxW23n8kid8 and S. Shigetoshi et al., A 20 Mfps global shutter CMOS image sensor with improved sensitivity and power consumption, IISW, 2015

Due to ultra-short integration times, high-speed imaging is often also low-light imaging.

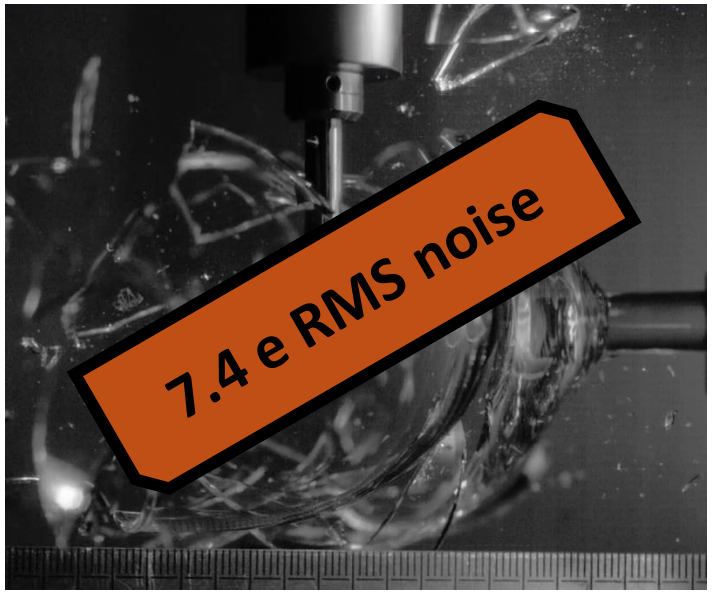
Low Number of Photons

Photon Transfer Curve (CIS)



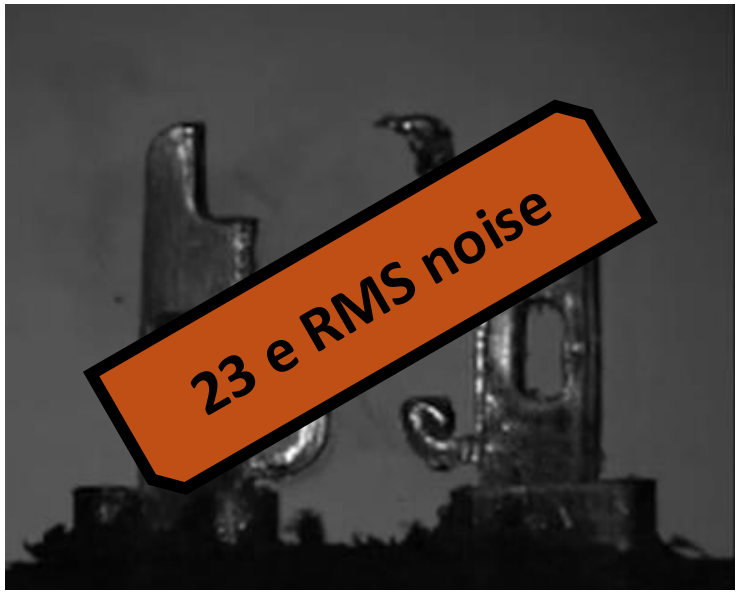
Transient phenomena occurring at extremely short timescales

33k fps



G. Cai et al, A 1.3M Pixel 34,700fps Global-Shutter BSI Imager with HDR and Motion Blur Suppression Capability, IISW, 2021

76k fps



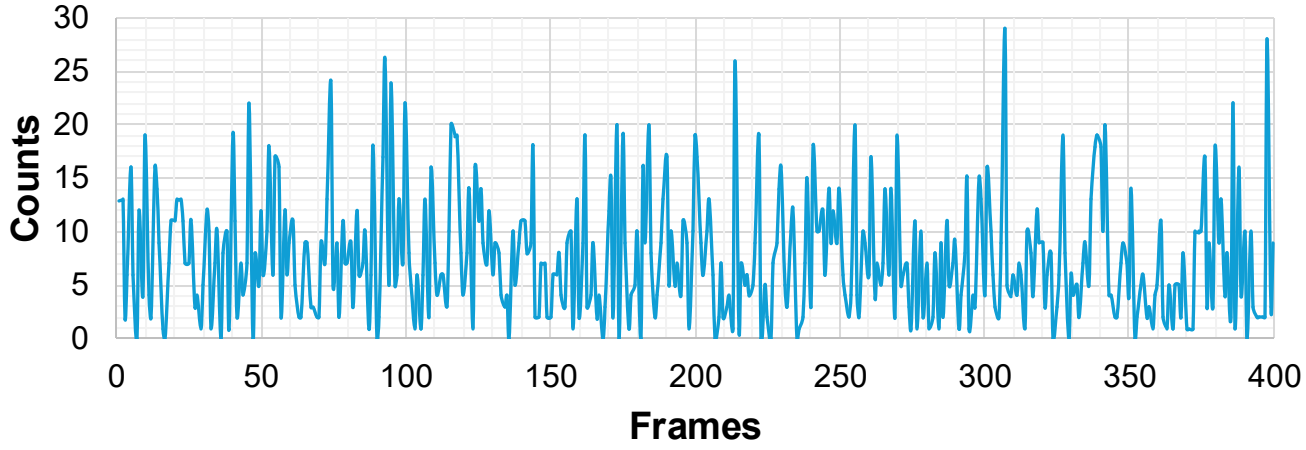
D. Van Blerkom et al, A 1Mpixel, 80k fps Global Shutter CMOS Image Sensor for High Speed Imaging, IISW, 2021

5M fps

https://www.youtube.com/watch?v=DxW23n8kid8 and S. Shigetoshi et al., A 20 Mfps global shutter CMOS image sensor with improved sensitivity and power consumption, IISW, 2015

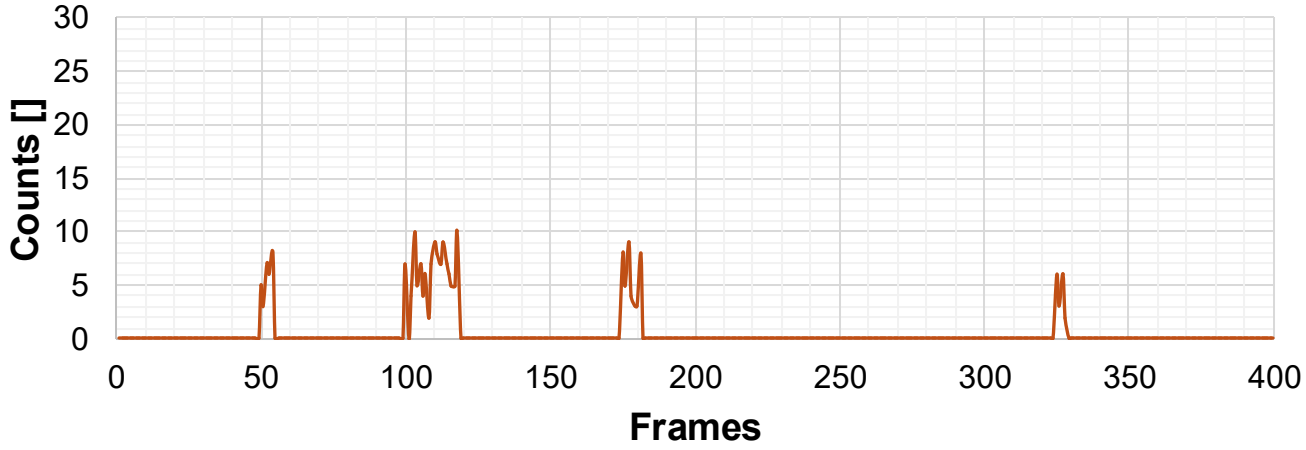
Readout Noise in Photon-Starved Imaging

Analogue CIS



- 10 e RMS readout noise is simulated without any input signal.
- A signal of 5 photons is added at four time instances.

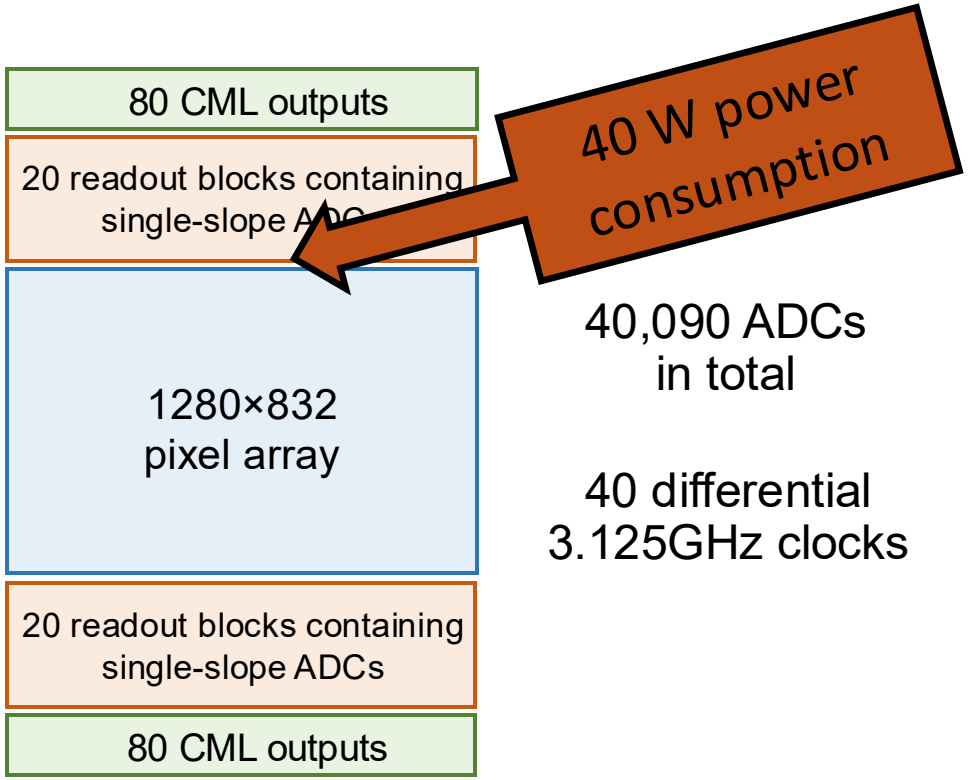
SPAD



- Zero readout noise.
- Signal is signified at four time instances.

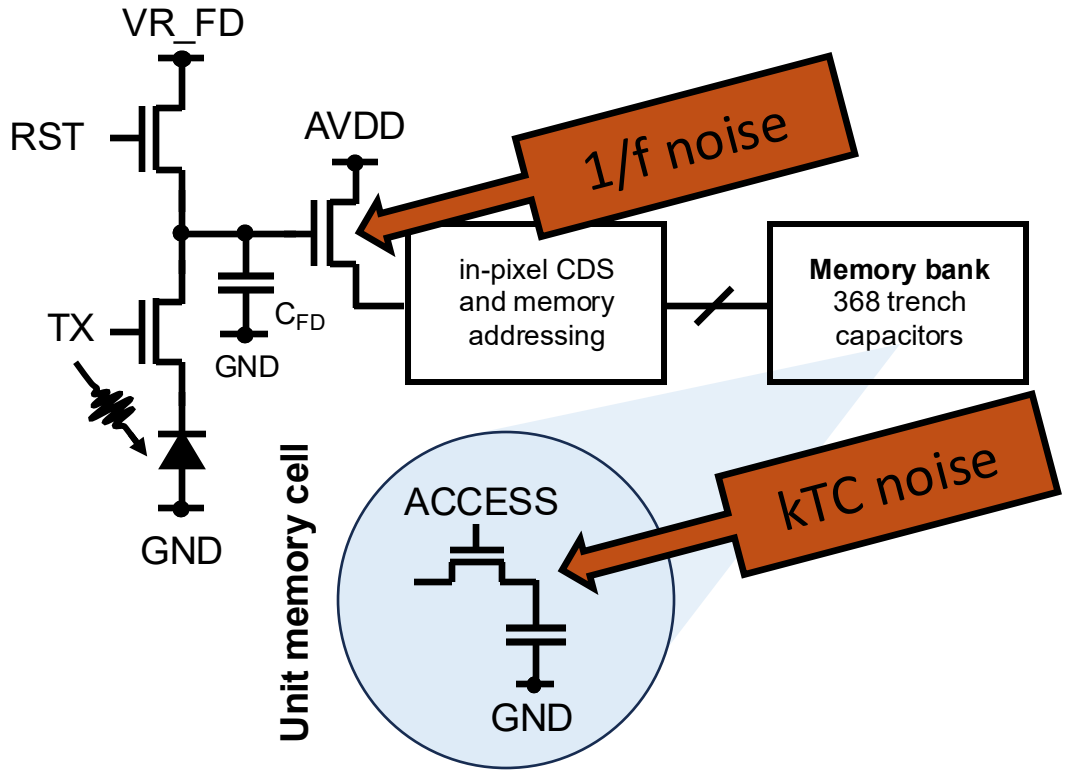
State-of-the-Art High-Speed CIS Design Techniques

Massively-Parallelized Readout and ADCs



D. Van Blerkom et al, A 1Mpixel, 80k fps Global Shutter CMOS Image Sensor for High Speed Imaging, IISW, 2021

368-Frames Burst Capture Pixel

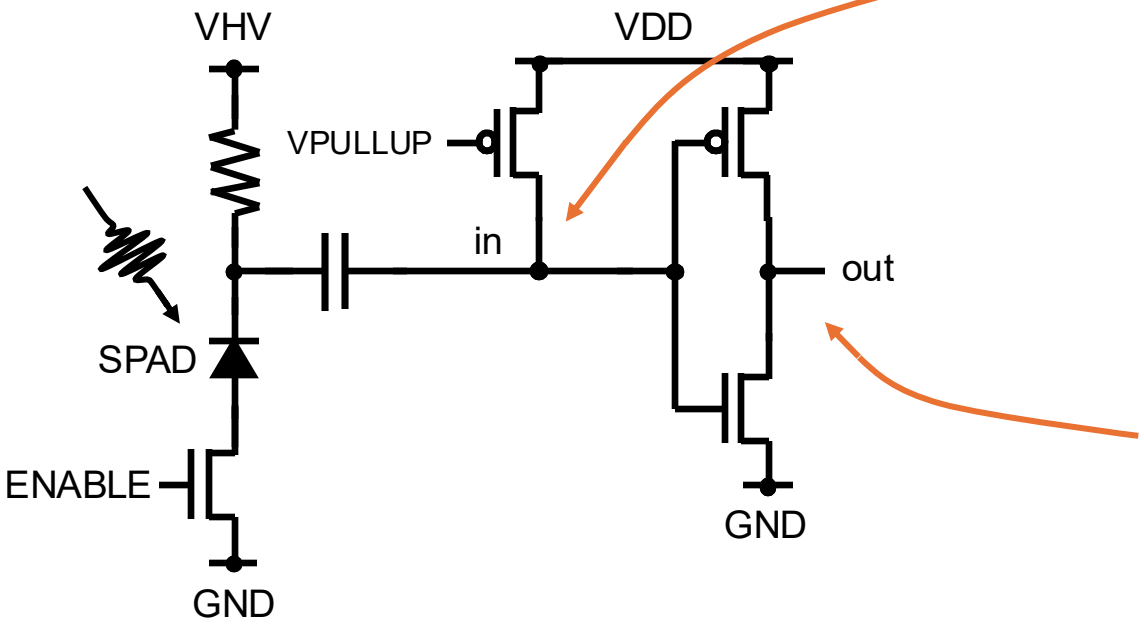


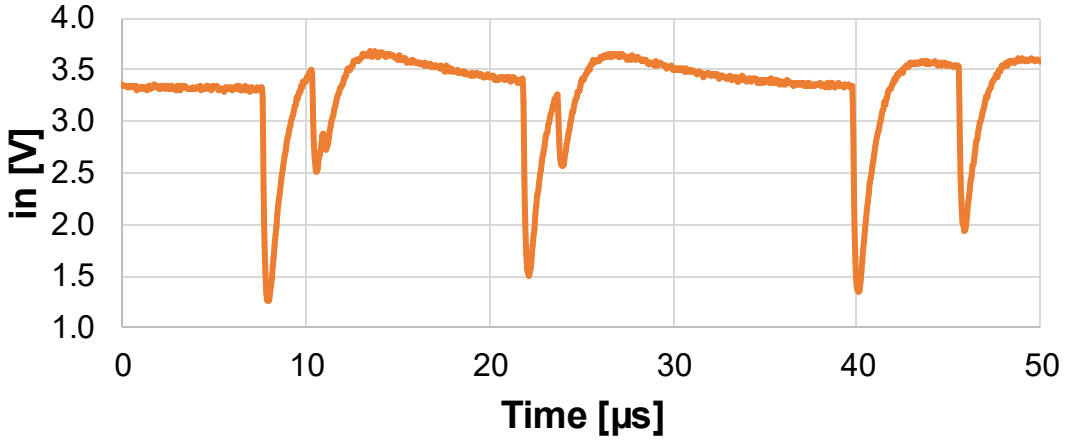
S. Manabu, Over 100 Million Frames per Second 368 Frames Global Shutter Burst CMOS Image Sensor with In-pixel Trench Capacitor Memory Array, IISW, 2019

SPAD-Based Imaging

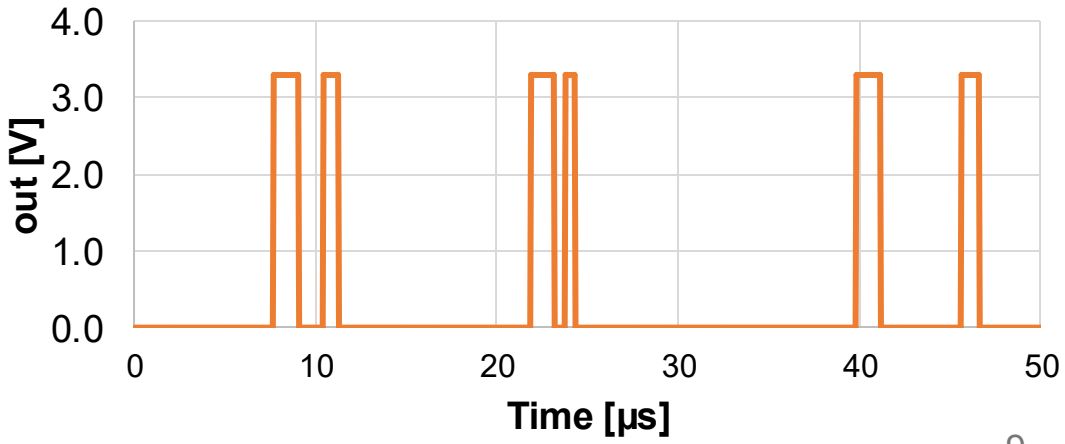
- Detection of single photons via avalanche multiplication.
- The avalanche is sensed by a frontend circuit and then quenched by a resistor.

No readout noise



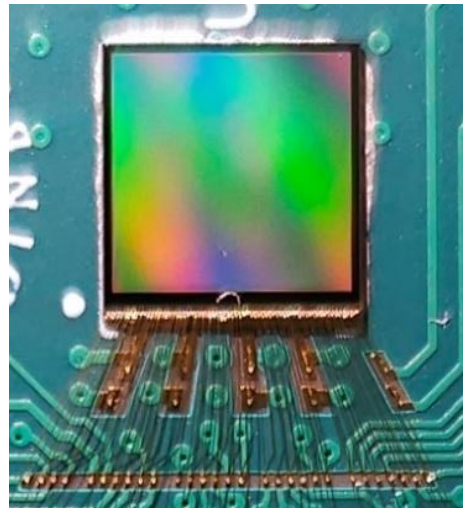


- Rising edge signals the arriving photon.

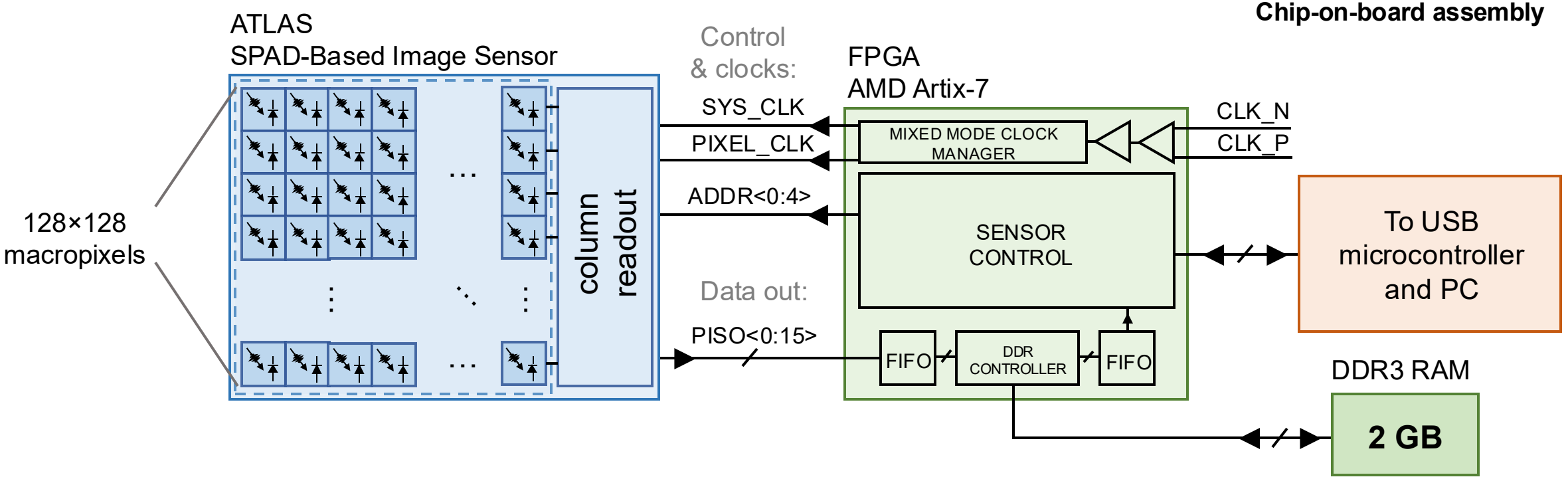


128×128 Macropixel SPAD Sensor and Camera

- 3-D-stacked back-side illuminated SPAD 512×512 SPAD imager.
- Sensor and the camera system capable of 2.18M fps burst imaging.
- Manufactured in STMicroelectronics' 3D40SPAD process.

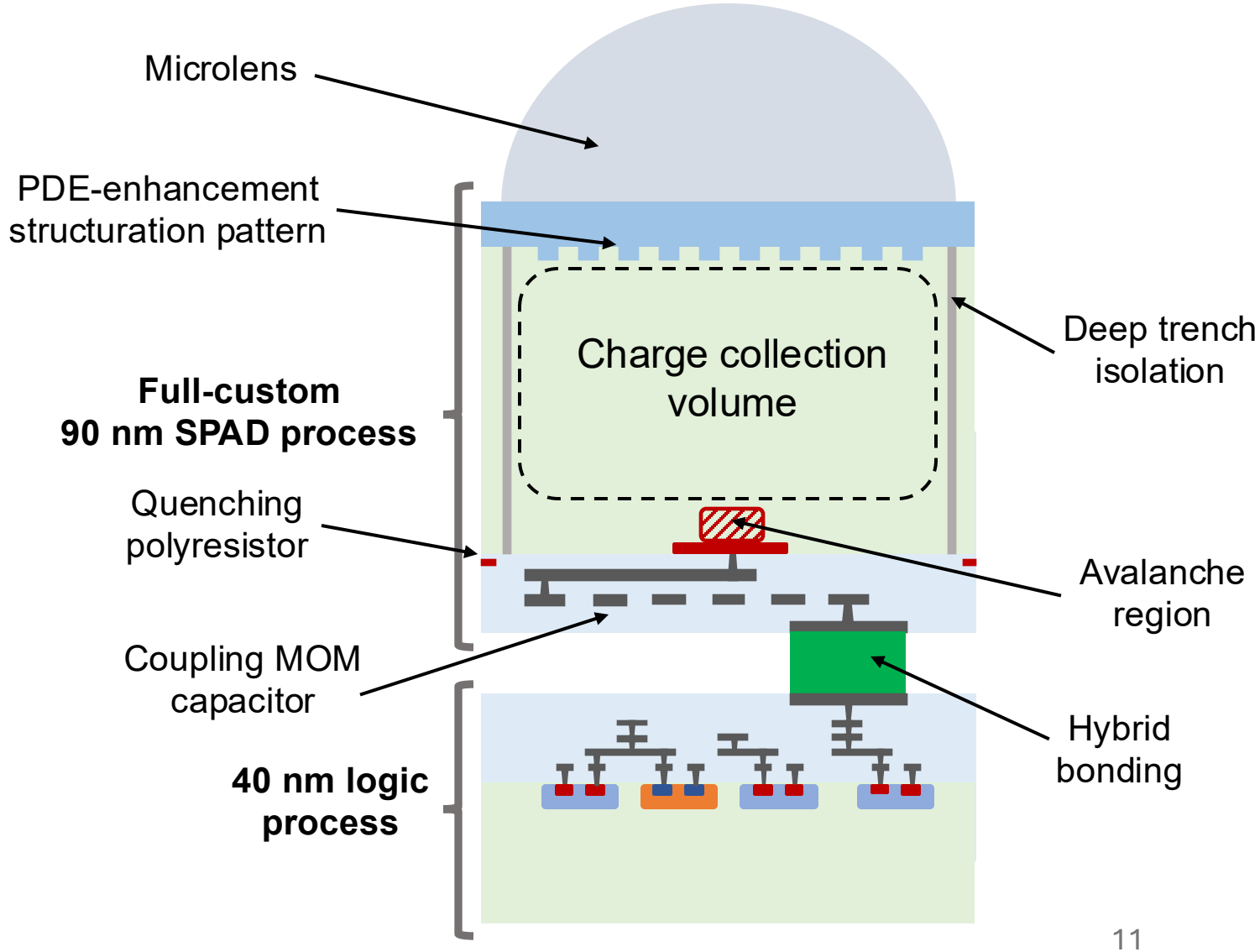


Chip-on-board assembly



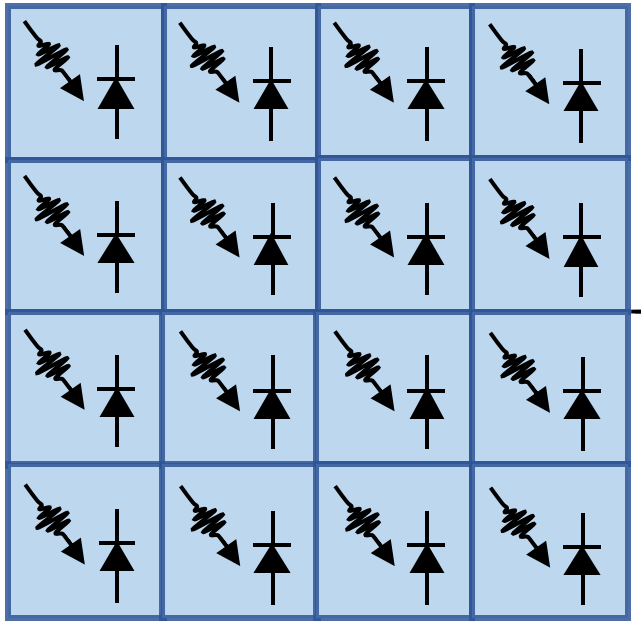
3-D-Stacked SPAD (Peak PDE=55%)

- Two wafers for light sensing and signal processing are made in two independently optimized processes.
- Top tier contains the SPAD device, quenching resistor and AC-coupling capacitor.
- Bottom tier contains CMOS transistors.
- Approx. 100% fill factor and low DCR are achieved while complex circuits can be integrated within the pixel.

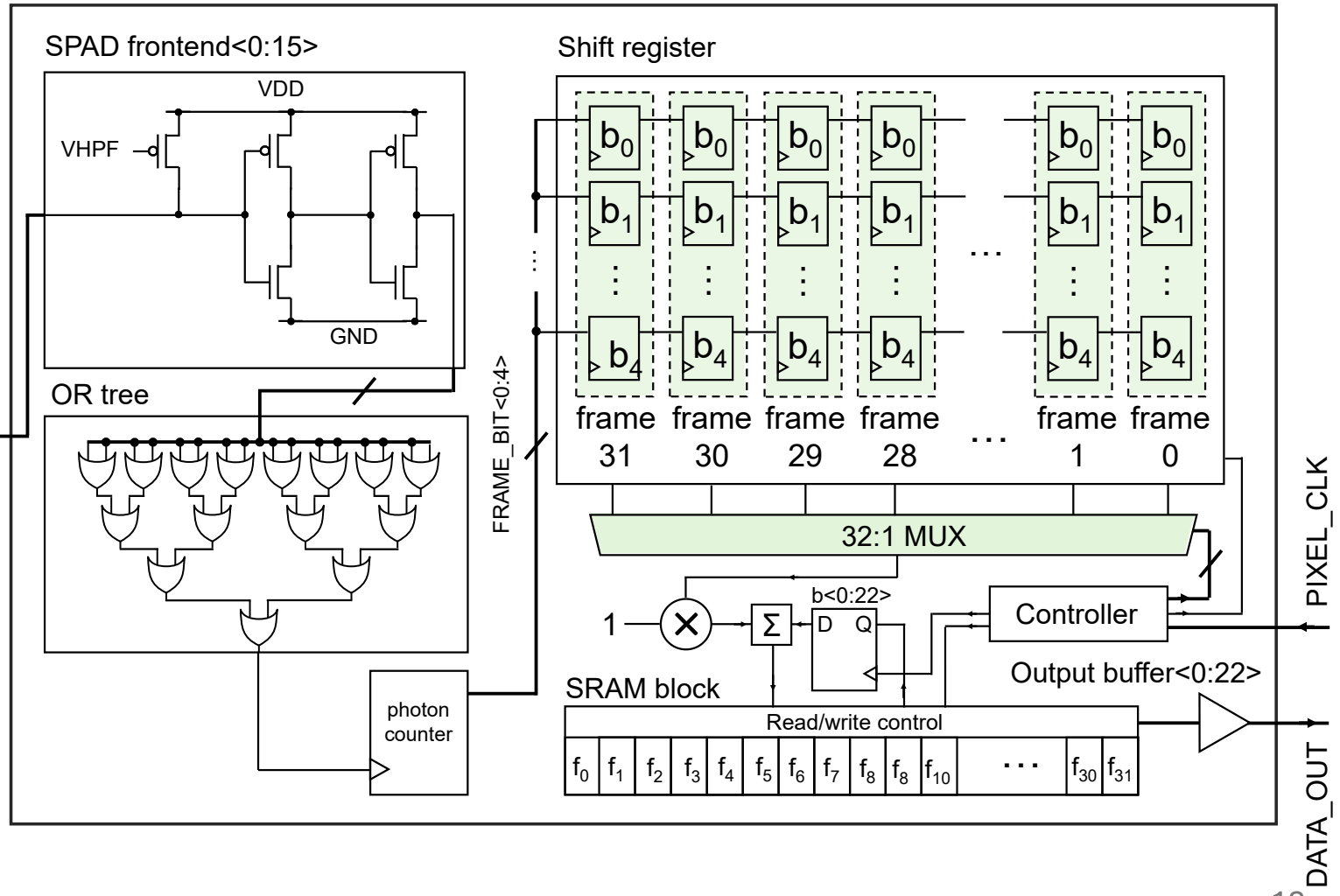


Macropixel Architecture

Top tier:
passively-quenched SPADs



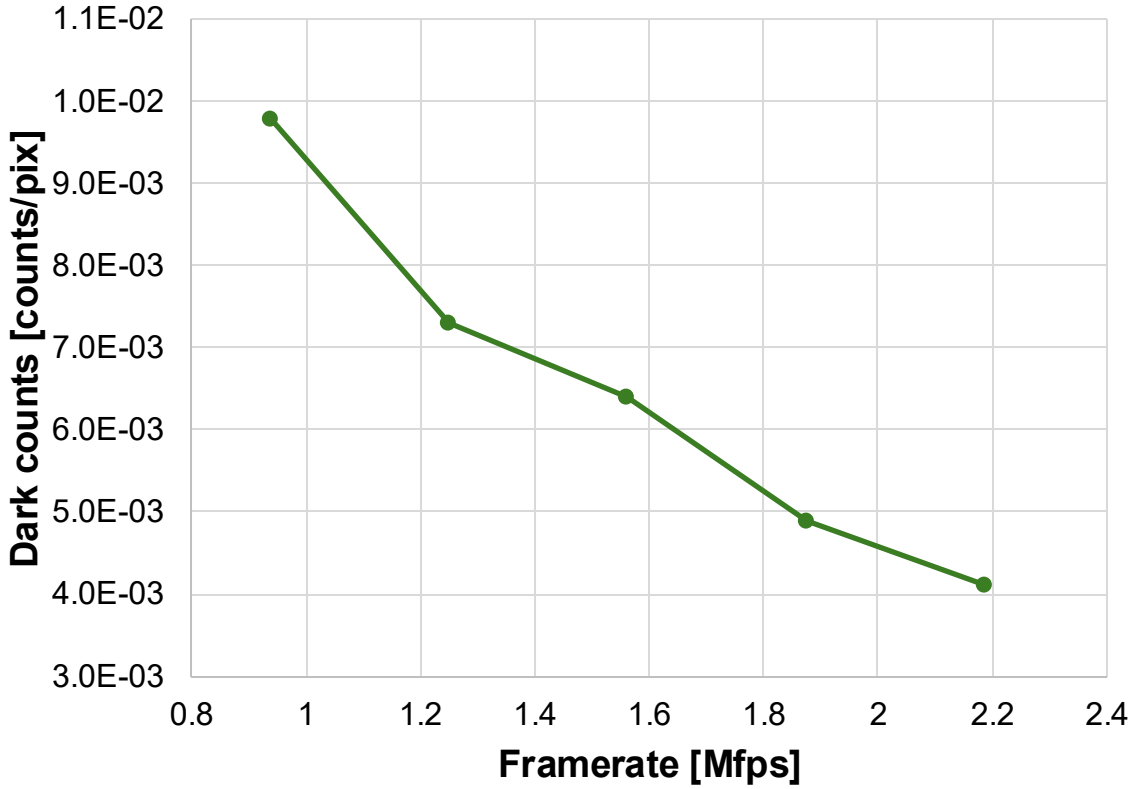
Bottom tier: pixel logic circuits



Characterization

1. Dark Counts vs. Framerate
2. Transfer Curve
3. LED Imaging
4. LED Blinking Test
5. High Speed Air Blaster

DCR vs. Framerate



Measurement Conditions:

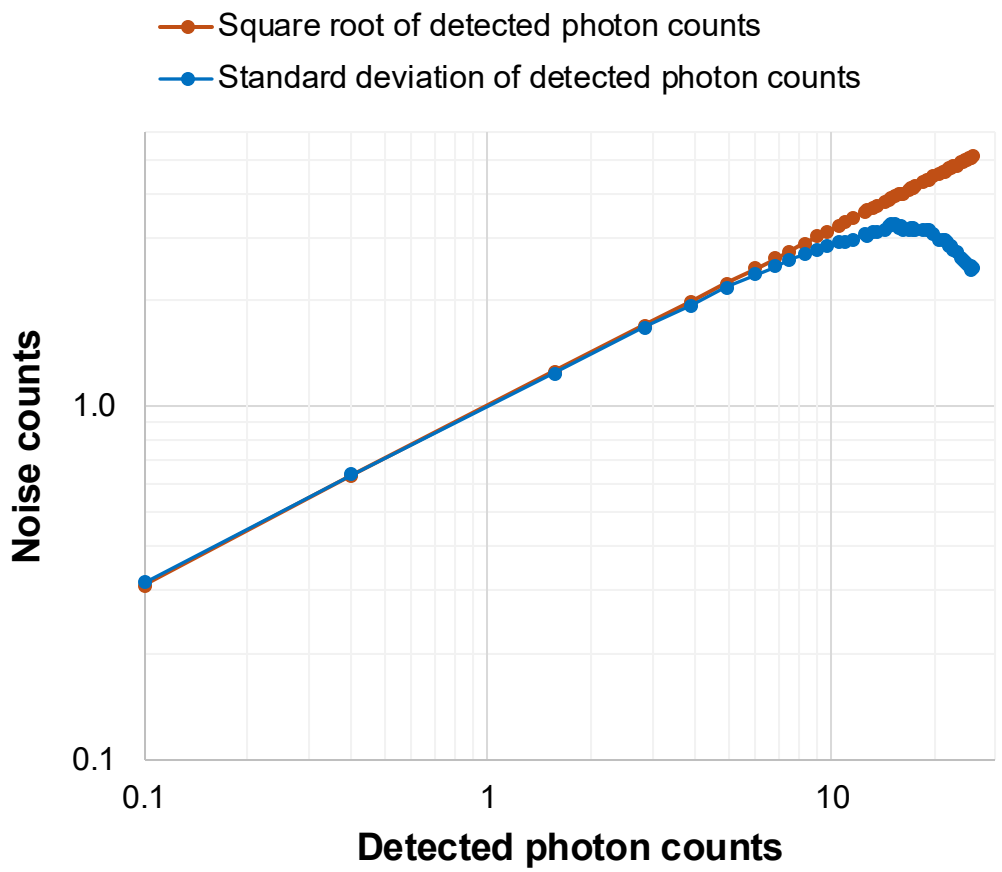
- Room temperature
- Complete light shielding
- 100 frames for each point
- Each point is averaged over 1,638,400 pixels

Shorter integration times are reducing thermally generated noise events in one frame

» Dark counts decrease as framerate increases

Noise Measurement

$$\sigma_{total}^2 = \sigma_{shot}^2 + \sigma_{readout}^2$$



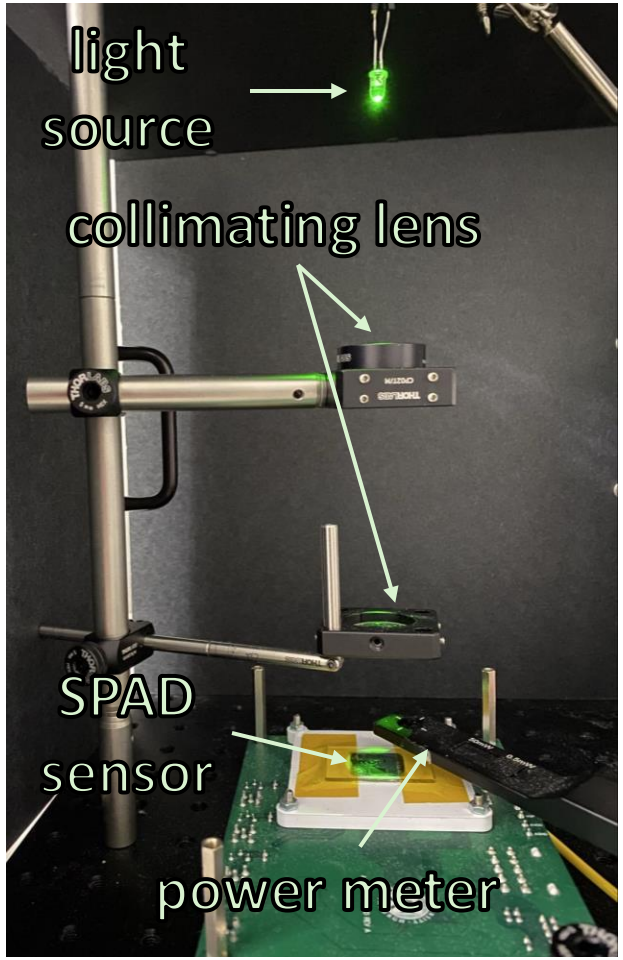
No slope-zero regime observed

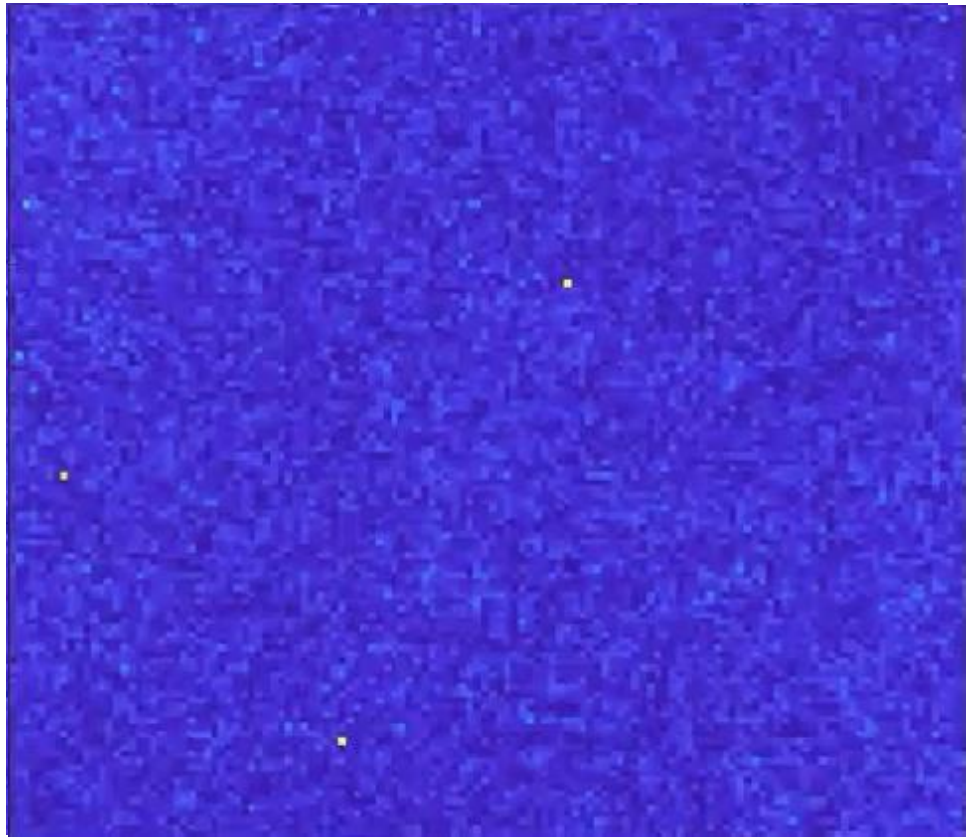
Measurement Conditions:

- Room temperature
- Power meter is applied to ensure linear photon counts increase
- Captured at 2.18 Mfps using collimated light
- 20 consecutive frames for each point
- Each point is calculated from 1,638,400 pixels

No readout noise, shot noise is the only limitation

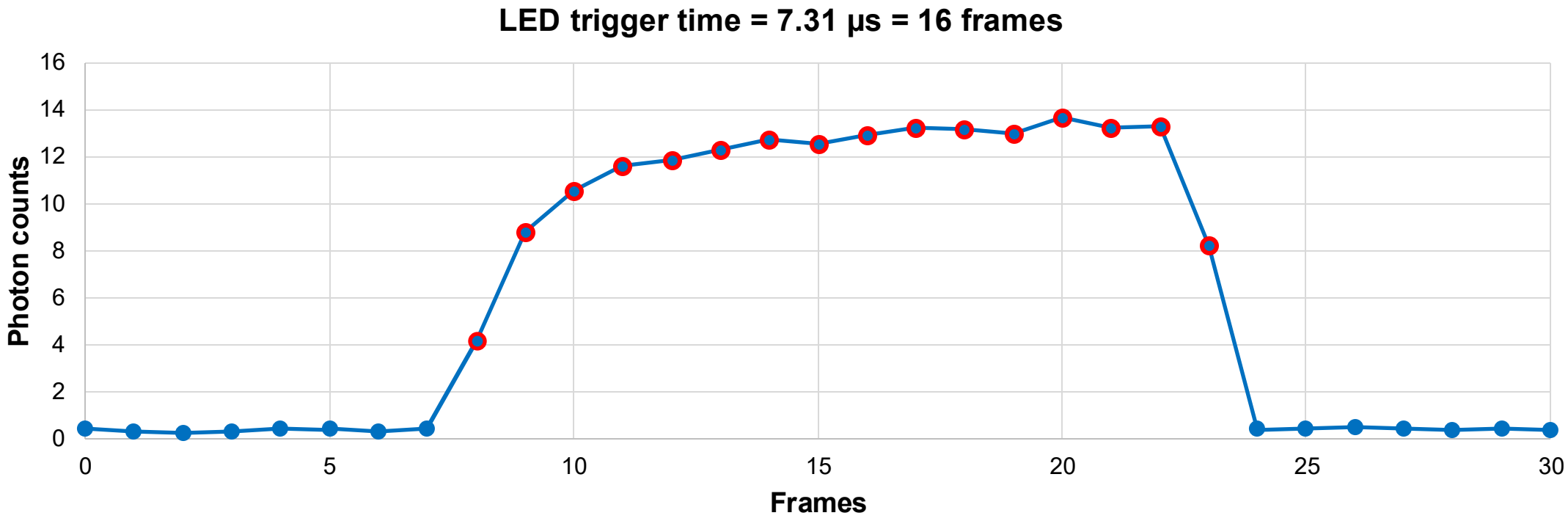
System Functionality Test





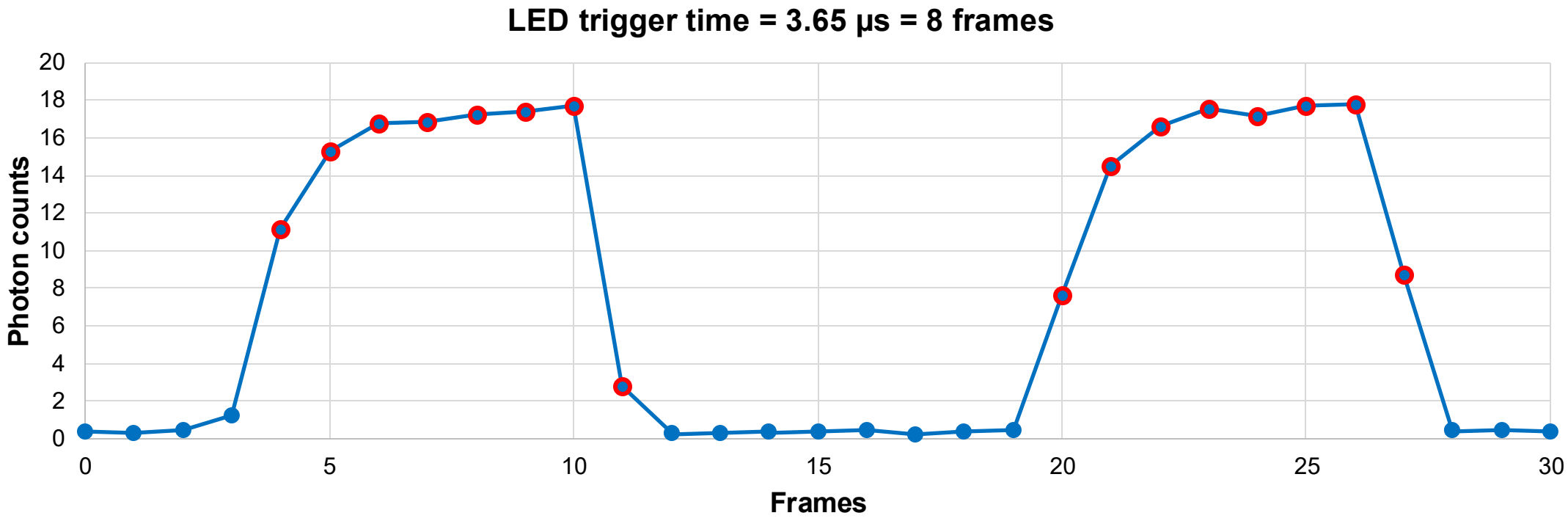
378 kHz LED @ 625k fps

Experiment Proving 2.18M fps Framerate



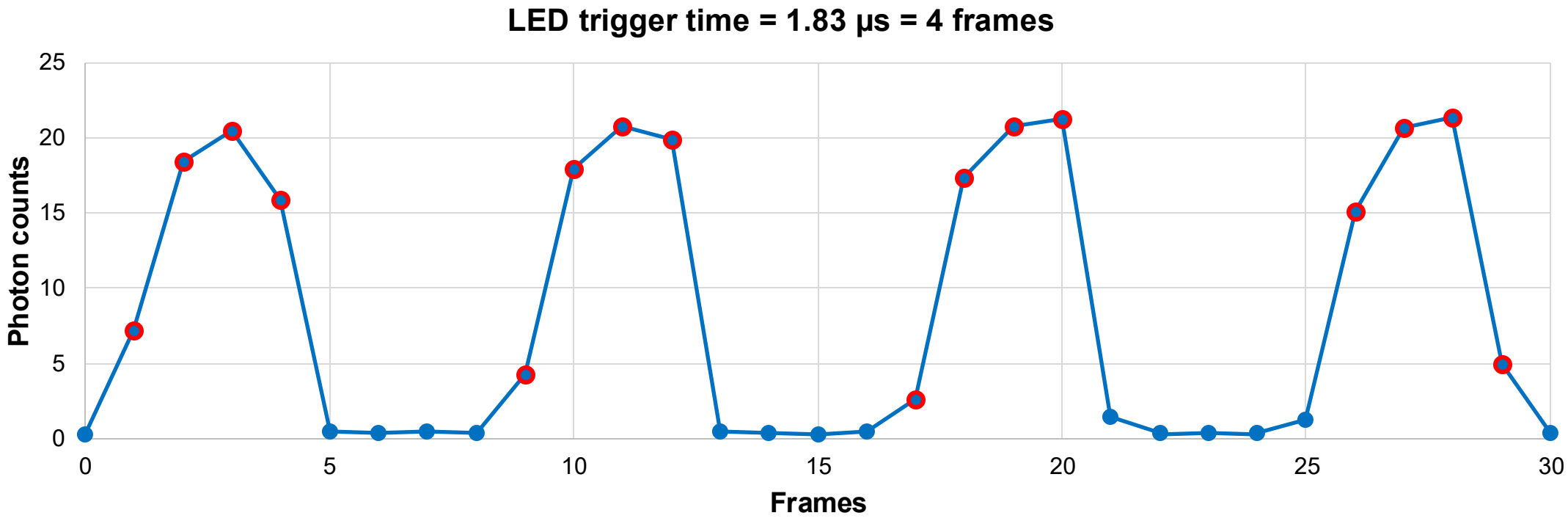
LED blinking frequency: 68 kHz

Experiment Proving 2.18M fps Framerate



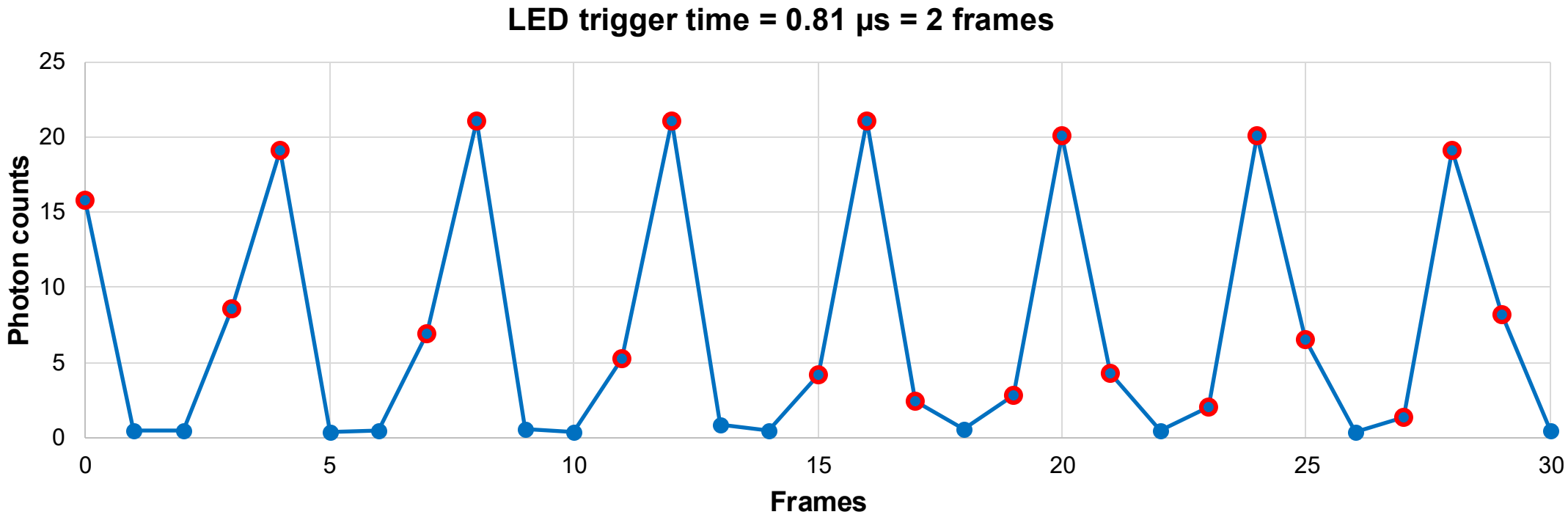
LED blinking frequency: 136 kHz

Experiment Proving 2.18M fps Framerate



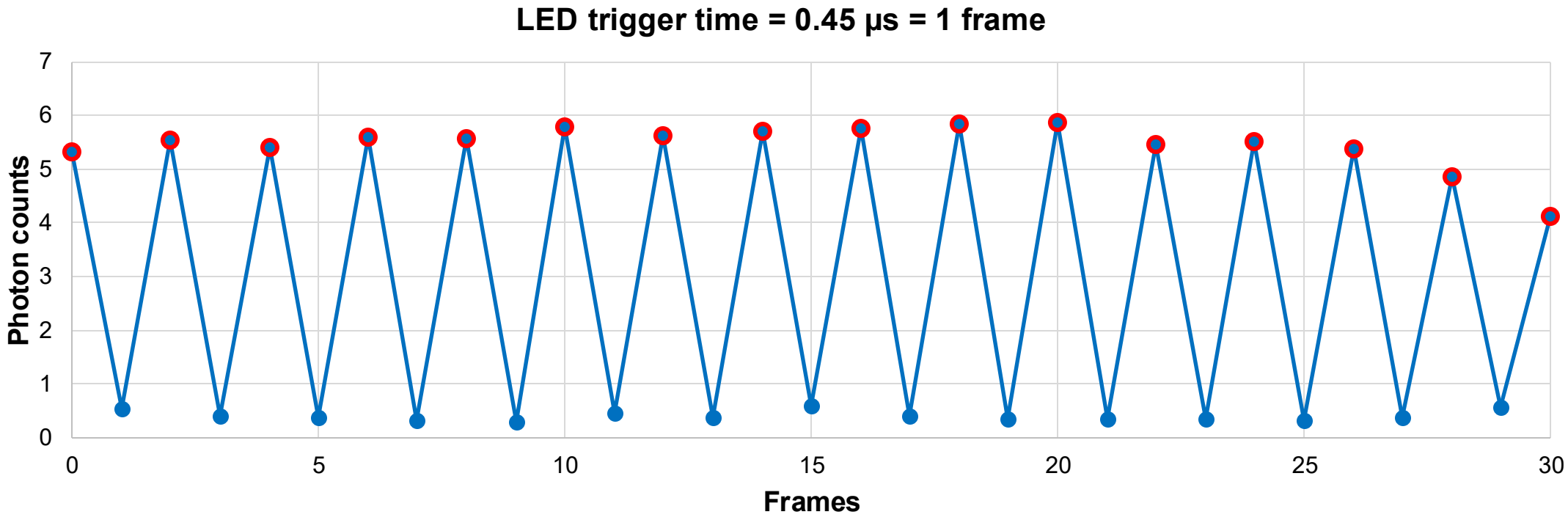
LED blinking frequency: 273 kHz

Experiment Proving 2.18M fps Framerate



LED blinking frequency: 547 kHz

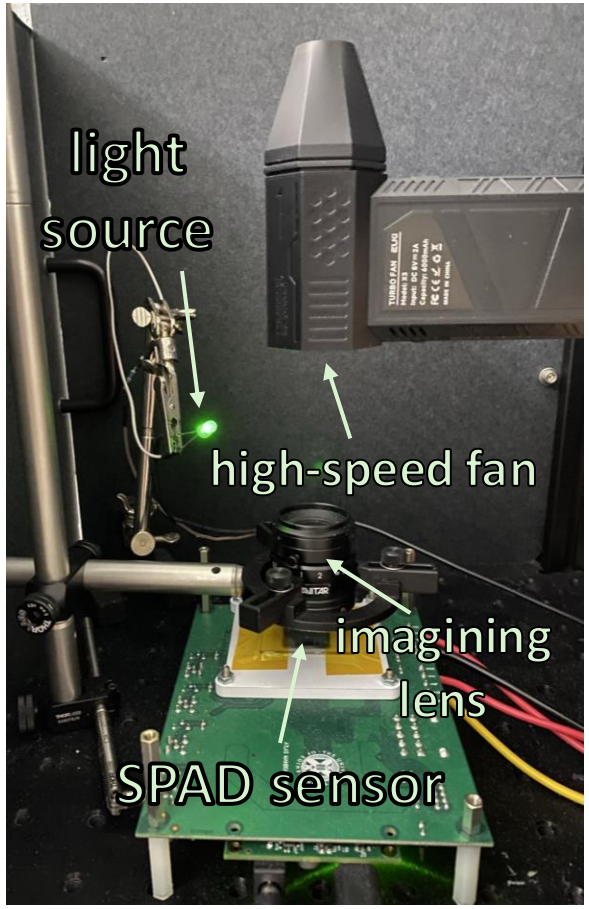
Experiment Proving 2.18M fps Framerate

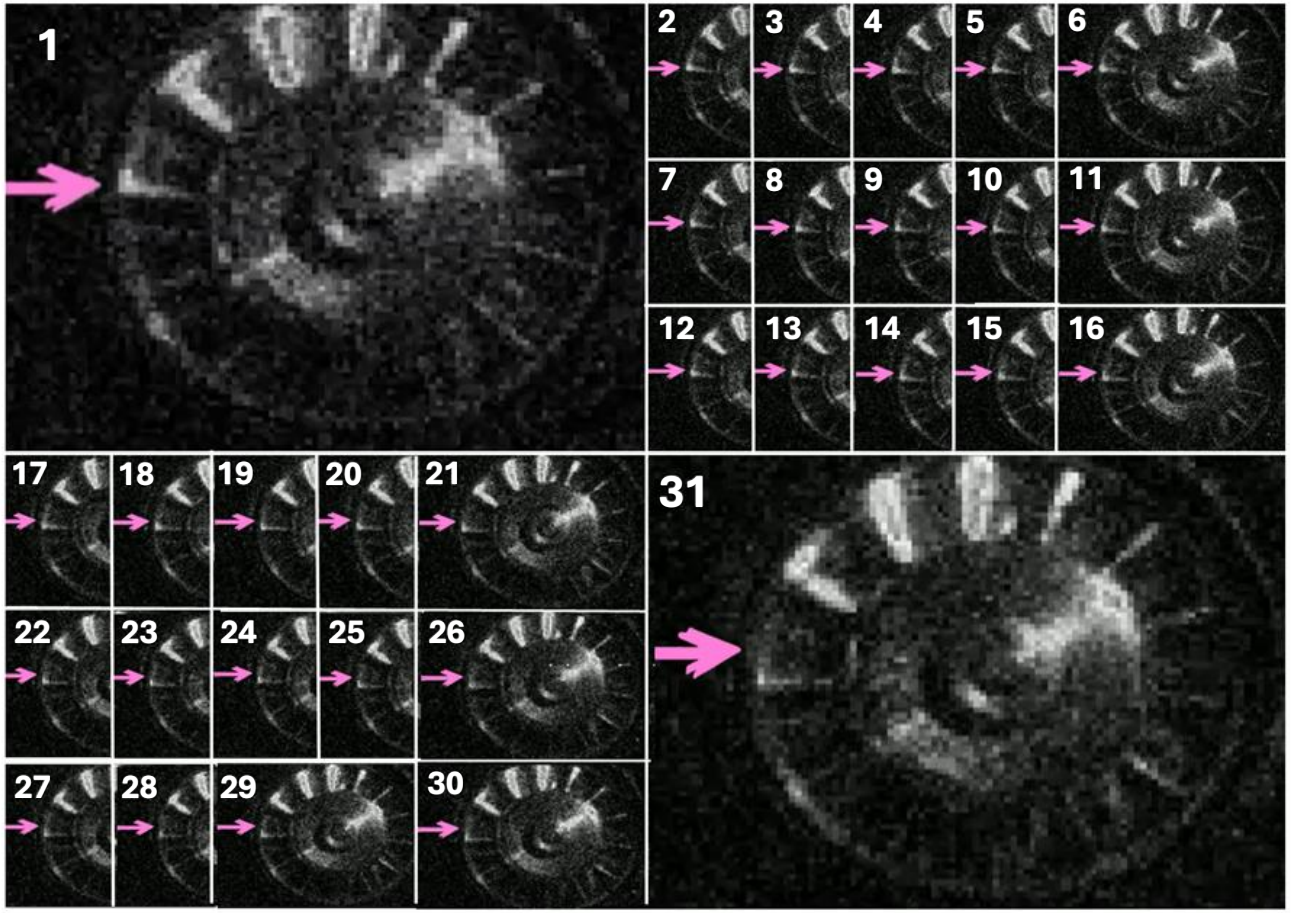


LED blinking frequency: 1094 kHz

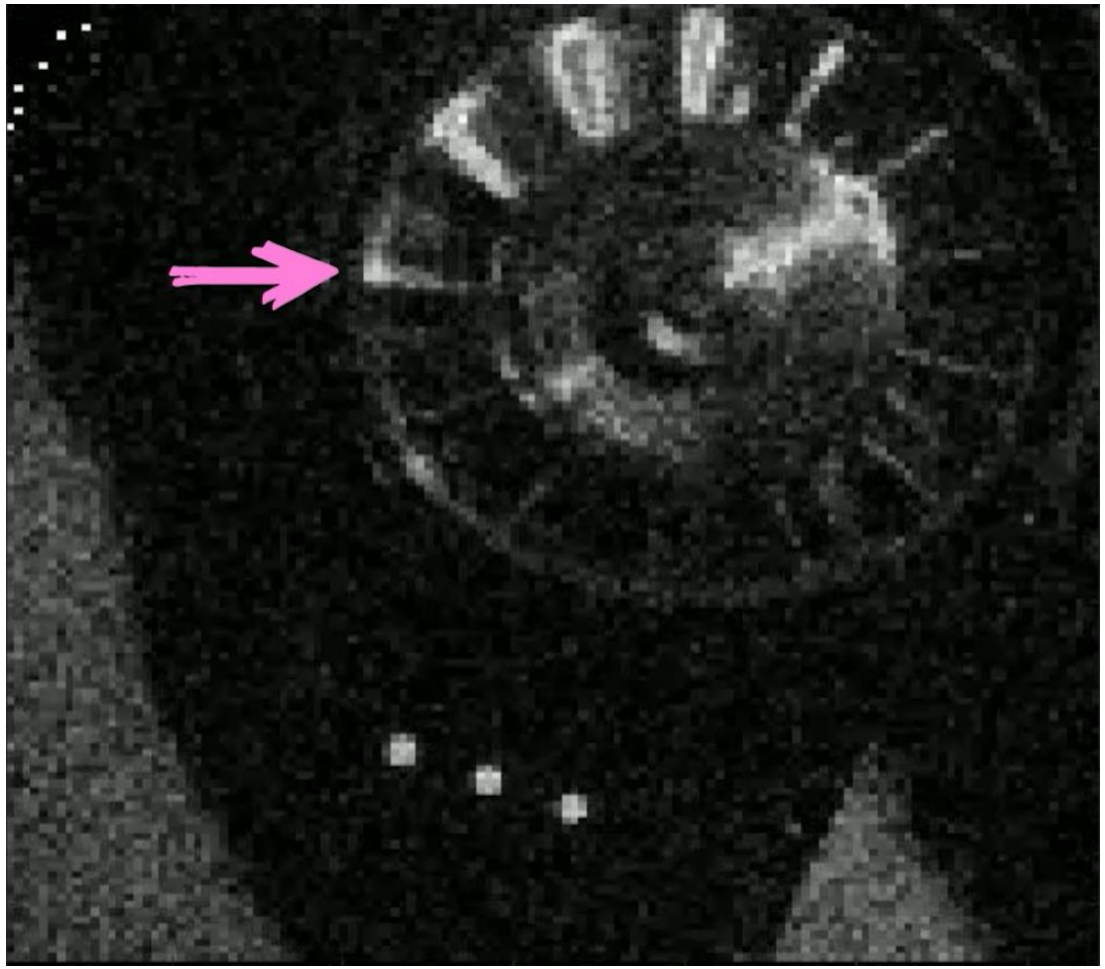
Transient Event Imaging

using a 150,000-rpm air-blaster fan





Transient Event Imaging



- Declared fan speed: 150,000 rpm
- Captured 32-frame burst
- Blade rotation angle: 8° over 31 frames
- Observed fan speed: 102,000 rpm

State-of-the-Art Comparison

Parameter	This work	S. Shigetoshi [1]	S. Manabu [5]	V. Dao [6]	D. Van Blerkom [3]
Technology	3-D-stacked 90 nm BSI / 40 nm	180 nm	180 nm	BSI	110 nm BSI
Imaging device	SPAD	Pinned photodiode	Pinned photodiode	CCD	Partially-pinned photodiode
Maximum framerate (burst) [fps]	2.18M	20M	100M	25M	N/A
Maximum framerate (continuous) [fps]	3k	7.8k	N/A	N/A	80k
Readout noise [e- RMS]	0	5	N/A	N/A	23
Photon detection efficiency/ Quantum efficiency (peak) [%]	55	N/A	N/A	N/A	N/A
Resolution	128×128	400×250	50×108	32×32	1280×832
Data rate (burst) [Mpix/s]	3.6E+10	2.0E+12	5.4E+11	2.6E+10	N/A
Data rate (continuous) [Mpix/s]	1.6E+07	7.8E+08	N/A	N/A	8.5E+10
Architecture	In-pixel memory	Column memory	In-pixel memory	In-pixel memory	Parallel readout
Memory type	Shift register	N/A	Trench capacitor	CCD gate	N/A
Burst length [frames]	32	256	368	1220	N/A
Pixel size [μm^2]	40.68×40.68	32×32	70×35	72.56×72.56	18.54×18.54
Fill factor [%]	~100	63	24	~100	N/A
Full well [e-]	31	10k	N/A	3k	9k
Power consumption [W]	1	10	N/A	N/A	<40

Conclusions

- A successful operation of a SPAD array at 2.18M fps has been shown, demonstrating its feasibility for a single-photon counting ultra high-speed image sensor.
- The pixel has a 5-bit depth, limiting the maximum photon count to 31, constraining the dynamic range.
- Future improvements are expected to enhance both high-speed frames and photon counts to be more adaptable to different application requirements.

References

1. S. Shigetoshi, R. Kuroda, T. Takeda, F. Shao, K. Miyauchi, and Y. Tochigi, “A 20 Mfps global shutter CMOS image sensor with improved sensitivity and power consumption,” in *Proceedings of the 2015 International Image Sensor Workshop*, pp. 166-169, Vaals, The Netherlands, 2015.
2. TMX 7510. Accessed December 11, 2024. https://www.phantomhighspeed.com/products/cameras/tmx/7510.
3. D. Van Blerkom, L. Truong, J. Rysinski, R. Corlan, K. Venkatesan, S. Bagwell, L. Oniciuc, and J. Bergey, “A 1Mpixel, 80k fps global shutter CMOS image sensor for high speed imaging,” in *Proceedings of the 2021 International Image Sensor Workshop*, pp. 166-169, online, 2021.
4. A. Gorman, N. Finlayson, A. Erdogan, L. Fisher, Y. Wang, F. Della Rocca, H. Mai, E. Sie, F. Marsili, and R. Henderson, “ATLAS: a large array, on-chip compute SPAD camera for multispeckle diffuse correlation spectroscopy,” in *Biomedical Optics Express*, vol. 15, no. 11 (2024): 6499-6515.
5. S. Manabu, R. Kuroda, and S. Sugawa, “Over 100 Million Frames per Second 368 Frames Global Shutter Burst CMOS Image Sensor with In-pixel Trench Capacitor Memory Array,” in *Proceedings of the 2019 International Image Sensor Workshop*, pp. 23-27, Snowbird, UT, USA, 2019.
6. V. Dao, N. Ngo, A. Q. Nguyen, K. Morimoto, K. Shimonomura, P. Goetschalckx, L. Haspeslagh, P. De Moor, K. Takehara, and T. G. Etoh, “An image signal accumulation multi-collection-gate image sensor operating at 25 Mfps with 32× 32 pixels and 1220 in-pixel frame memory,” in Sensors, vol. 18, no. 9 (2018): 3112.

Acknowledgements

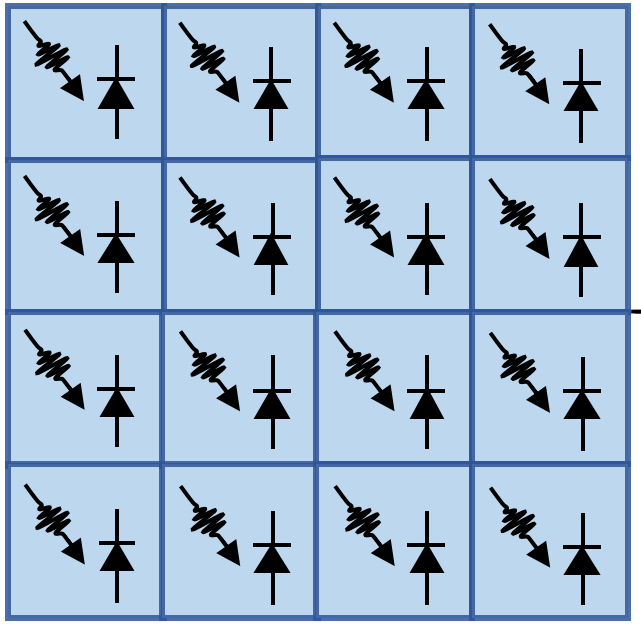
- **Maciej Wojtkiewicz** for support with experiments and chip architecture understanding
- **Francescopaolo Mattioli Della Rocca** for chip design.
- **Ahmet T Erdogan** for firmware development and understanding.
- **Lars Fisher** for PCB design.
- **Robert K Henderson** for supervision and guidance.
- **STMicroelectronics** for chip fabrication

This work was supported by **EPSRC-funded InlightenUs project.**

Backup Slides

Macropixel Architecture

Top tier:
passively-quenched SPADs



Bottom tier: pixel logic circuits