EPFL

Reconfigurable, Large-Format D-ToF/Photon-Counting SPAD Image Sensors with Embedded FPGA for Scene Adaptability

Tommaso Milanese*, Baris Can Efe*, Claudio Bruschini*,

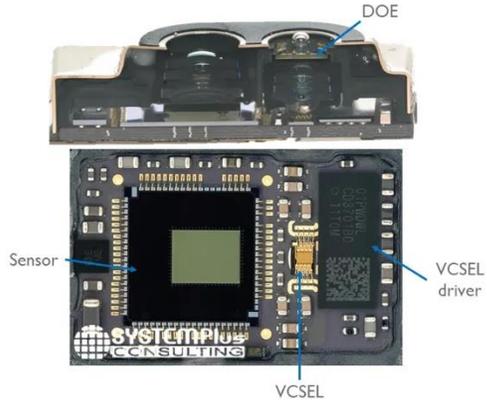Nobukazu Teranishi**, Edoardo Charbon*

*AQUA, STI School of Engineering, École polytechnique fédérale de Lausanne (EPFL), Neuchâtel CH-2000, Switzerland

**Research Institute of Electronics, Shizuoka University, Hamamatsu, Japan

Concept & research goals

SPAD imaging applications

Consumer

LiDAR

Apple iPad Pro LiDAR opening and cross-section

Apple

Auto focus / presence detection

STMicroelectronics

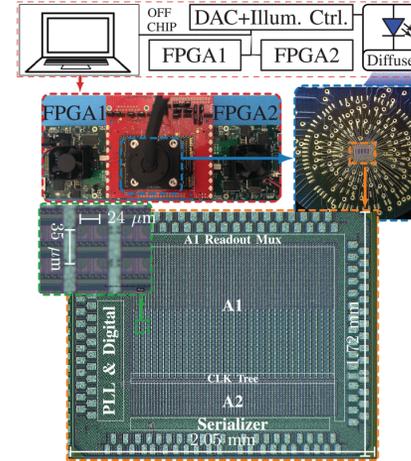## Biomedical

(TOF) PET

Philips – Siemens – GE Healthcare

X-ray imaging

Hand phantom (GP mode) Hand phantom (LP mode) Dog jaw (GP mode)
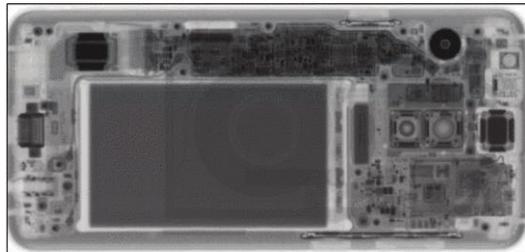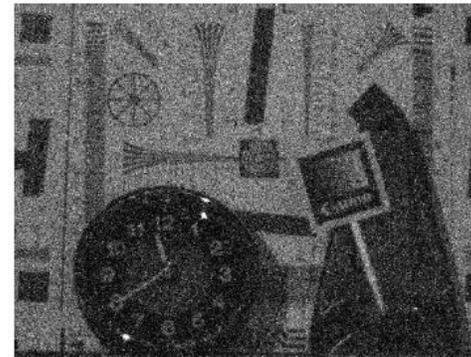
Park, VLSI24

Security

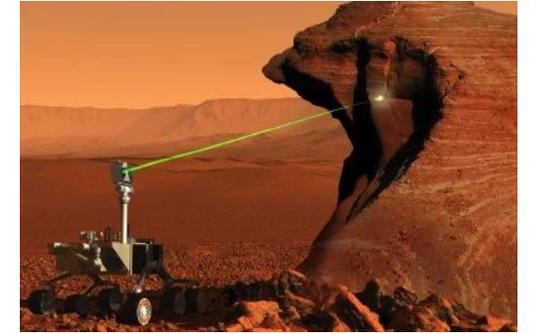### QRNG

Keshavarzian, JSSC,2023

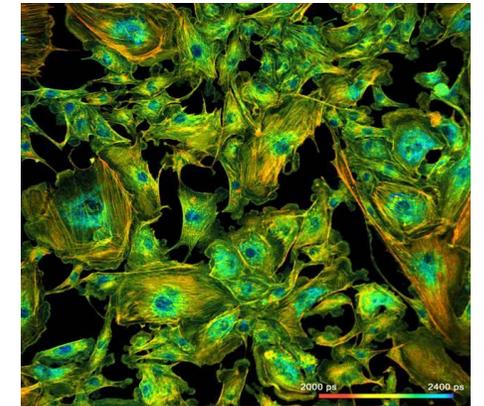### Low-light imaging

Morimoto, IEDM,2021

Scientific
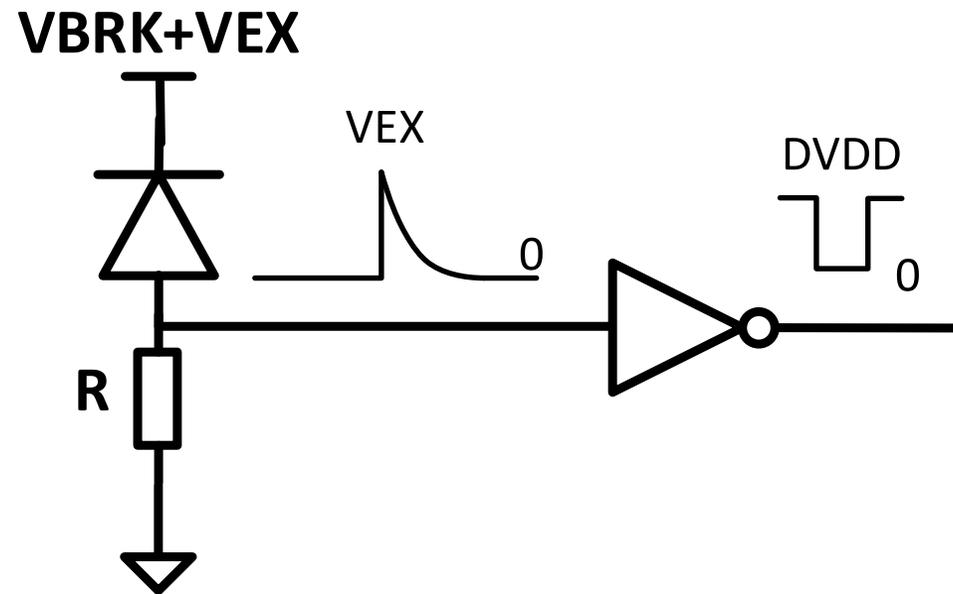
Raman spectroscopy

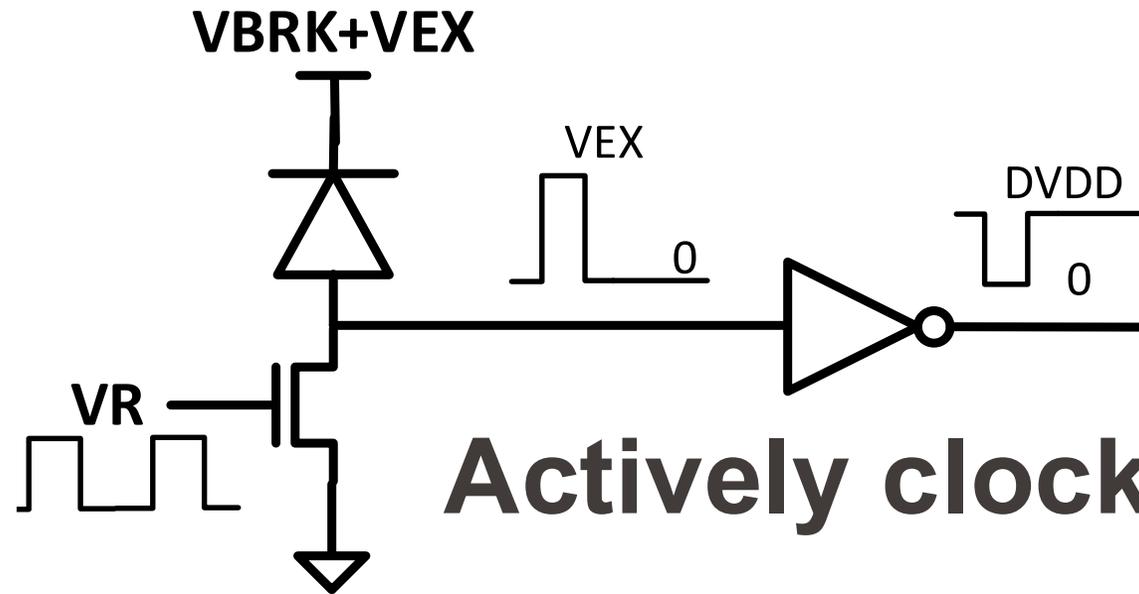Maruyama, JSSC,2013

FLIM

Becker & Hickl

SPAD operation

- Photon-to-digital conversion
- SPAD gain > 10^5
- Imaging device suited for **digital processing**


VBRK+VEX

VEX

DVDD

R

Passive quenching and passive recharge

SPAD operation

- Photon-to-digital conversion
- SPAD gain > 10^5
- Imaging device suited for **digital processing**

VBRK+VEX

VEX

DVDD

VR

Actively clocked recharge

Passive quenching and actively clocked recharge [Charbon 2005]

SPAD imaging platform for rapid prototyping

Discrete implementation

Monolithic implementation

Milanese, OPEX, 2023
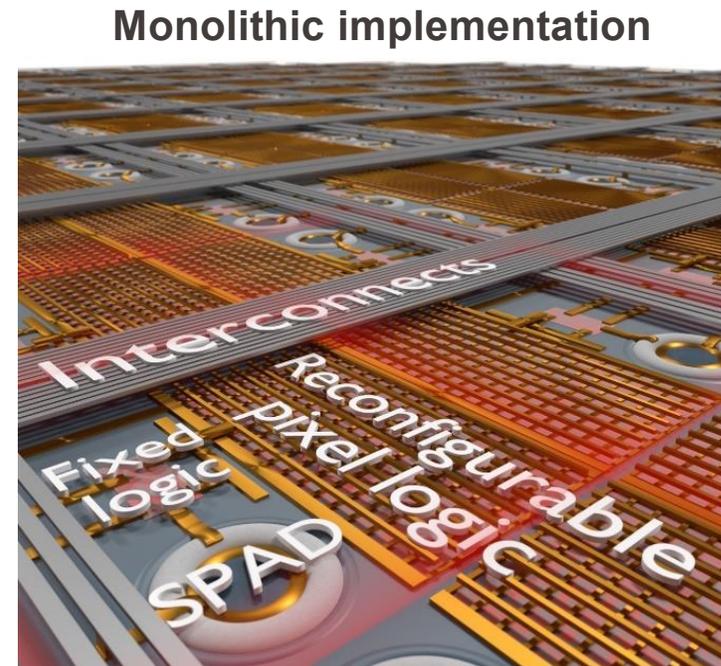
This work

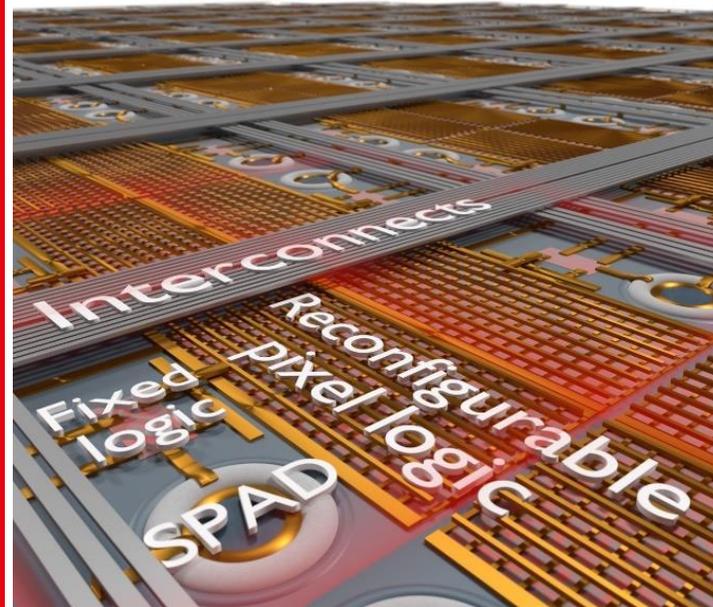Illustrations: H. Homulle from Bruschini et al., SPIE, 2023.

SPAD imaging platform for rapid prototyping

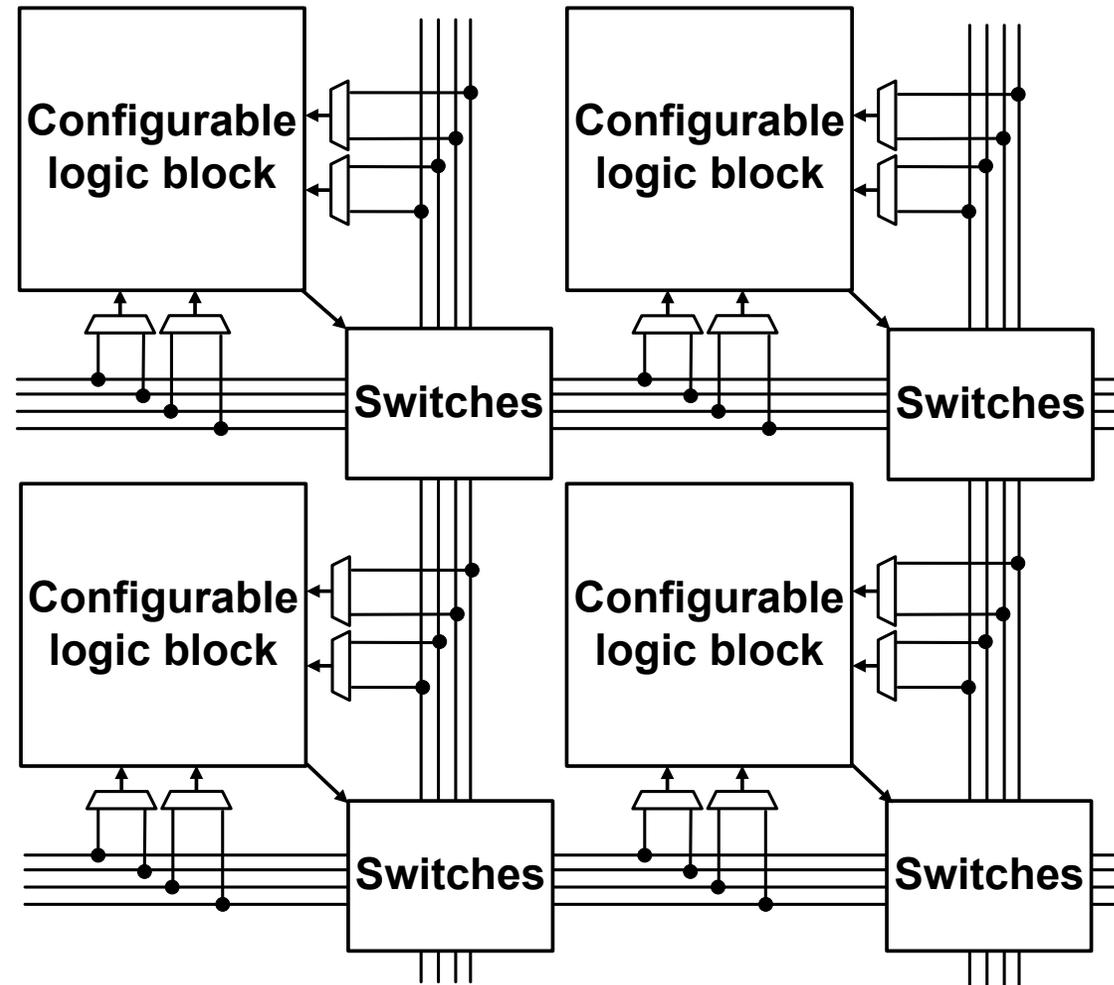**Discrete implementation**
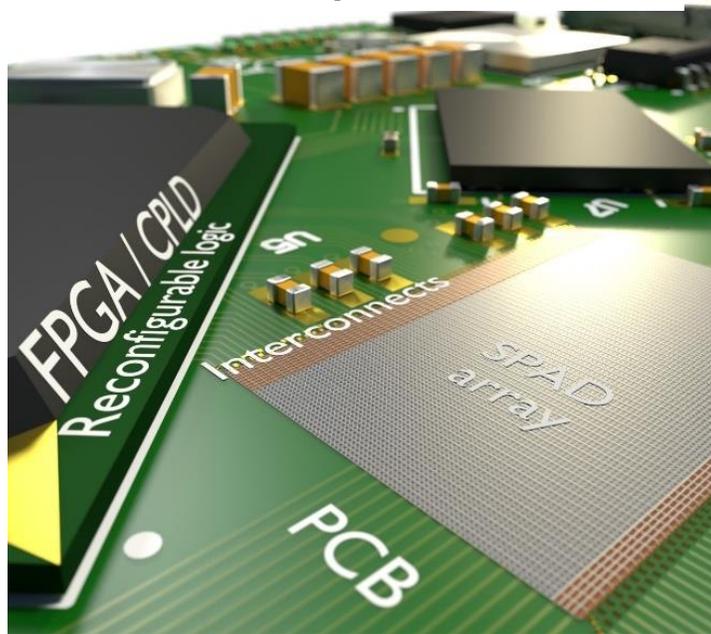
Milanese, OPEX, 2023

Monolithic implementation

This work

Illustrations: H. Homulle from Bruschini et al., SPIE, 2023.
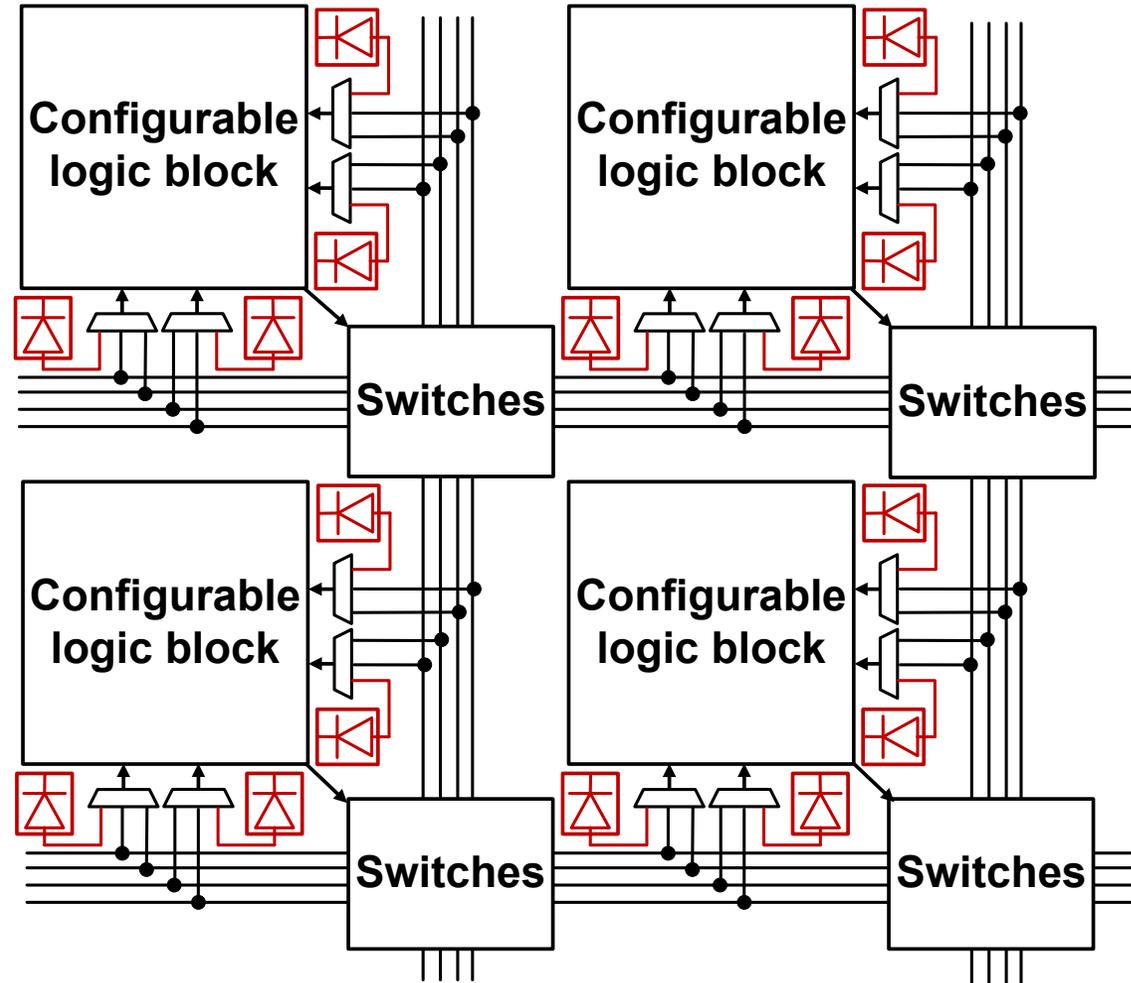
An FPGA-like architecture

- Standard FPGA architecture [1]

[1] A. Boutros and V. Betz, "FPGA Architecture: Principles and Progression," in IEEE Circuits and Systems Magazine, vol. 21, no. 2, pp. 4-29.

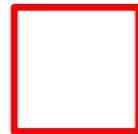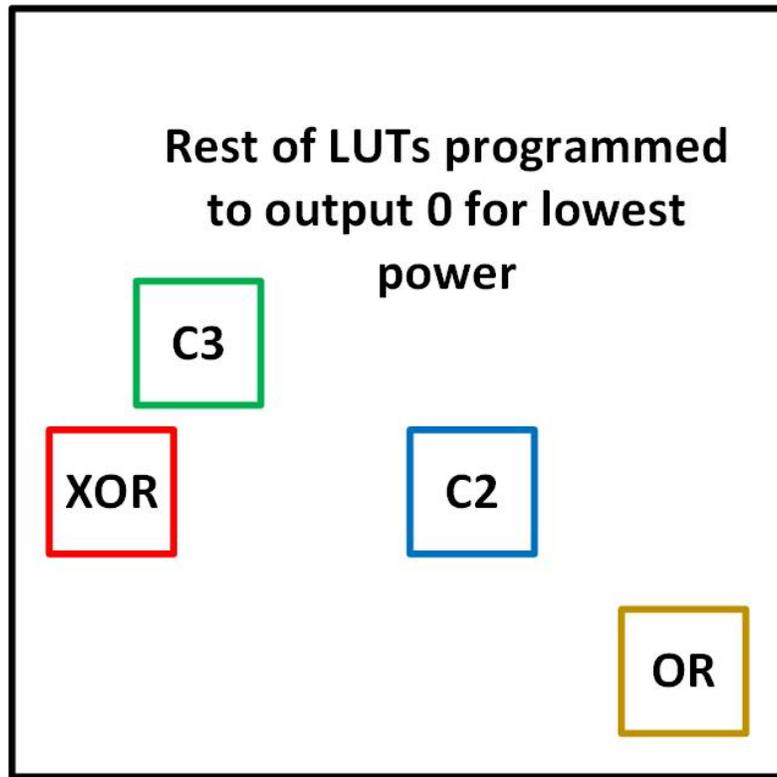# An FPGA-like architecture

- SPAD + FPGA architecture

SPAD pixel

Research goals: scene adaptability

- An FPGA-based SPAD readout allows real-time scene adaptability

SPAD array camera

Scene

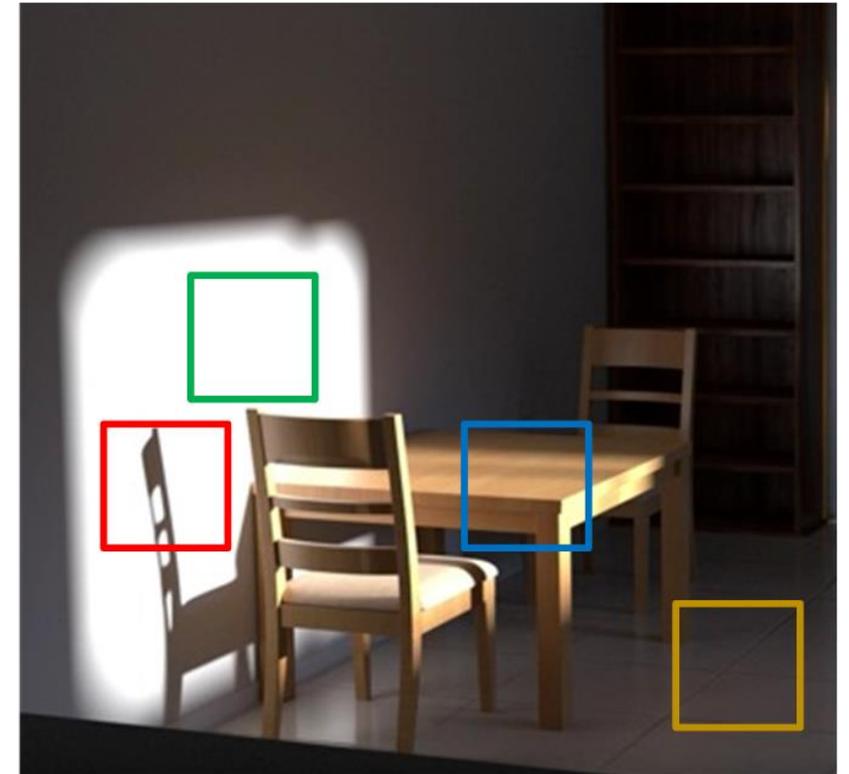
High-flux PC

High-flux DToF

Medium-flux DToF

Low-flux DToF

Rest of LUTs programmed to output 0 for lowest power

C3

XOR

C2

OR

C2 = 2 levels coincidence

C3 = 3 levels coincidence

Reconfigurable macropixel

Monolithic SPAD readout

- Look-up table (LUT) based
- Passive quenching and recharge for proof-of-concept simplicity (no balanced trees)
- Reconfigurable by host for **scene adaptability**

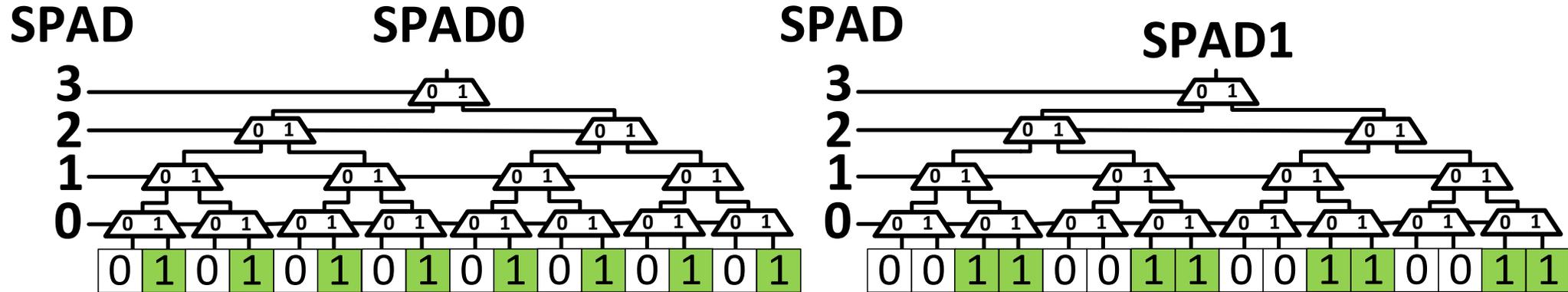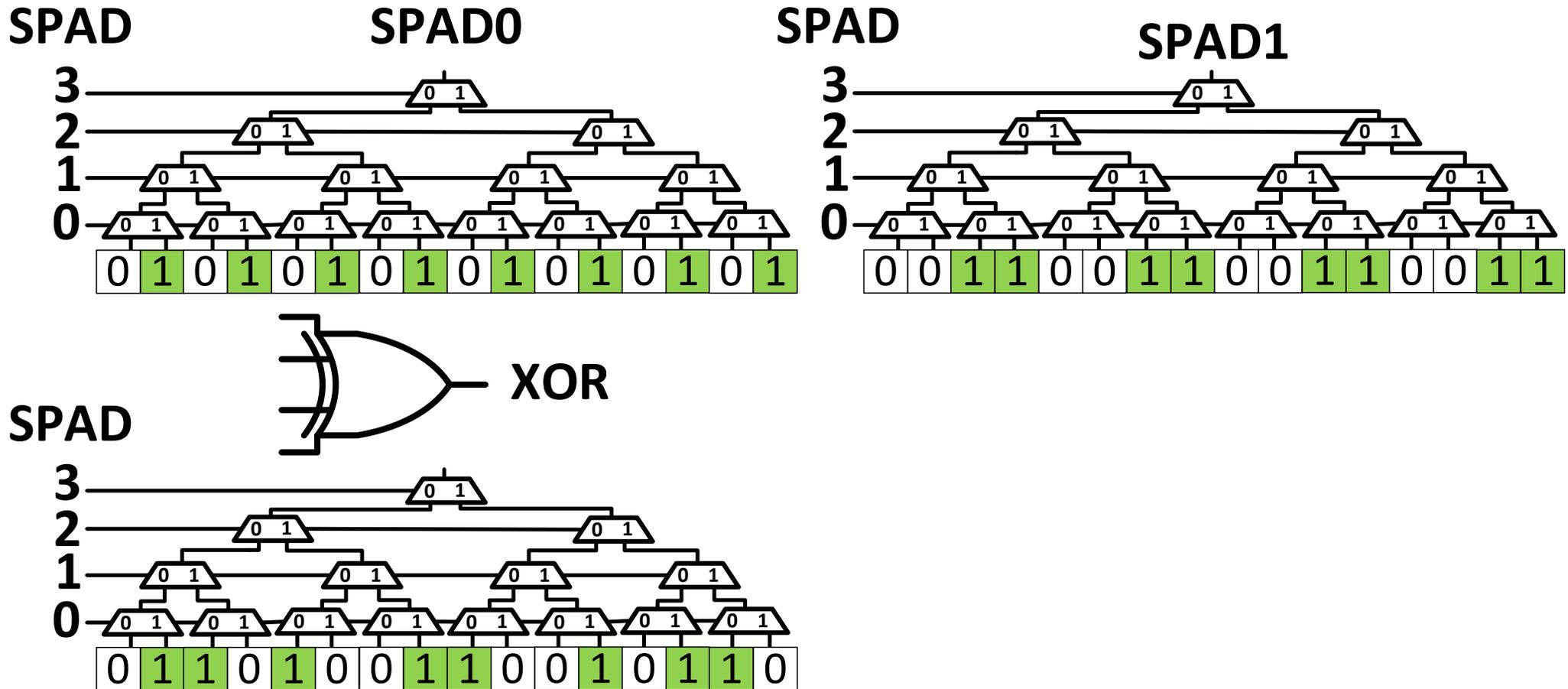# Monolithic SPAD readout

- SPAD time multiplexing → high-spatial resolution
- Low-frame rate

Monolithic SPAD readout

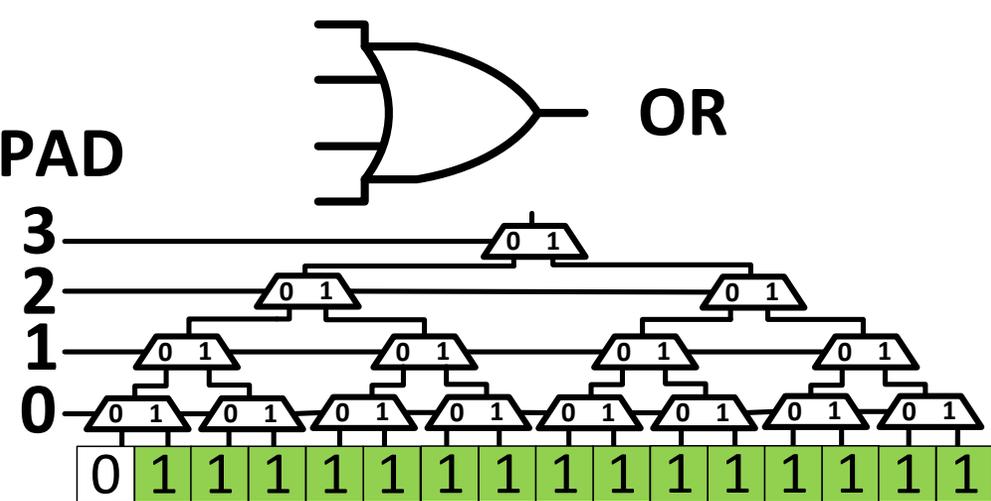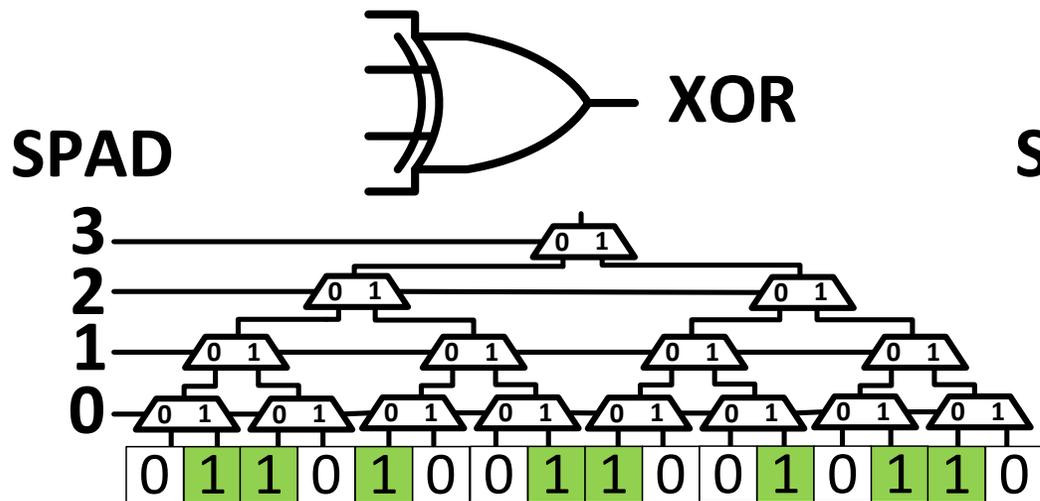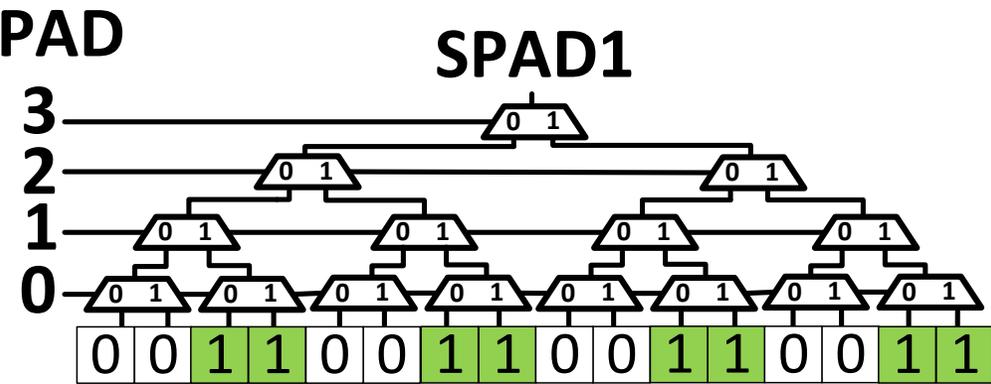- SPAD time multiplexing → high-spatial resolution
- Low-frame rate

- XOR→ High-flux photon counting

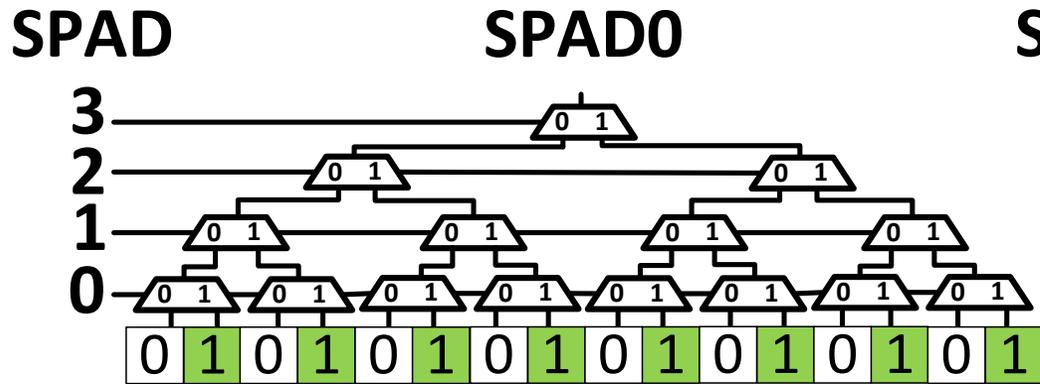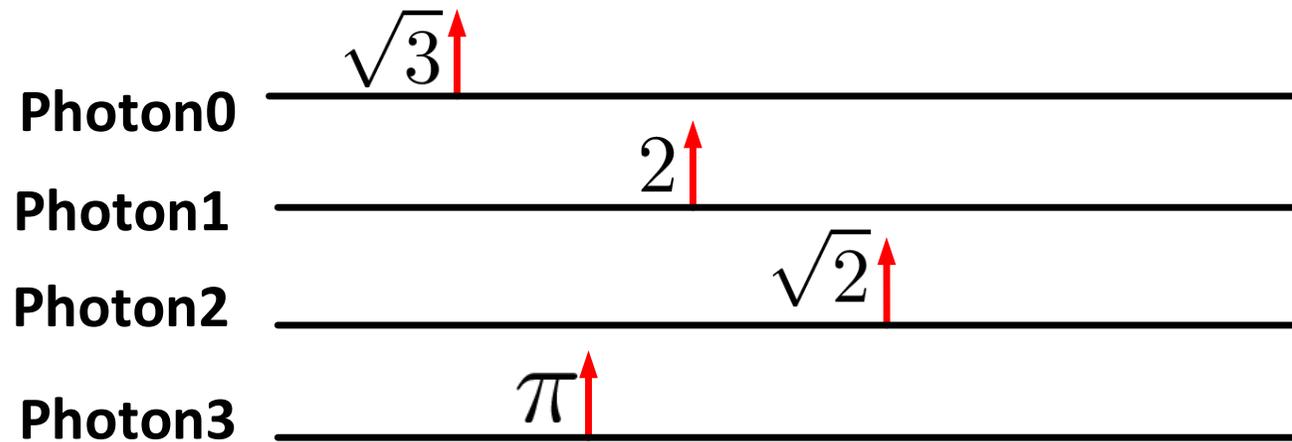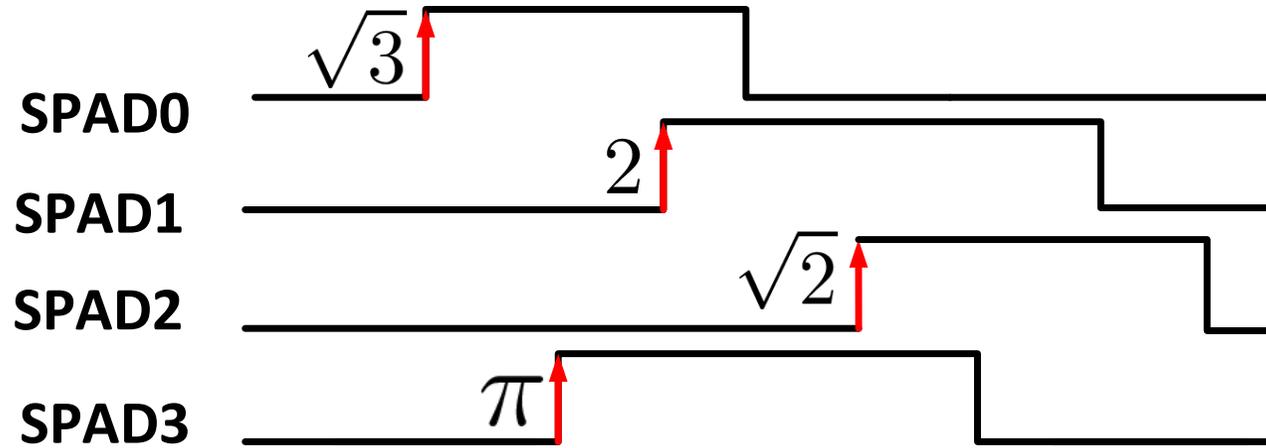# Monolithic SPAD readout

- SPAD time multiplexing → high-spatial resolution
- Low-frame rate

- XOR→ High-flux photon counting
- OR→ LiDAR

Spiking neuron-like operation

Photon0 —————— $\sqrt{3}$ ↑

Photon1 —————— 2 ↑

Photon2 —————— $\sqrt{2}$ ↑

Photon3 —————— π ↑

Spiking neuron-like operation

SPAD0 $\sqrt{3}$

SPAD1 2

SPAD2 $\sqrt{2}$

SPAD3 π

Spiking neuron-like operation

Spiking neuron-like equation

$$W_s = \boxed{\pi} \cdot \text{SPAD3} + \boxed{\sqrt{2}} \cdot \text{SPAD2} + $$
$$+ \boxed{2} \cdot \text{SPAD1} + \boxed{\sqrt{3}} \cdot \text{SPAD0}$$

$$O = \begin{cases} 1 & \text{if } W_s > \boxed{4.94}, \\ 0 & \text{otherwise.} \end{cases}$$
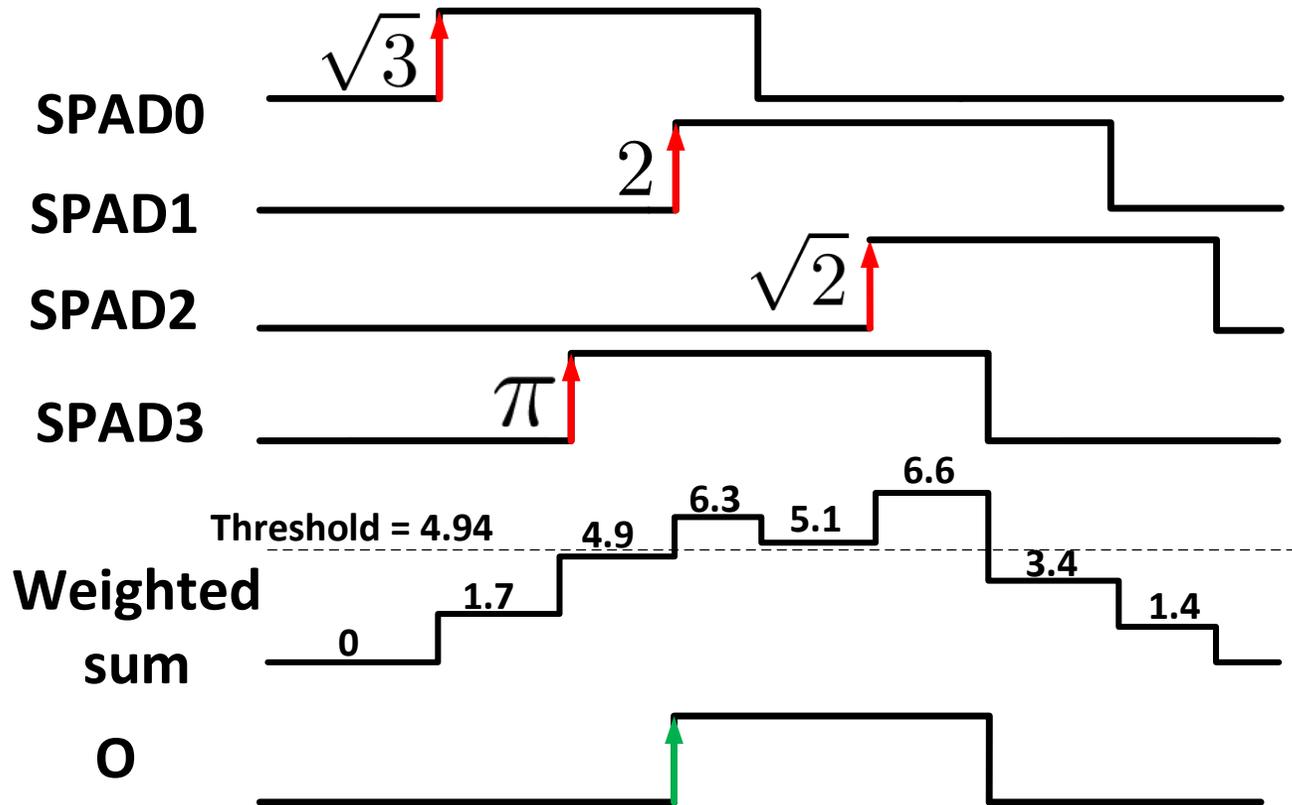
$\boxed{}$ = arbitrary numbers
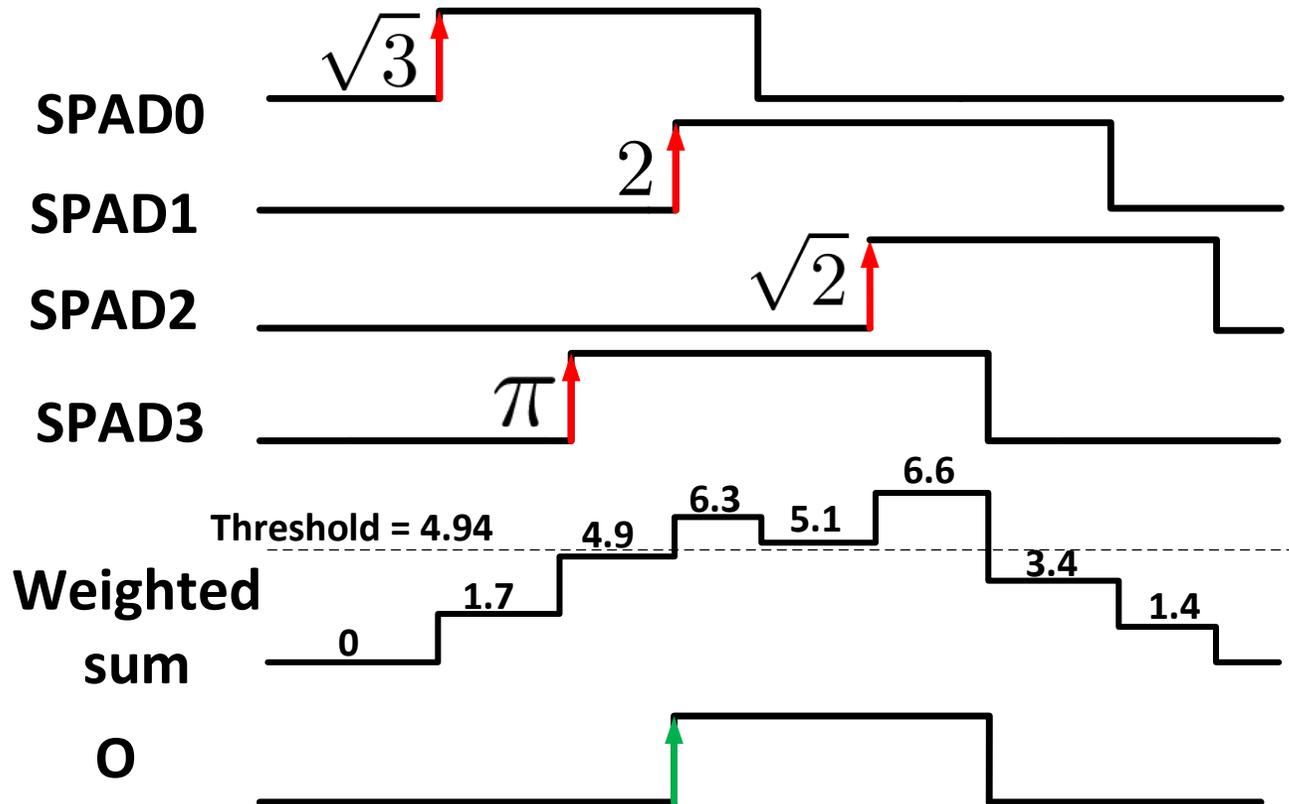
Spiking neuron-like operation

Spiking neuron-like equation

$$W_s = \boxed{\pi} \cdot \text{SPAD3} + \boxed{\sqrt{2}} \cdot \text{SPAD2} +$$
$$+ \boxed{2} \cdot \text{SPAD1} + \boxed{\sqrt{3}} \cdot \text{SPAD0}$$

$$O = \begin{cases} 1 & \text{if } W_s > \boxed{4.94}, \\ 0 & \text{otherwise.} \end{cases}$$

$\boxed{}$ = arbitrary numbers

LUT table

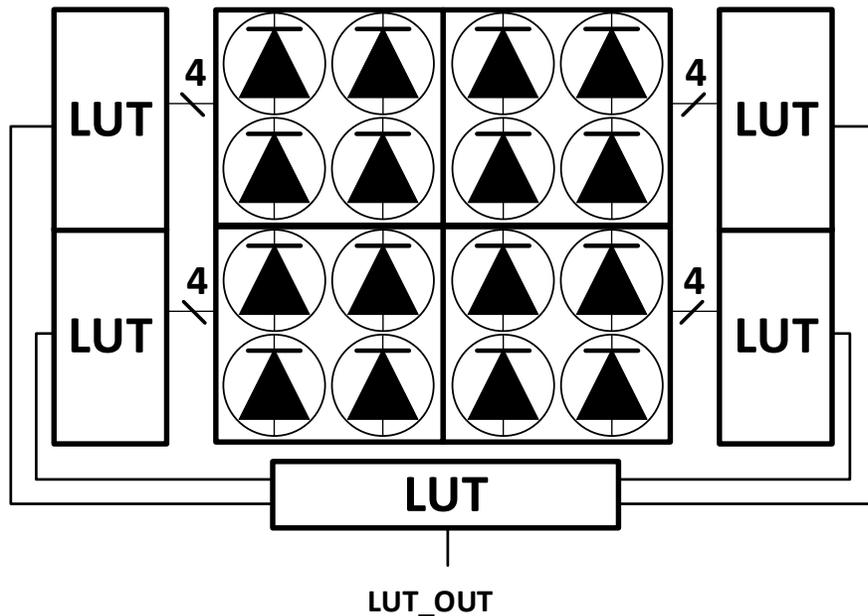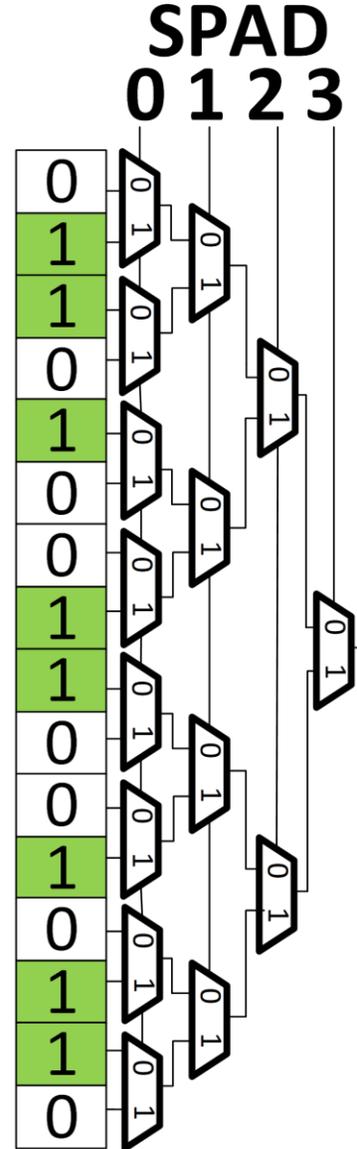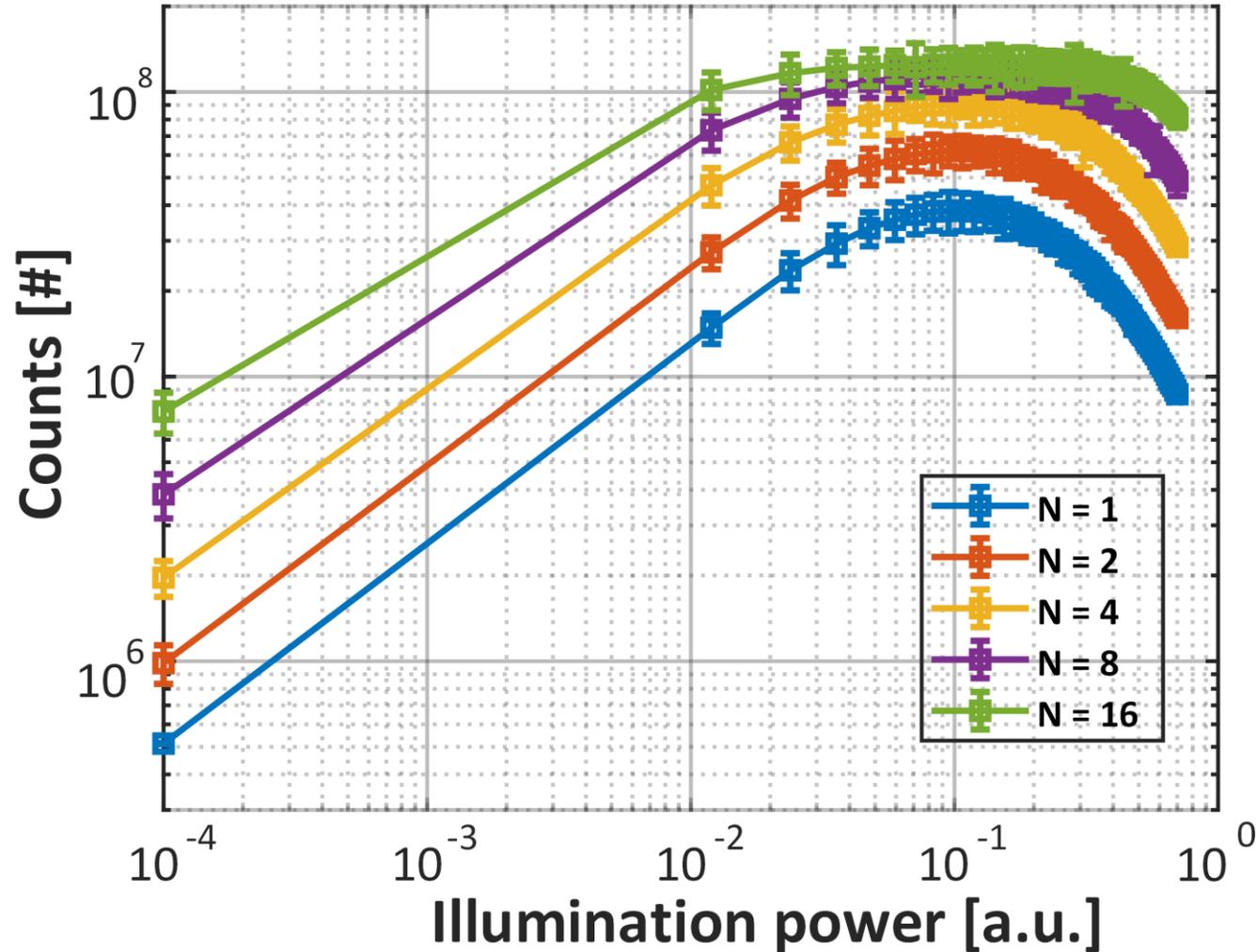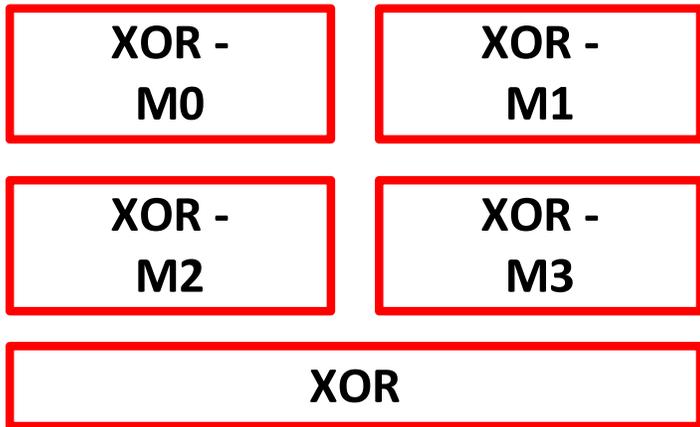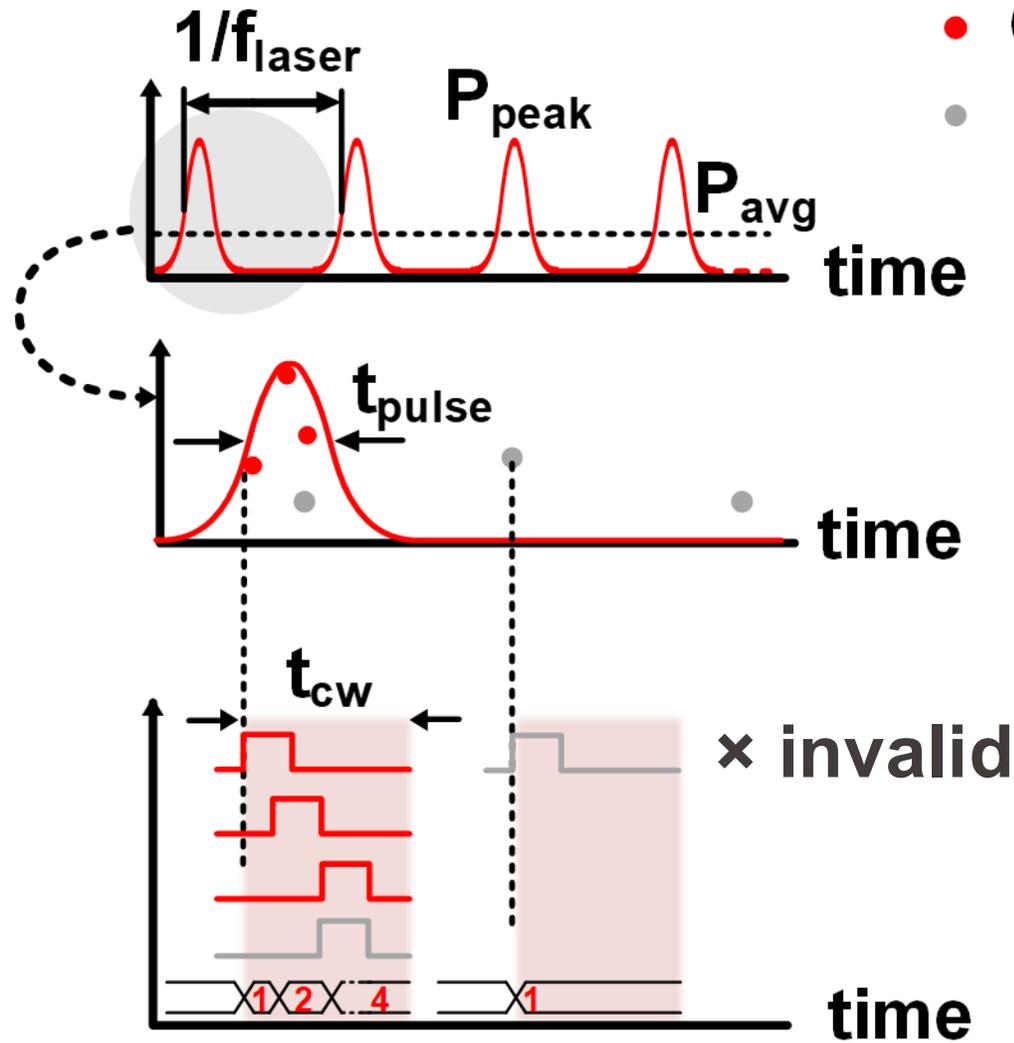| SPAD3	SPAD2	SPAD1	SPAD0	WS	O
0	0	0	0	0	0
0	0	0	1	1.73	0
0	0	1	0	2	0
0	0	1	1	3.73	0
0	1	0	0	1.41	0
0	1	0	1	3.14	0
0	1	1	0	3.41	0
0	1	1	1	5.15	1
1	0	0	0	3.14	0
1	0	0	1	4.87	0
1	0	1	0	5.14	1
1	0	1	1	6.87	1
1	1	0	0	4.55	0
1	1	0	1	6.29	1
1	1	1	0	6.55	1
1	1	1	1	8.29	1

Results

Monolithic SPAD readout

- Proof-of-concept 110 nm
- 16 SPADs with 5 LUTs
- JTAG: 80 FF x 10 ns = 800 ns programming time

16 SPADs - 2 levels LUT circuit
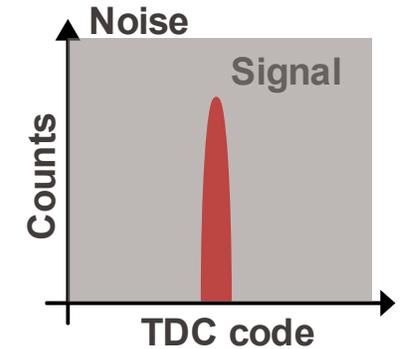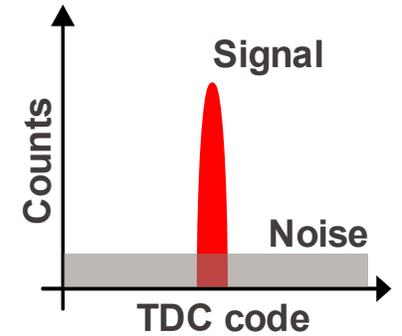
Linearity - XOR
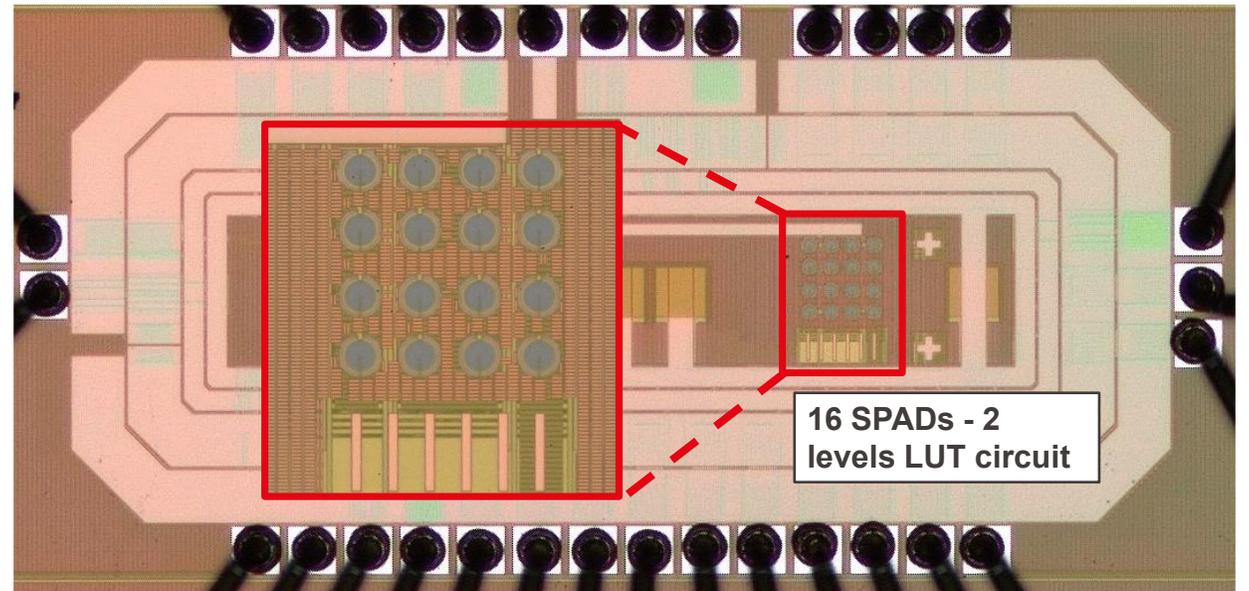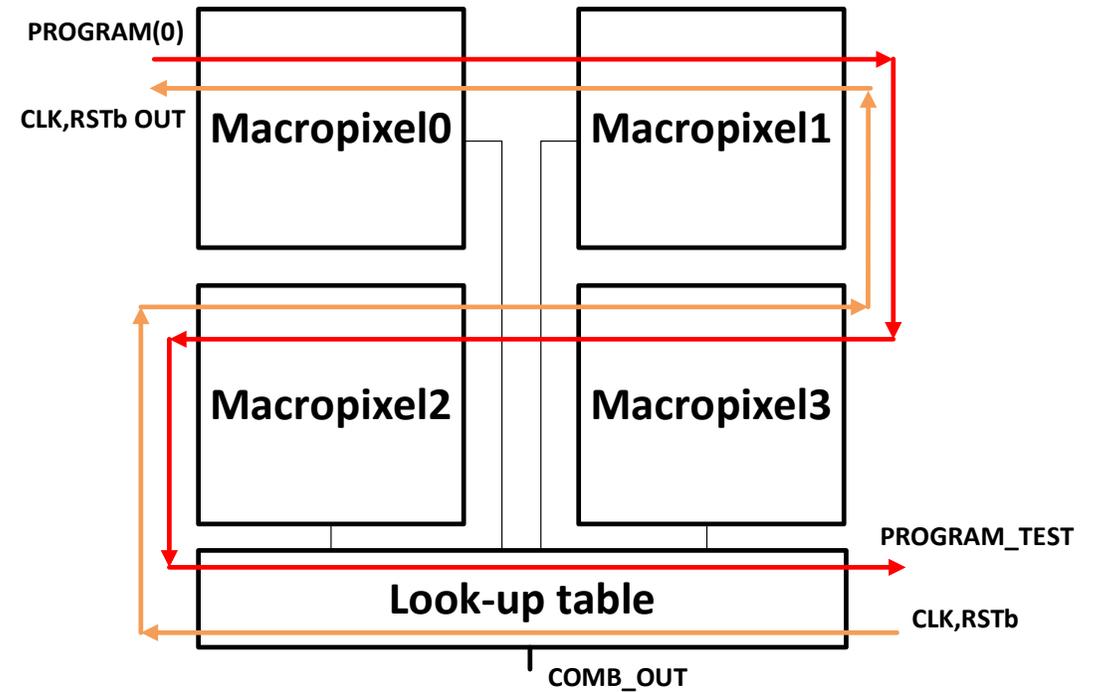
- 1 V excess bias
- 1-2-4-8-16 SPADs

XOR - M0

XOR - M1

XOR - M2

XOR - M3

XOR

Linearity - OR

- 16 SPADs
- 1-2-3-4 V excess bias

OR - M0

OR - M1

OR - M2

OR - M3

OR

Coincidence

- A photon activates the shutter
- Shutter is stopped by next or later photons

$1/f_{laser}$

P_{peak}

P_{avg}

time

t_{pulse}

time

t_{cw}

× invalid

time

X 1 X 2 X .. 4   X 1

- **Coincident photon**
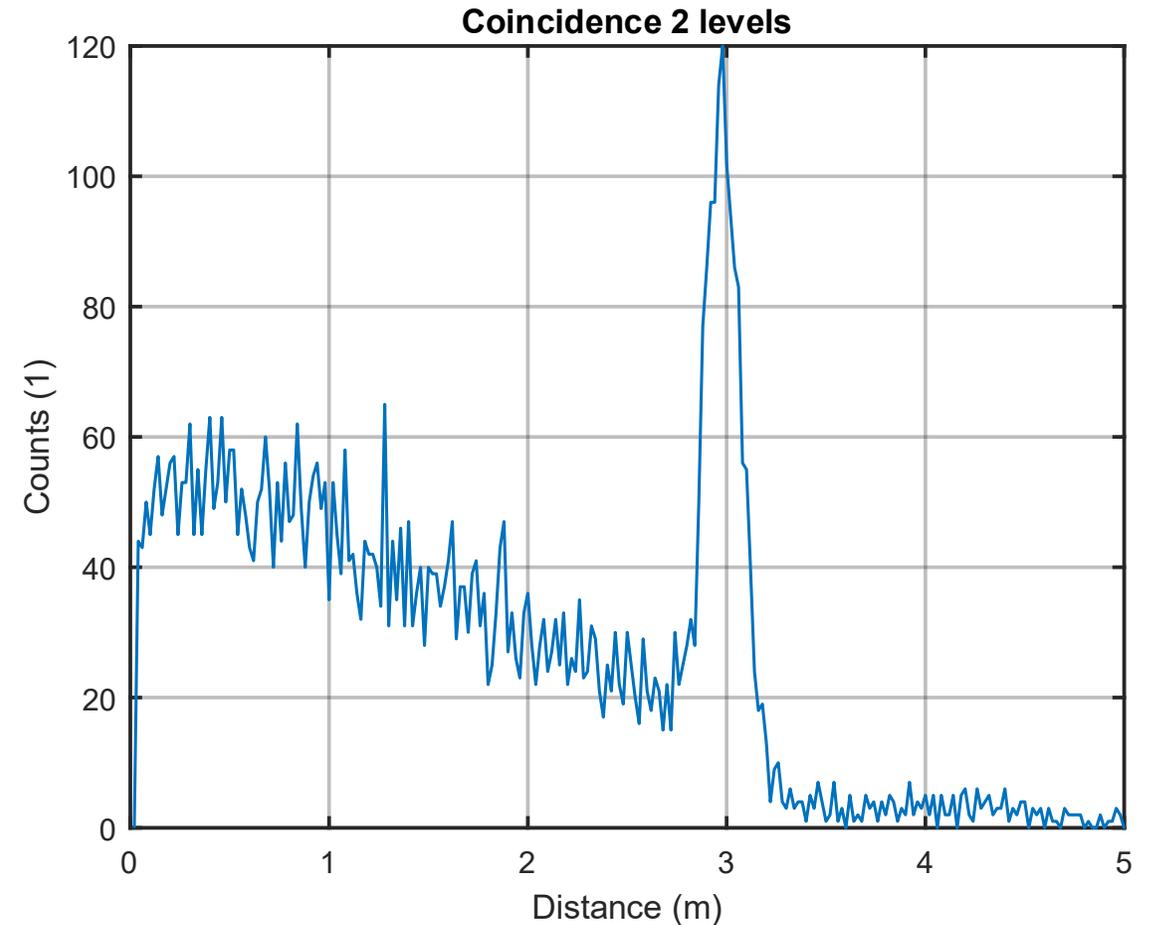- **Noise photon**

Counts

Signal

Noise

TDC code

Noise

Signal
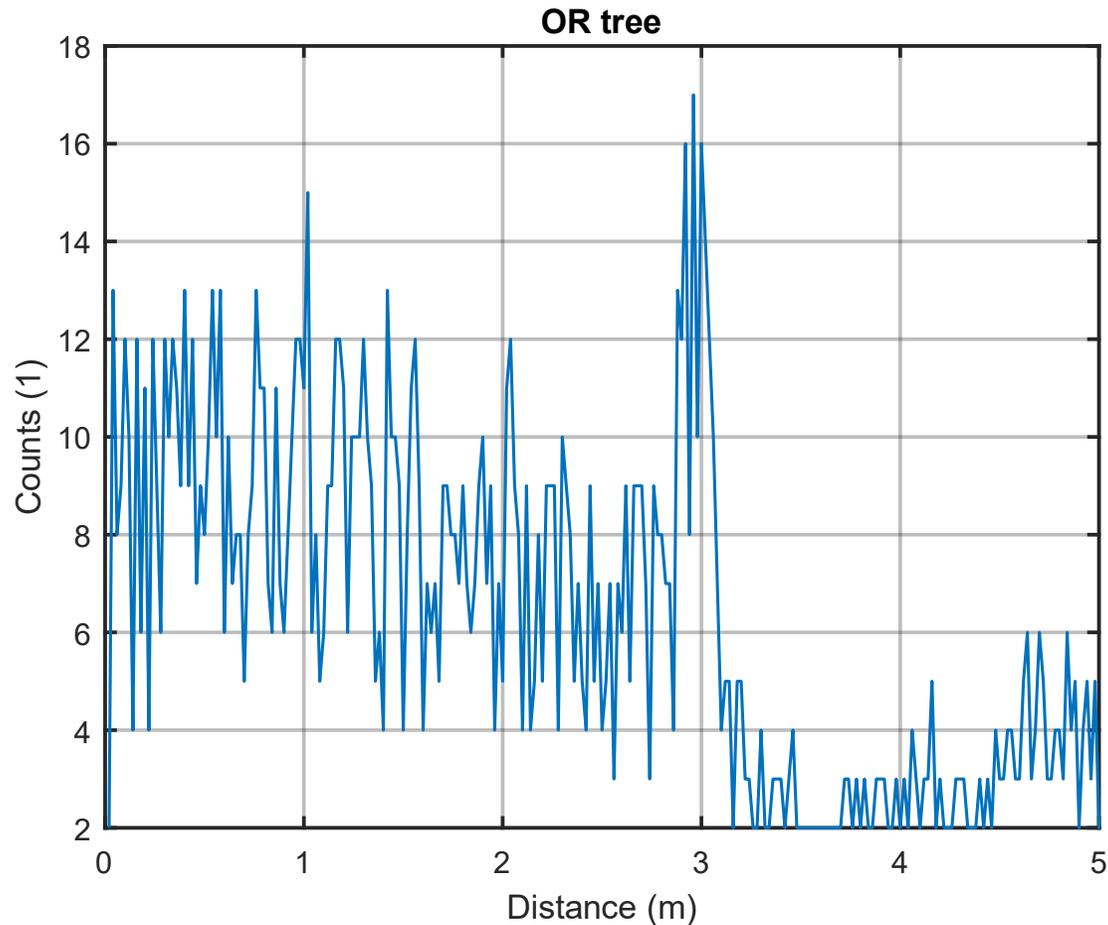
Counts

TDC code

A. Ximenes et al, ISSCC 2019

P. Padmanabhan, "Direct time-of-flight SPAD image sensors for light detection and ranging.", EPFL thesis, 2021.

Coincidence vs OR

- Simulated single-shot TDC
- OR tree piled-up
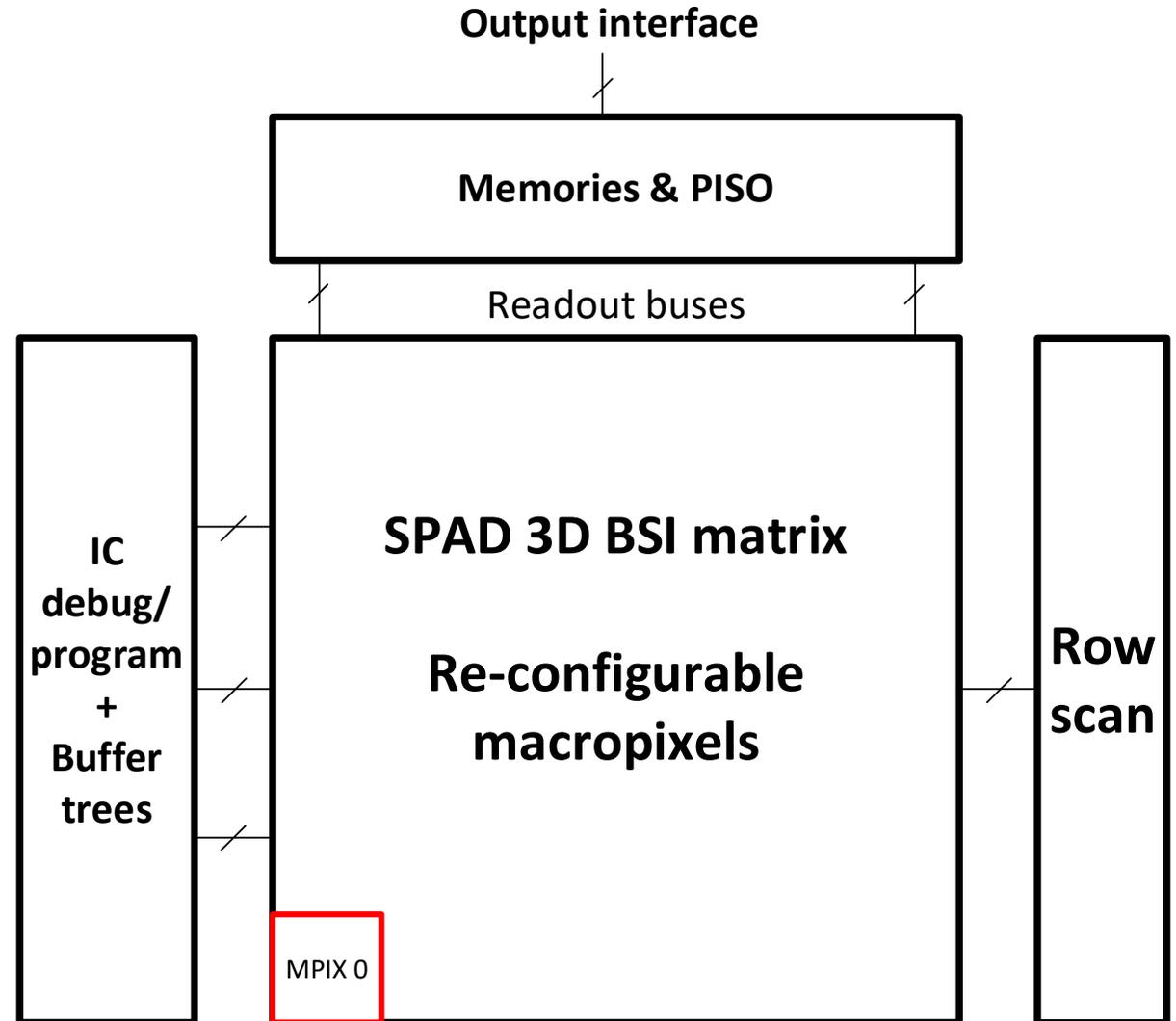- 2 levels coincidence performs better

Perspectives

New architectures for reconfigurable pixels

- 3D-stacked technology
- 2x2 SPADs macropixel
- 64x64 SPADs
- 32x32 macropixels proof-of-concept

64x64 SPAD

2x2 macropix

Electronics
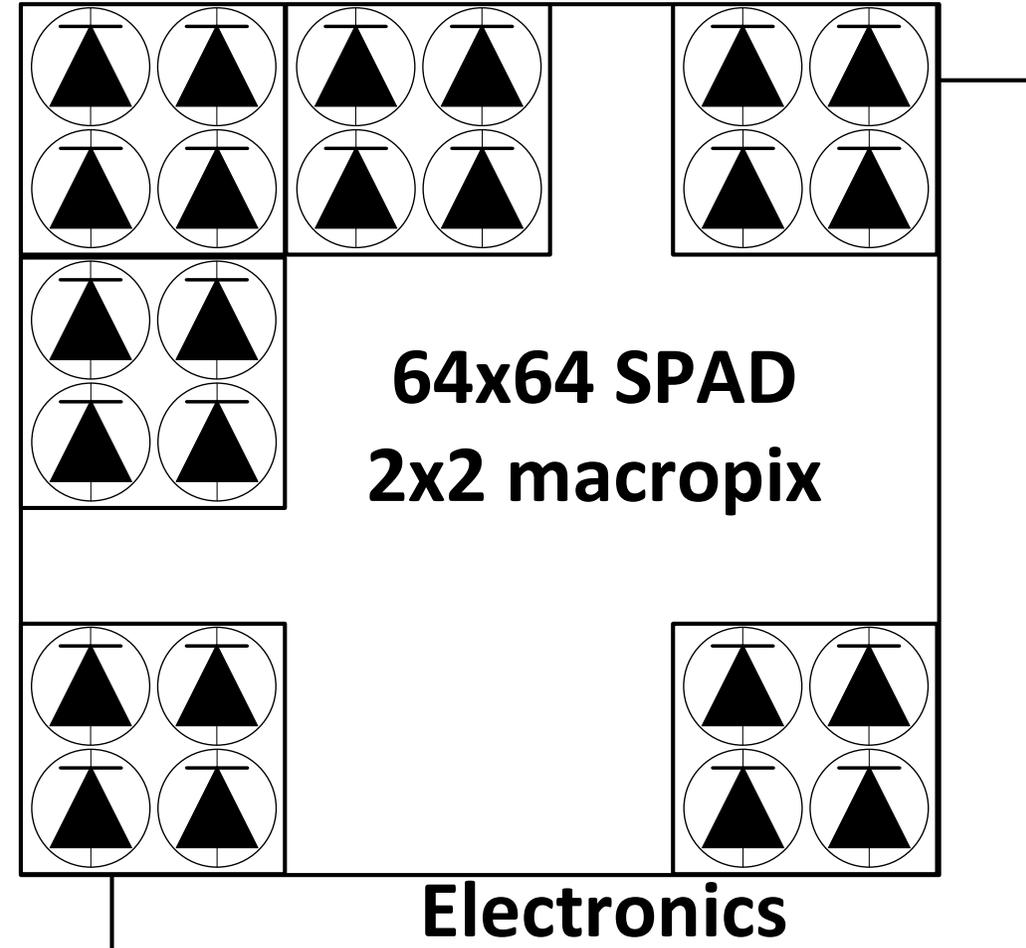
Architecture for reconfigurable pixels

- Top-level diagram
- JTAG array programming
- Memories for high TAR*
- 3D stacked BSI technology

Output interface

Memories & PISO

Readout buses

IC debug/ program + Buffer trees

SPAD 3D BSI matrix

Re-configurable macropixels

MPIX 0

Row scan

*TAR = Temporal aperture ratio.

TDC/photon counter

- Window generation circuit
- Generate window only if TDC is programmed for ToF

TDC vs counter
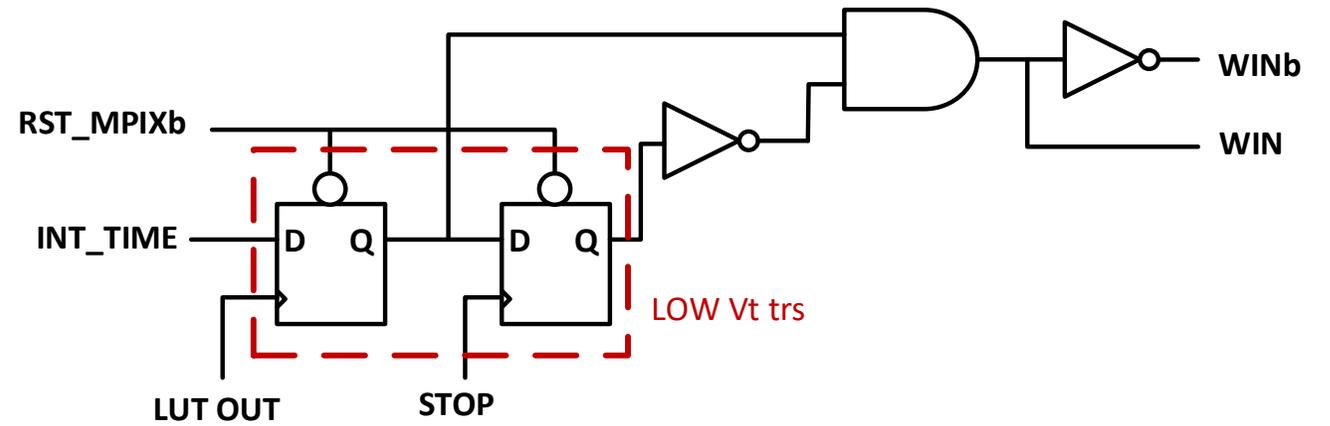
- Window generation circuit
- Generate window only if TDC is programmed for ToF
- Otherwise GRO [1] doesn't start
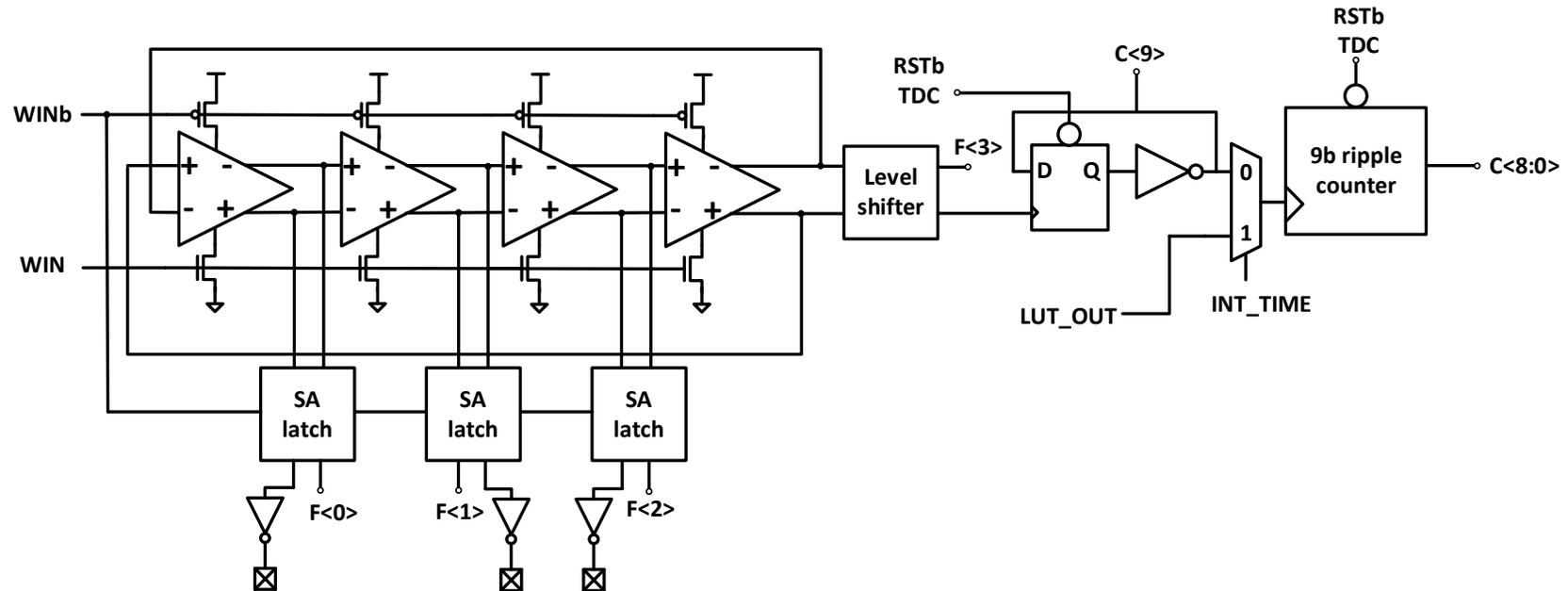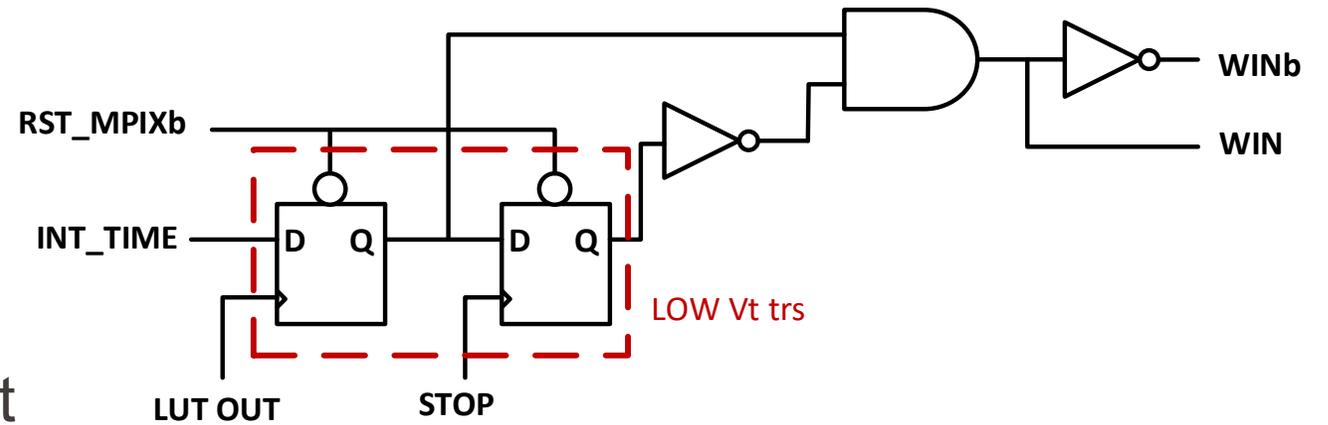
[1] Veerappan, Chockalingam, et al. "A 160× 128 single-photon image sensor with on-pixel 55ps 10b time-to-digital converter." *2011 IEEE International Solid-State Circuits Conference*. IEEE, 2011.

Power/speed considerations

64x64 SPADs
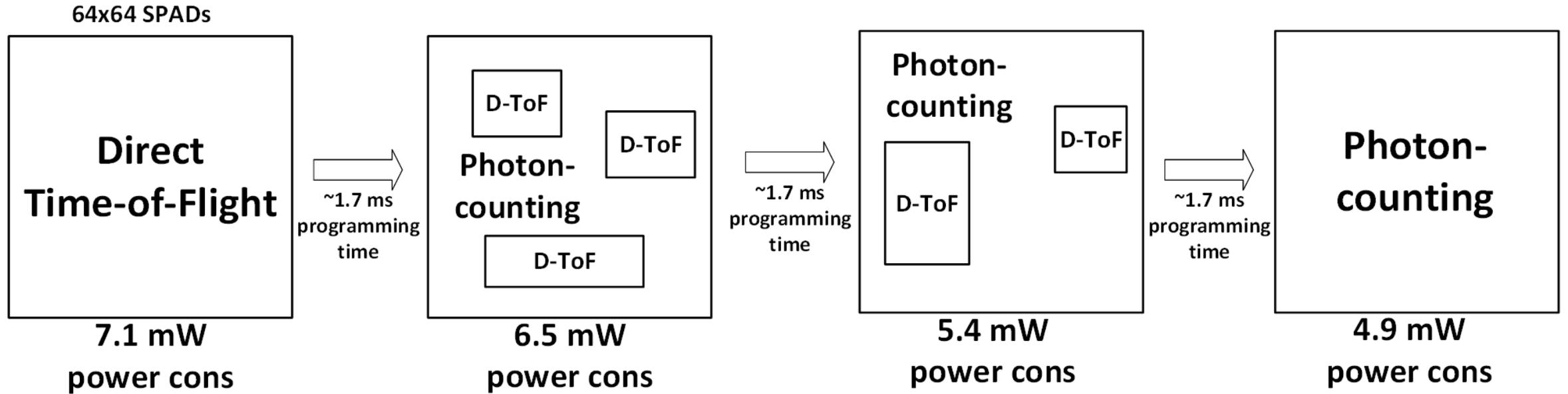
- Single macropixel power consumption
  - ToF $\rightarrow$ 6.9 uW
  - Intensity $\rightarrow$ 4.8 uW
- 1 Mcps per pixel with 2 us integration time.
- Estimation on single readout cycle (one exposure + read).

Summary

Summary

- SPAD imaging platform for rapid prototyping
  - Scene adaptability
  - Standard combinations OR - XOR
  - Spiking neuron
- 2D planar proof-of-concept macropixel characterization
  - Linearity
  - Coincidence
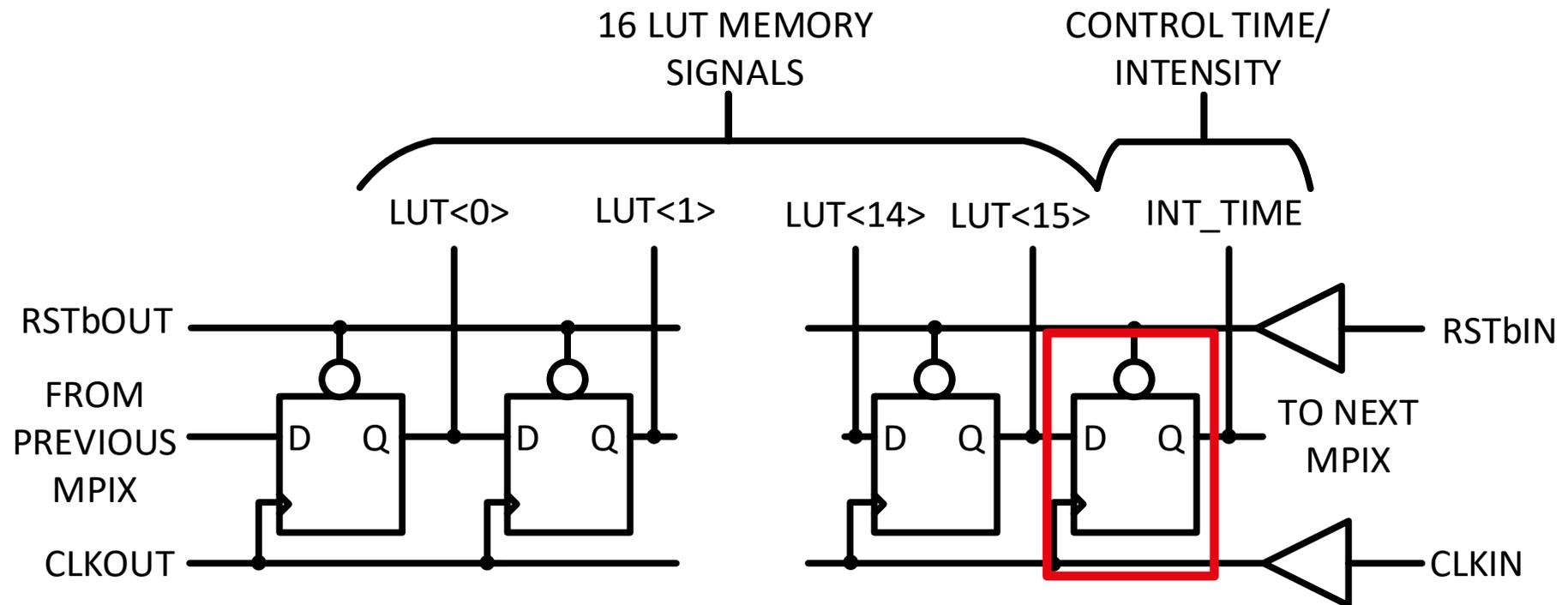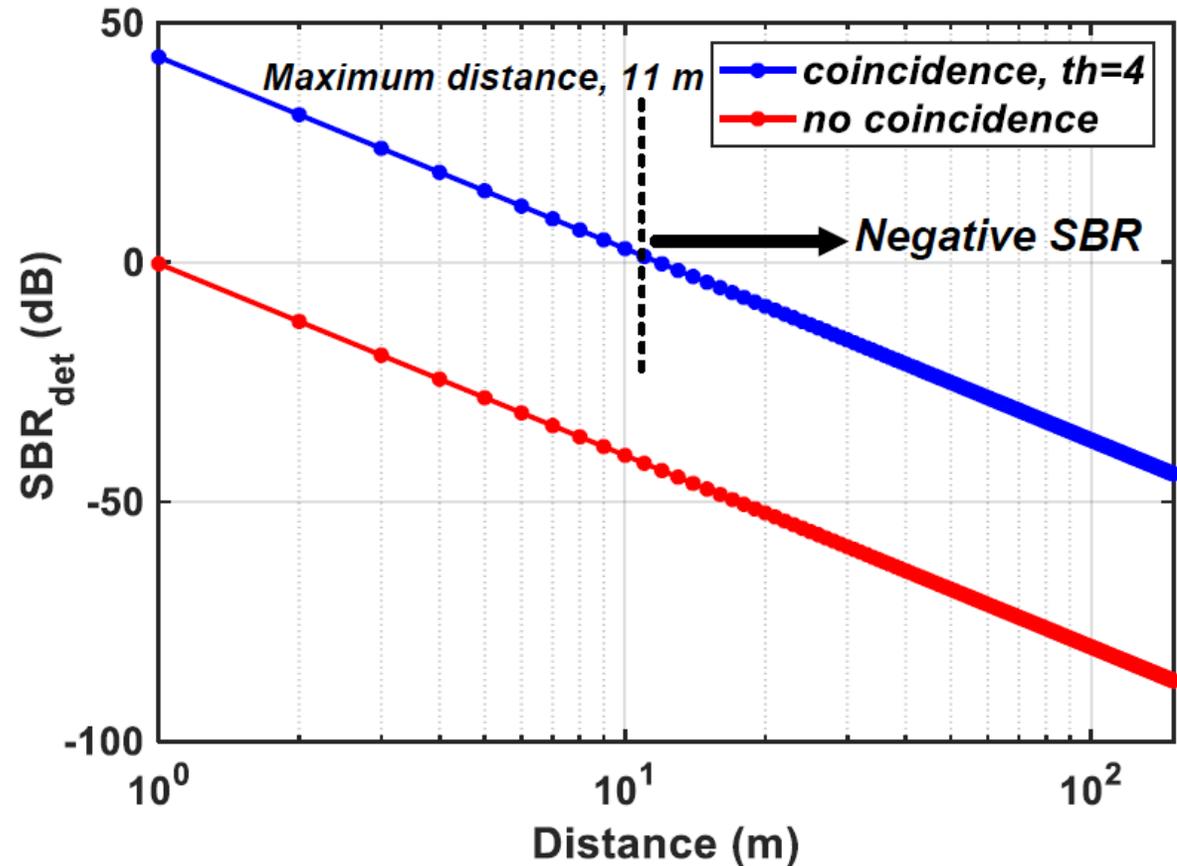- 3D-stacking implementation
  - Low-power sensor modes

EPFL

Thank you

Backup

Intensity vs ToF

- 17b shift register
- SPADs readout with LUT
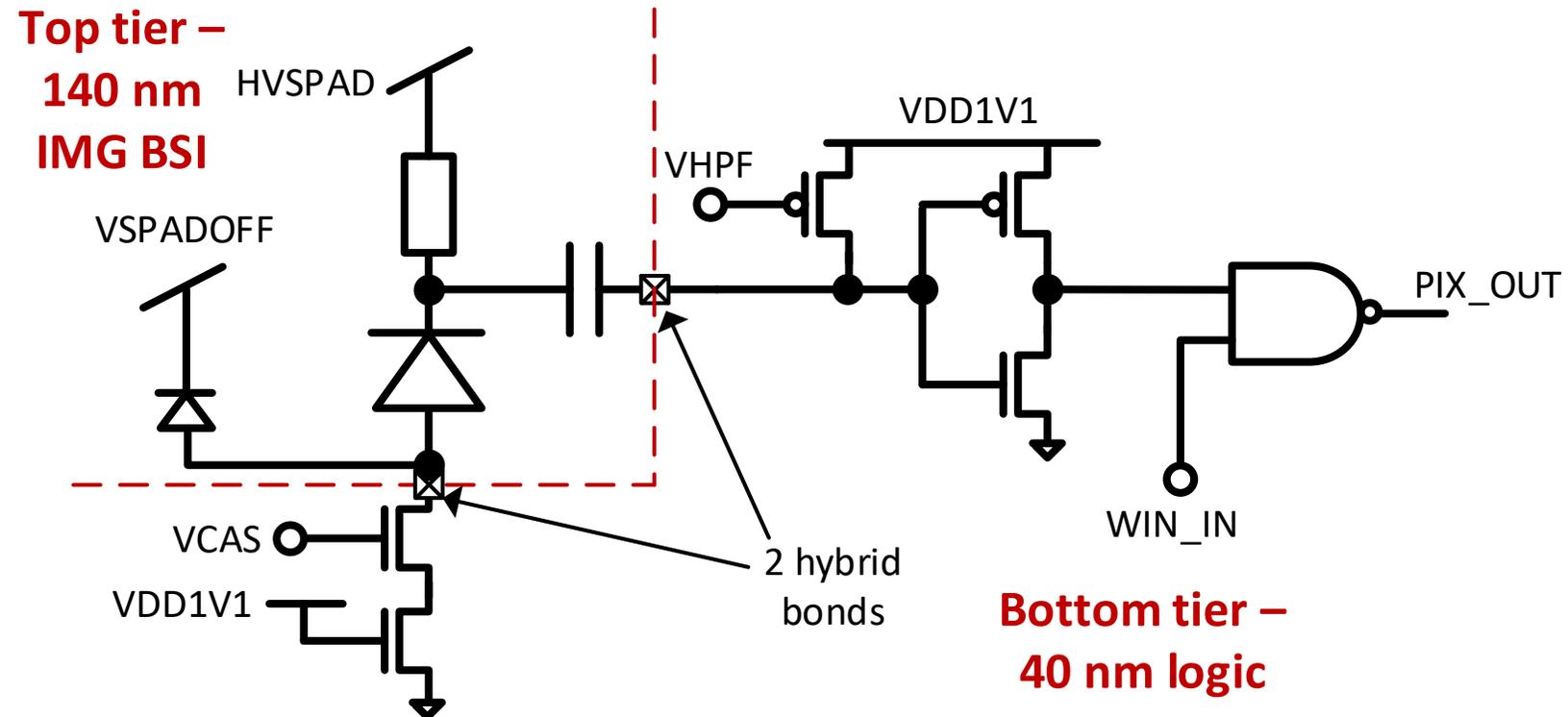- 1 flip-flop more for intensity/ToF

Coincidence detection

- Coincidence detection improves the detection range [1].

- But slows the data capture.

[1] P. Padmanabhan, "Direct time-of-flight SPAD image sensors for light detection and ranging.", EPFL thesis, 2021.

Macropixel 2

- Pixel schematics.
- Provided by STMicro up to the first inverter.
- Reference [1].

Top tier – 140 nm IMG BSI

HVSPAD

VSPADOFF

VHPF

VDD1V1

PIX_OUT

2 hybrid bonds

VCAS

VDD1V1
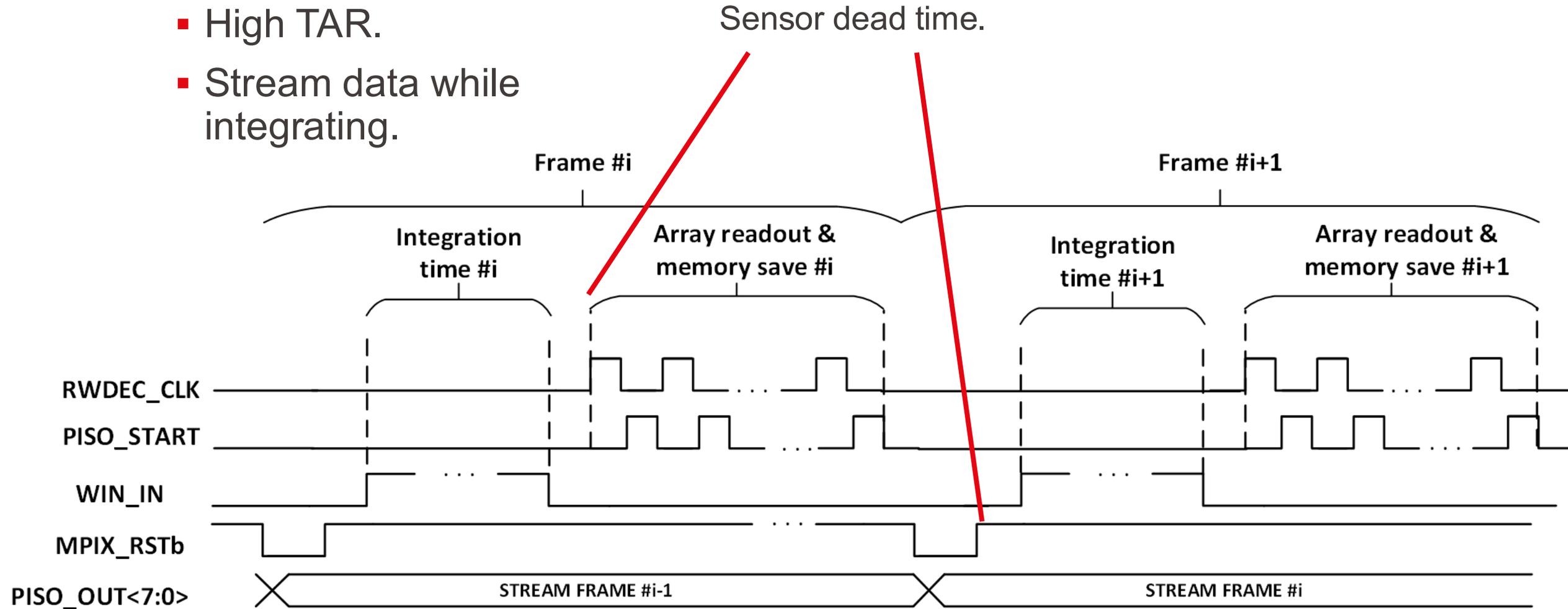
WIN_IN

Bottom tier – 40 nm logic

[1] Mamdy, B., et al. "A high PDE and high maximum count rate and low power consumption 3D-stacked SPAD device for Lidar applications." *Int. Image Sensor Workshop*. 2023.

Characterization

(a)

(b)

(c)

(d)
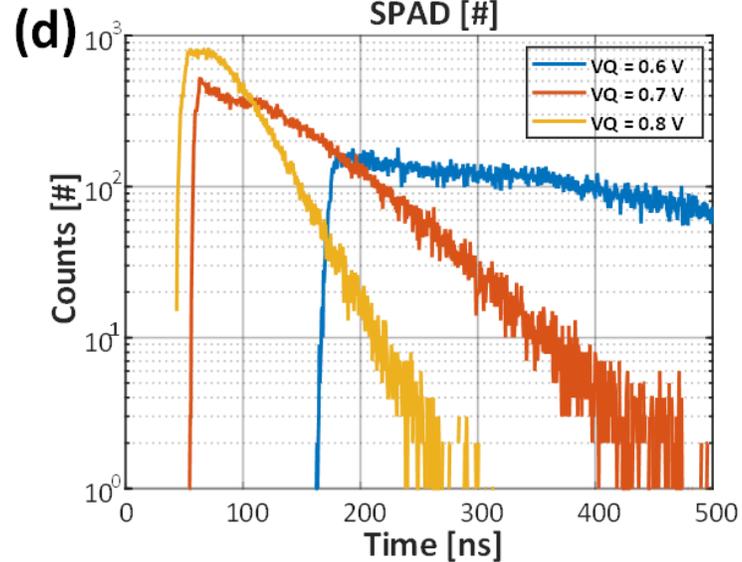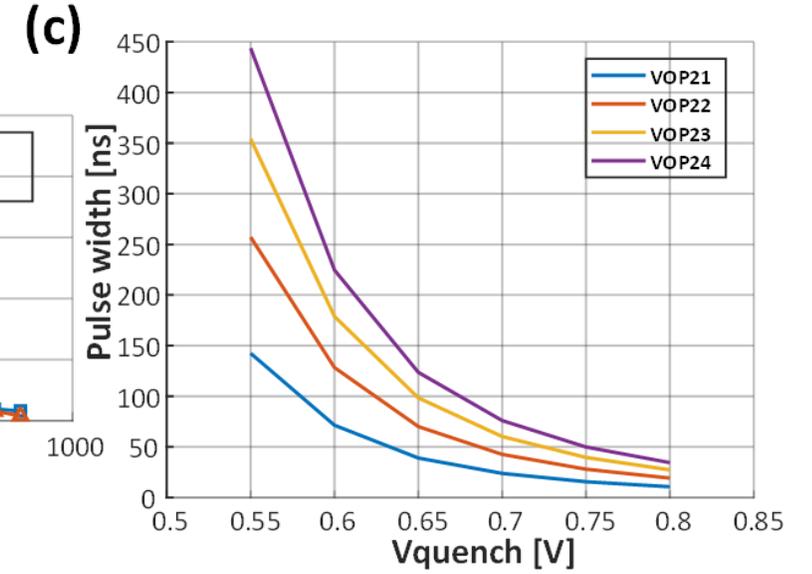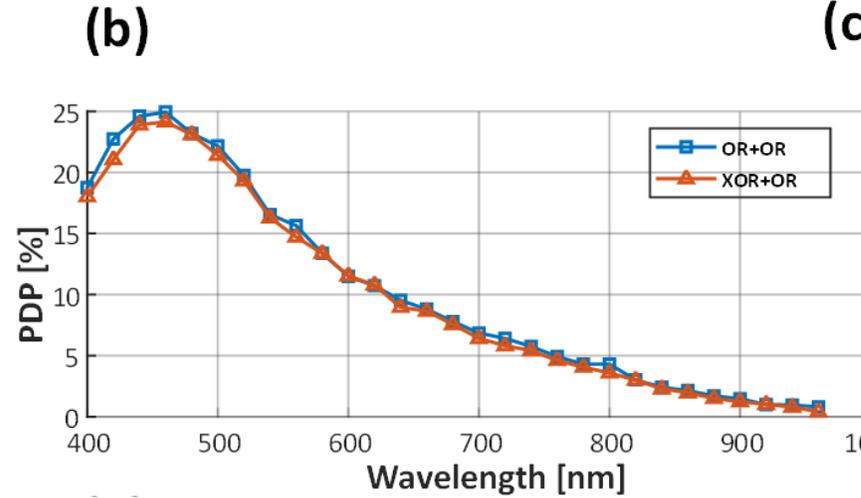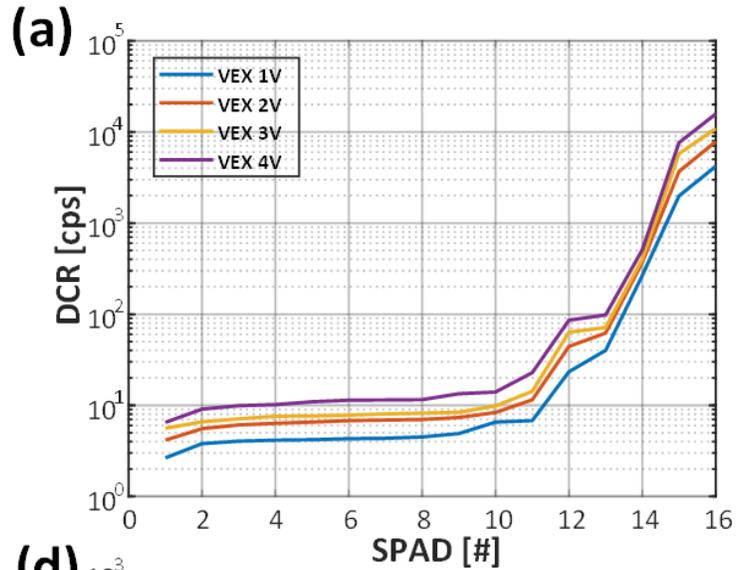
- Pulse width.
- PDP.
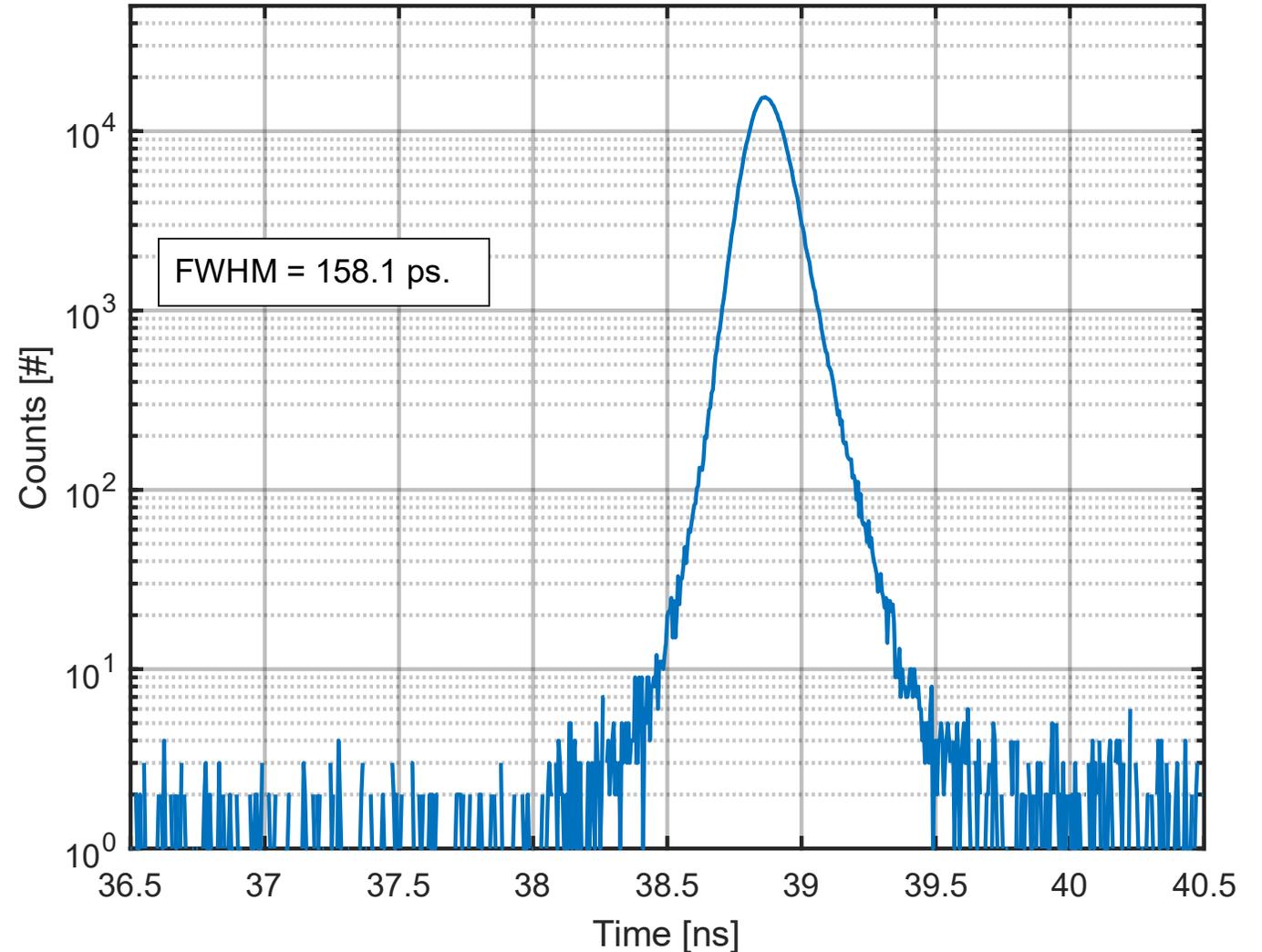- DCR.
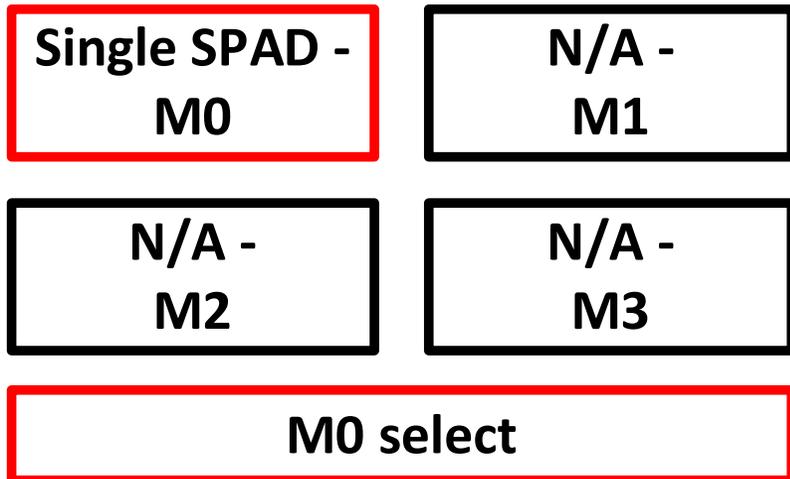- Afterpulsing (not observed).

Timing diagram

- Array readout
- High TAR.
- Stream data while integrating.

Sensor dead time.

Jitter – single SPAD

- 3 V excess bias
- Laser <80 ps pw
- TDC LSB 5 ps

Single SPAD - M0	N/A - M1
N/A - M2	N/A - M3

M0 select

FWHM = 158.1 ps.

Jitter – 4 SPADs OR

- 3 V excess bias
- Laser <80 ps pw
- TDC LSB 5 ps

OR - M0	N/A - M1
N/A - M2	N/A - M3

M0 select

FWHM = 675.4 ps.

Jitter – 16 SPADs OR
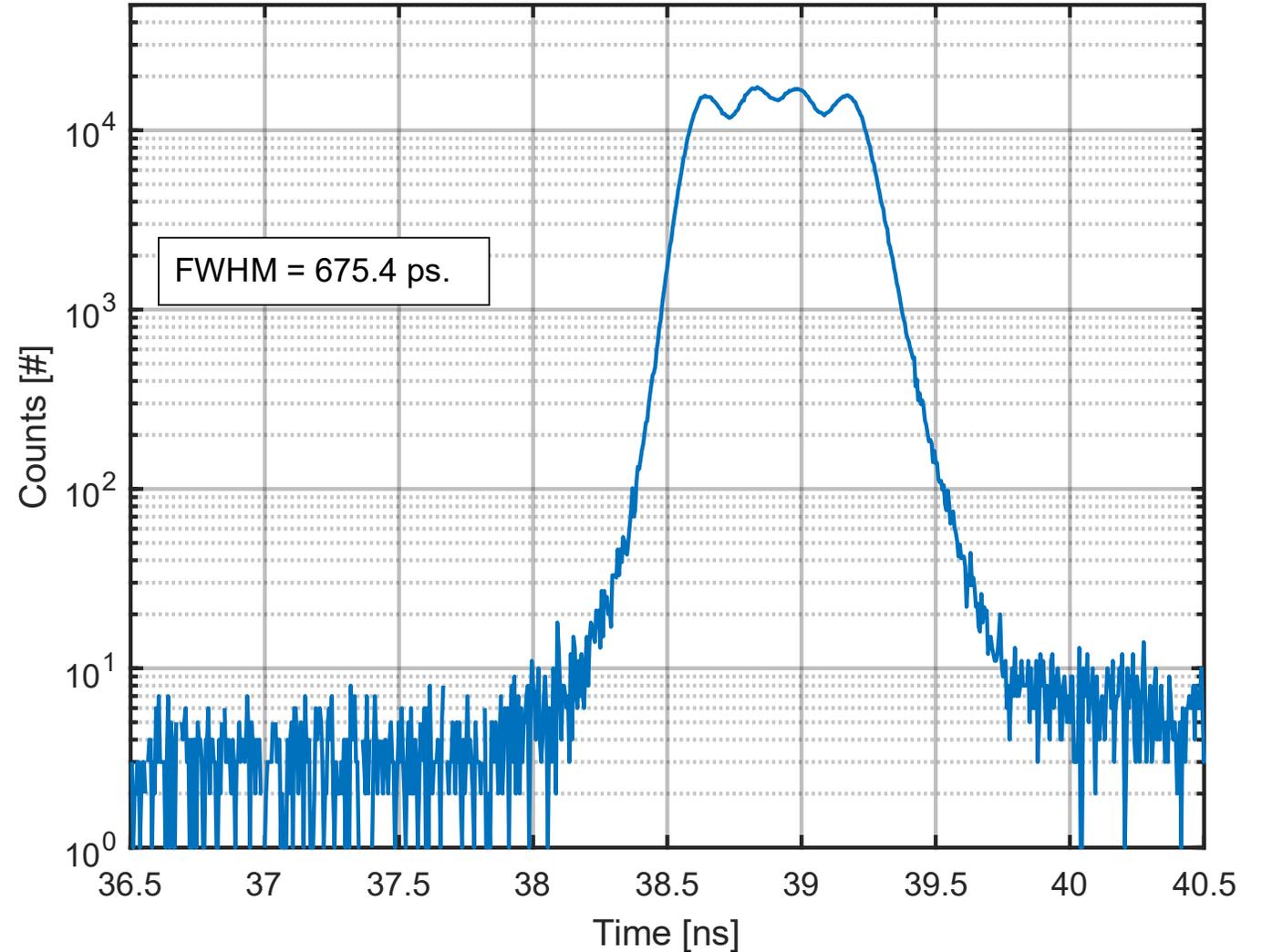
- 3 V excess bias.
- Laser 40 ps pw.
- TDC LSB 5 ps.

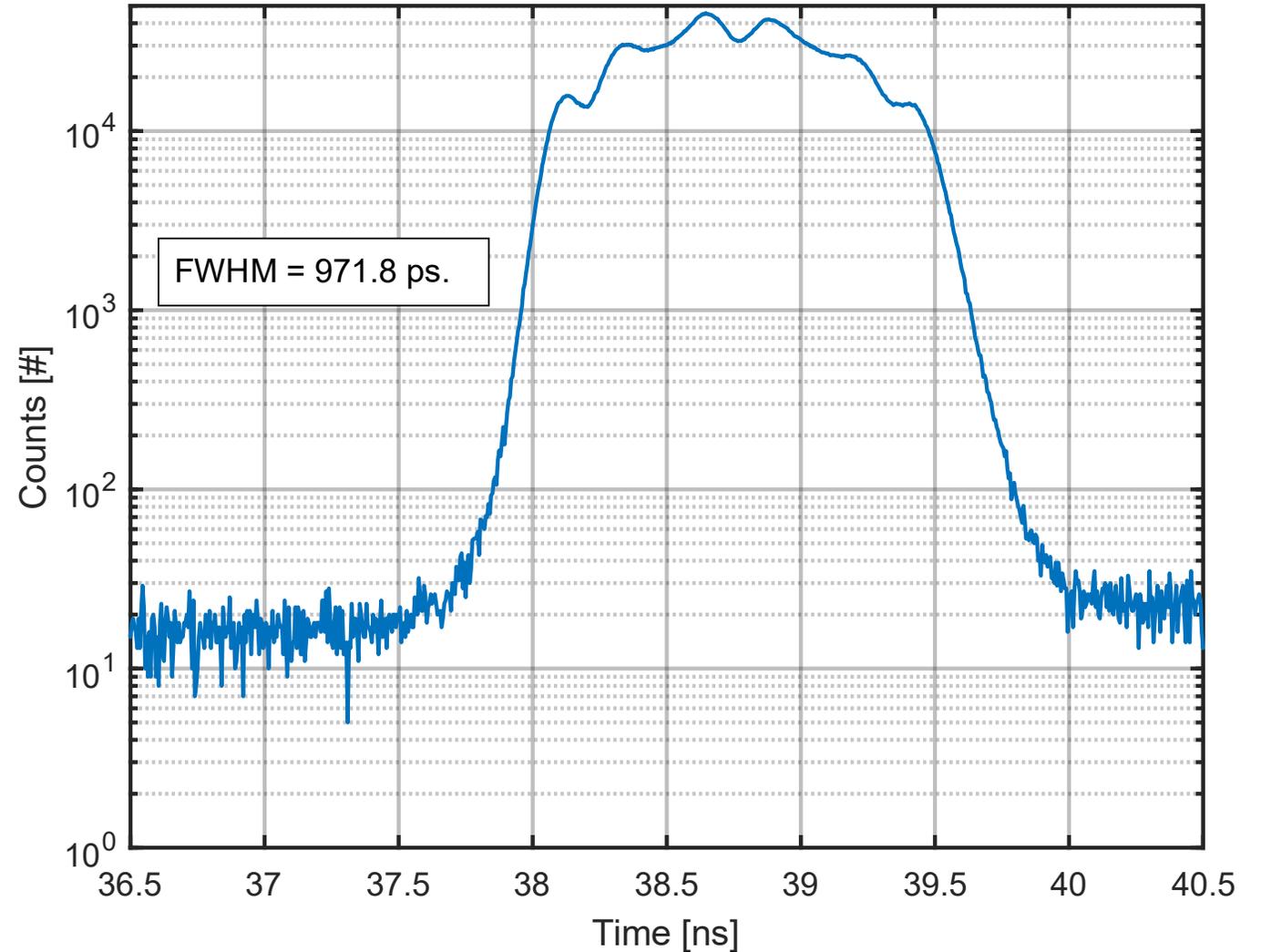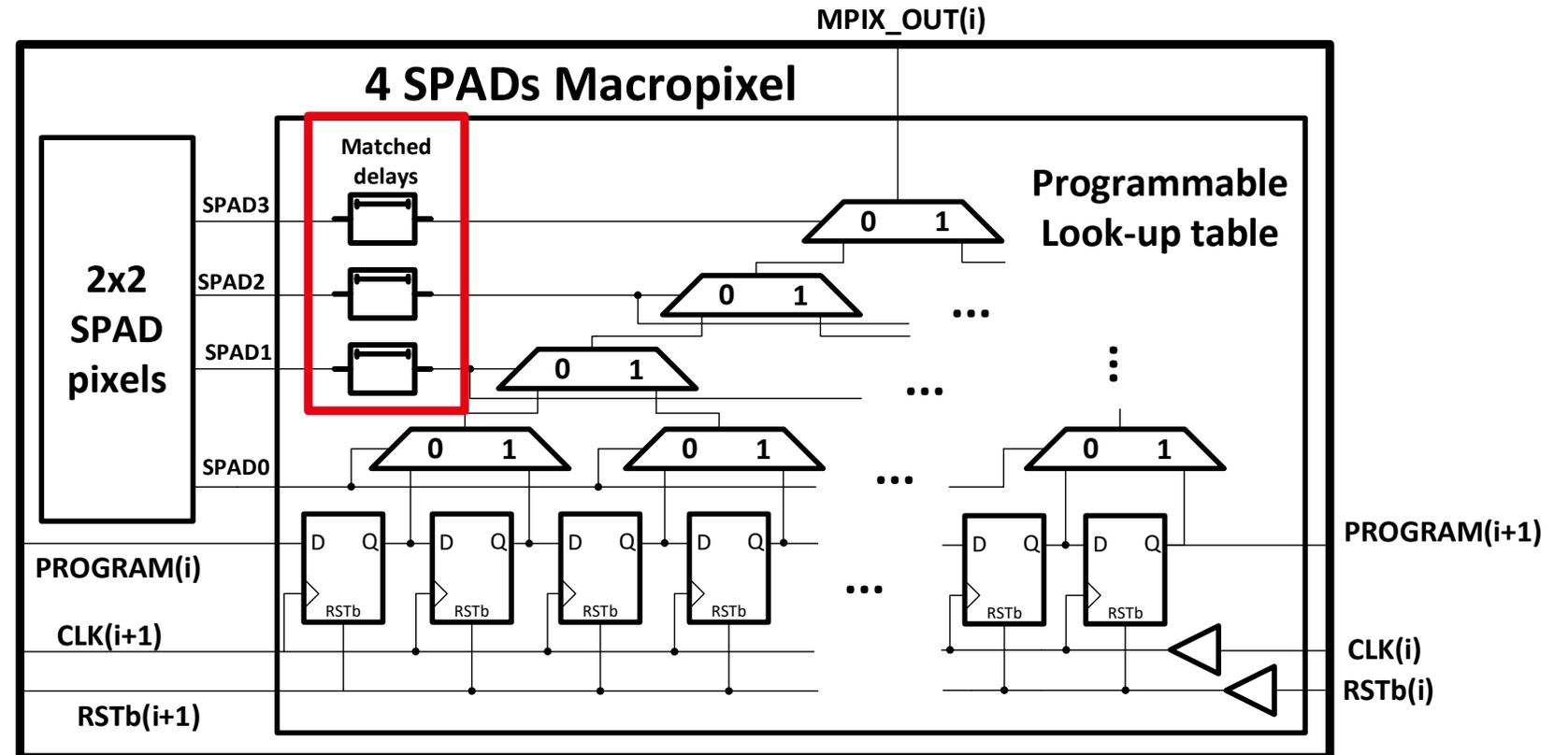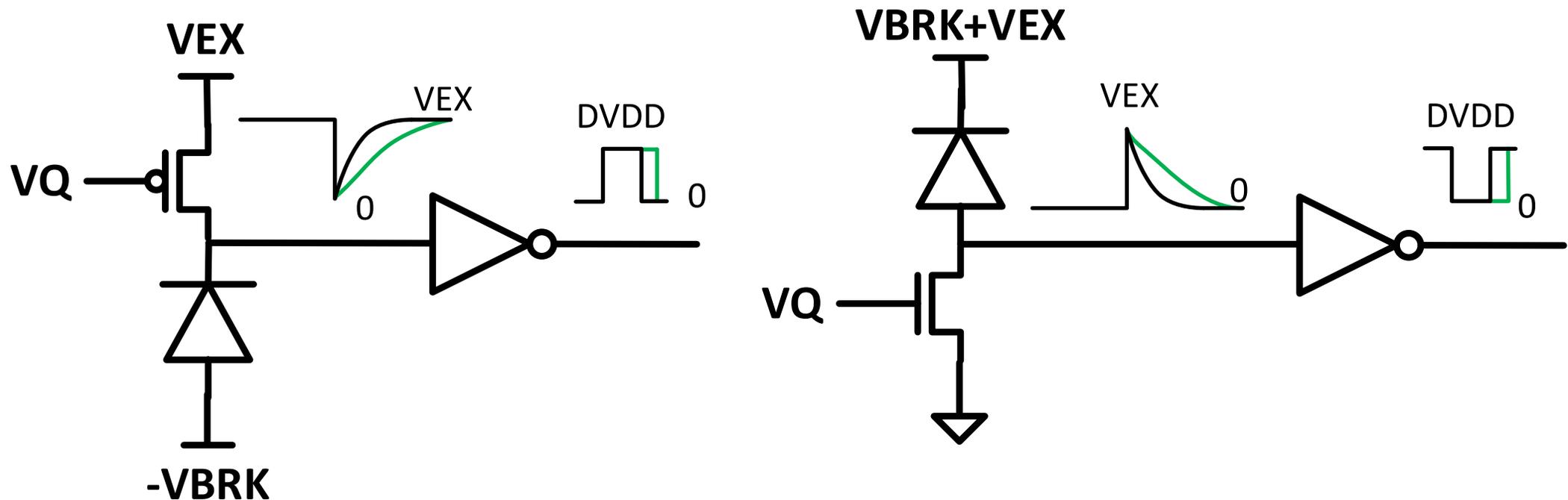| OR - M0	OR - M1
OR - M2	OR - M3
OR

FWHM = 971.8 ps.

Dummy correction for timing optimization

- Future implementations
- Avoid timing mismatch
- For timing sensitive applications

SPAD operation

- Photon-to-digital conversion
- SPAD gain > 10^5
- Imaging device suited for **digital processing**

Passive quenching and passive recharge

XOR – background estimation

- Maximum countrate – XOR configuration.