# Advanced Active Deep Trench Designs for Enhanced Charge Transfer Performances in CCD-on-CMOS Image Sensor

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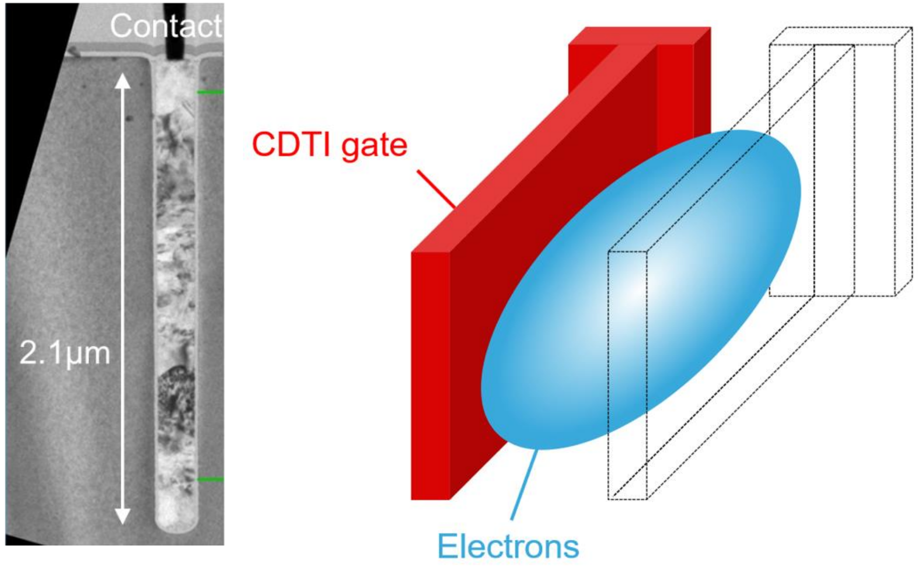
# 1 – Introduction

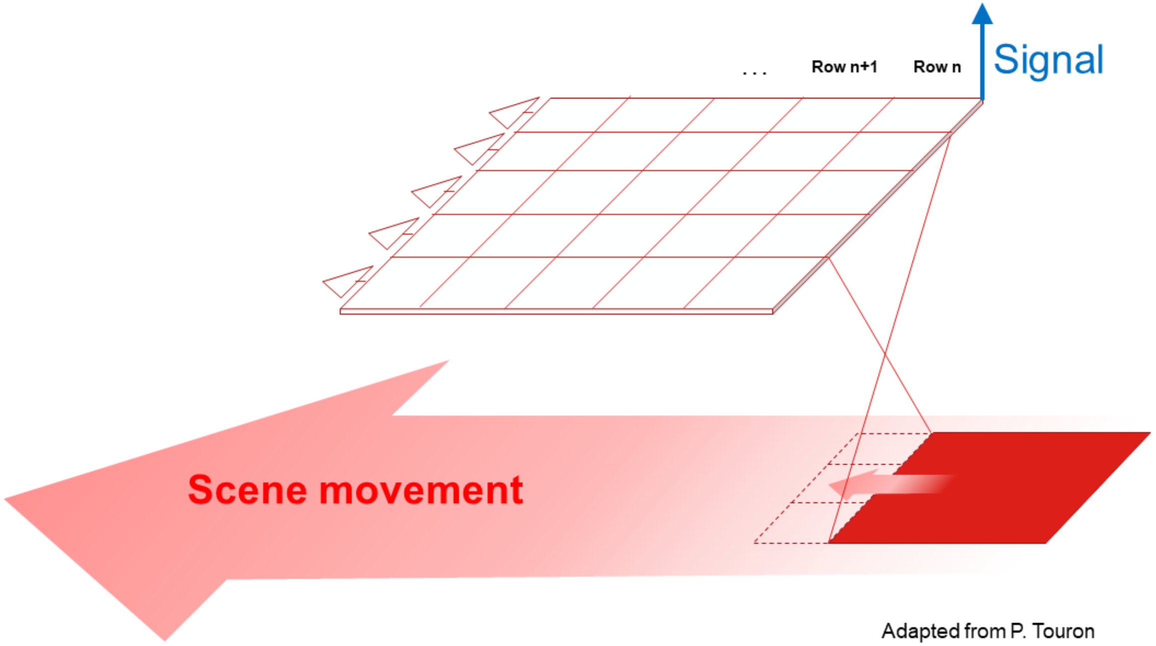
## CCD-on-CMOS applications

- Efficient and reliable charge transfer in a modern CMOS process :
  - Ease of integration,
  - Access to advanced tech nodes,
  - Low-power dissipation,
  - CMOS function / combination possibilities,
  - Rad-hard,
  - …

- P. Touron et al. « Capacitive Trench-Based Charge Transfer Device », *IEEE EDL*, 2020 :



- Time Delay Integration (TDI) : **Remote sensing** and **Machine vision** applications.

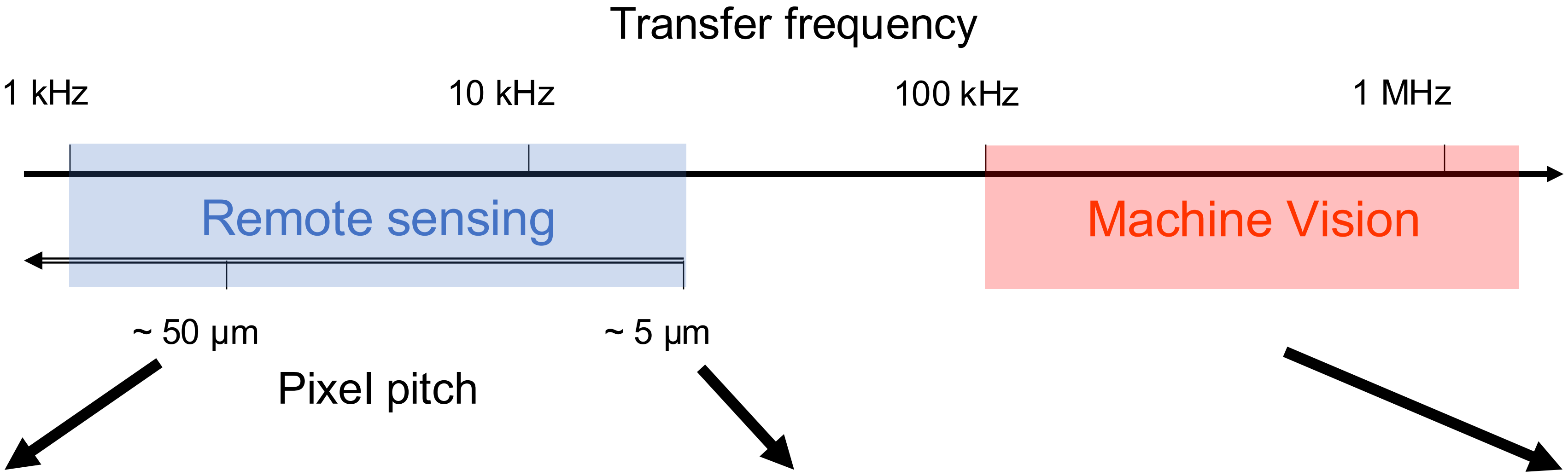


Adapted from P. Touron

- + many possible scientific and medical applications (DNA sequencing, multispectral imaging…)

# 1 – Introduction

## Current knowledge on Active Deep Trench CTE



Transfer frequency

1 kHz

10 kHz

100 kHz

1 MHz

Remote sensing

Machine Vision

~ 50 µm

~ 5 µm

Pixel pitch

✗ Inefficient transfer in large pixel because of the travel distance

✗ High dark current / total noise because of long phase opening

✓ Efficient transfer in reasonably sized pixels ($\leq 20\ \mu\mathrm{m}$)

− Sub-optimal dark current and noise performance

✗ Inefficient transfer because of short phase opening

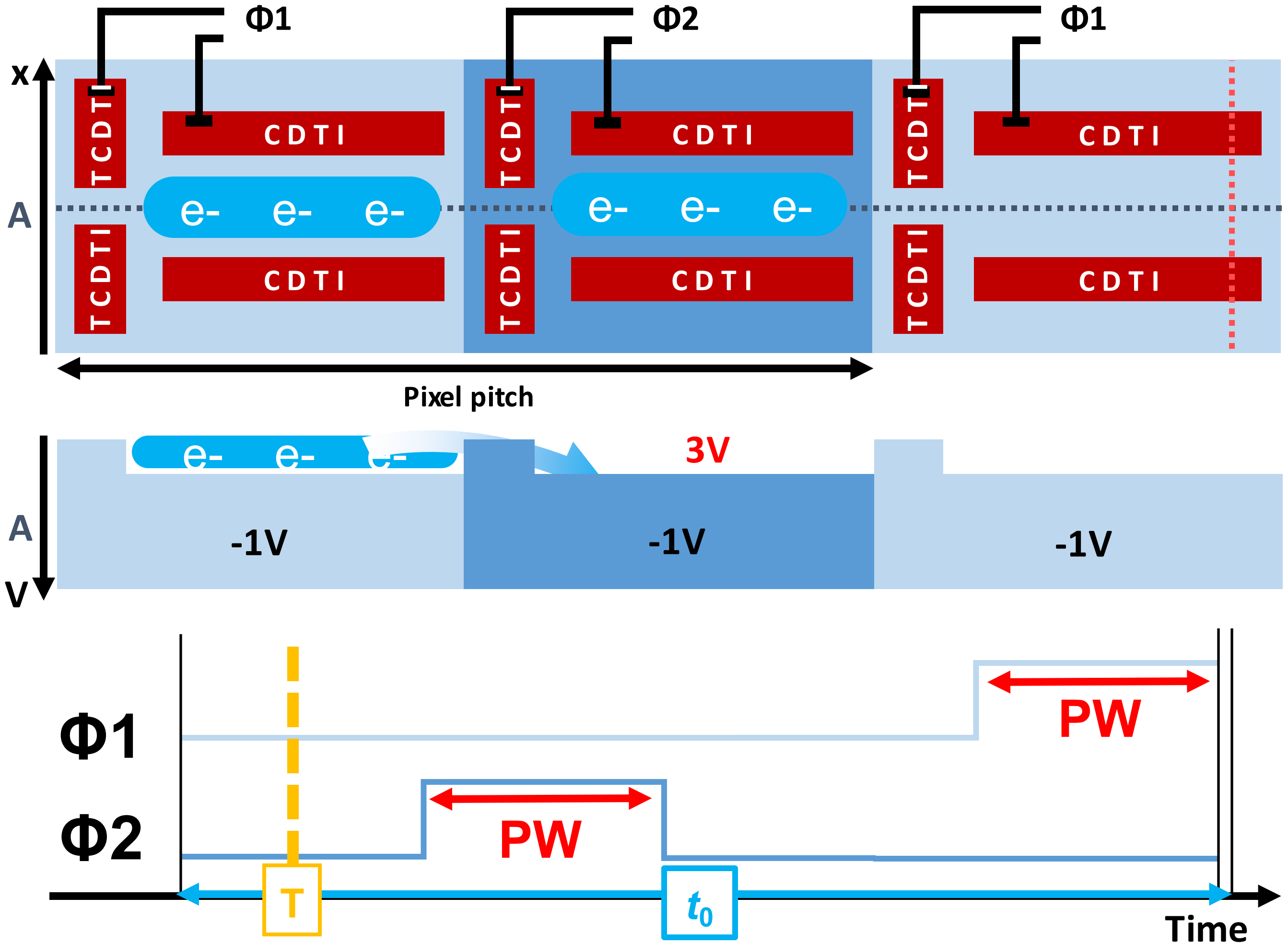
✓ Low dark current / total noise because of short phase opening

**Can charge transfer be improved in large pixels while keeping dark current low ?**

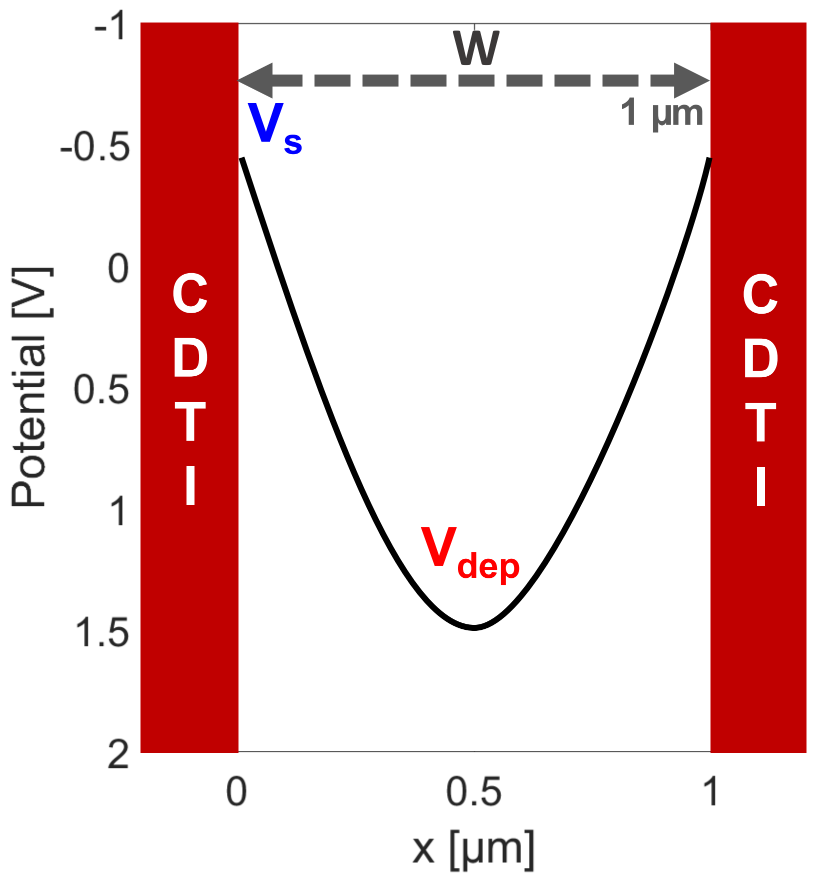
**Can charge transport be accelerated by design ?**

# 2 – Device Description

## Charge Transfer Operation



$$U(x) = \frac{-N_d q}{2\epsilon}(x^2 - \boldsymbol{W}x) + \mathbf{V_s}$$

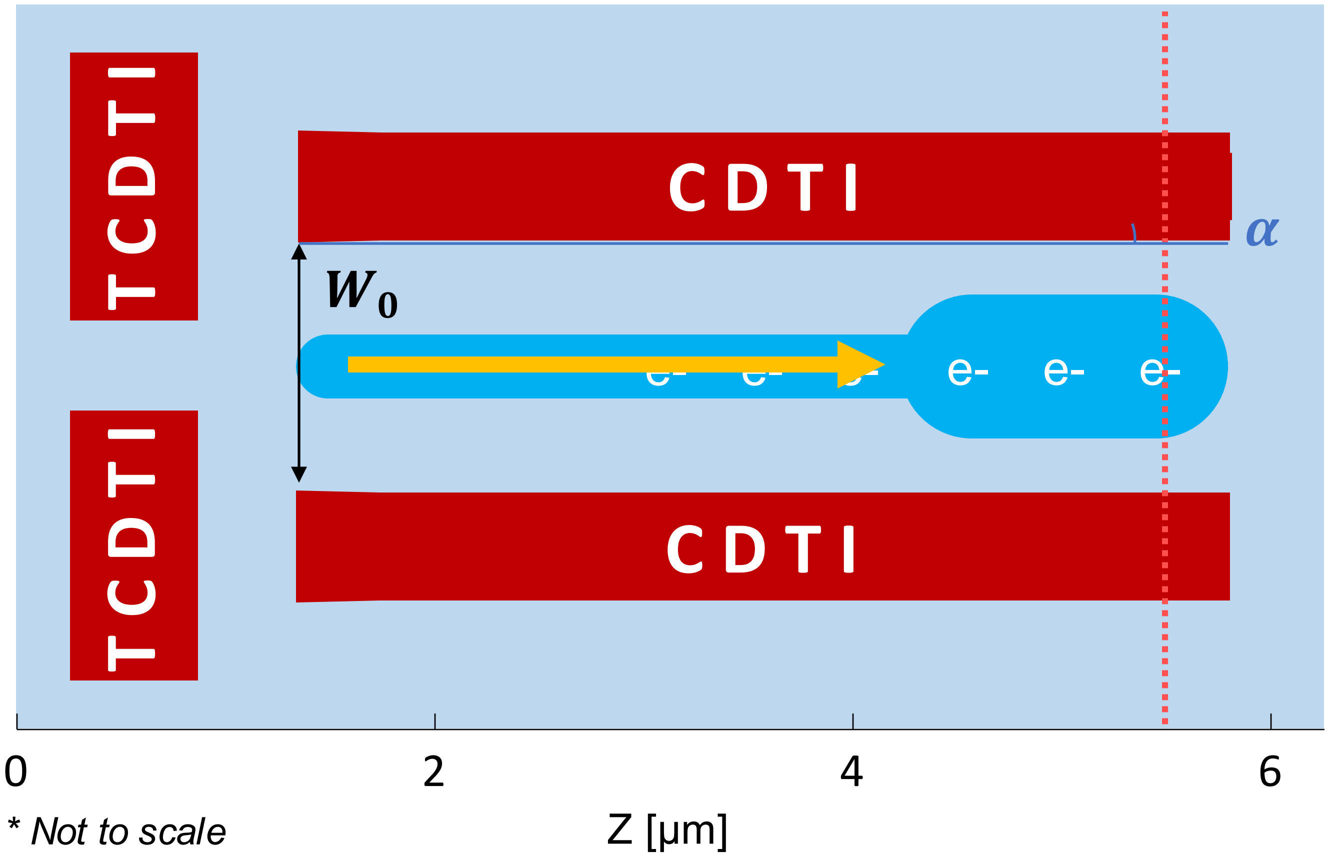


# 2 – Device Description

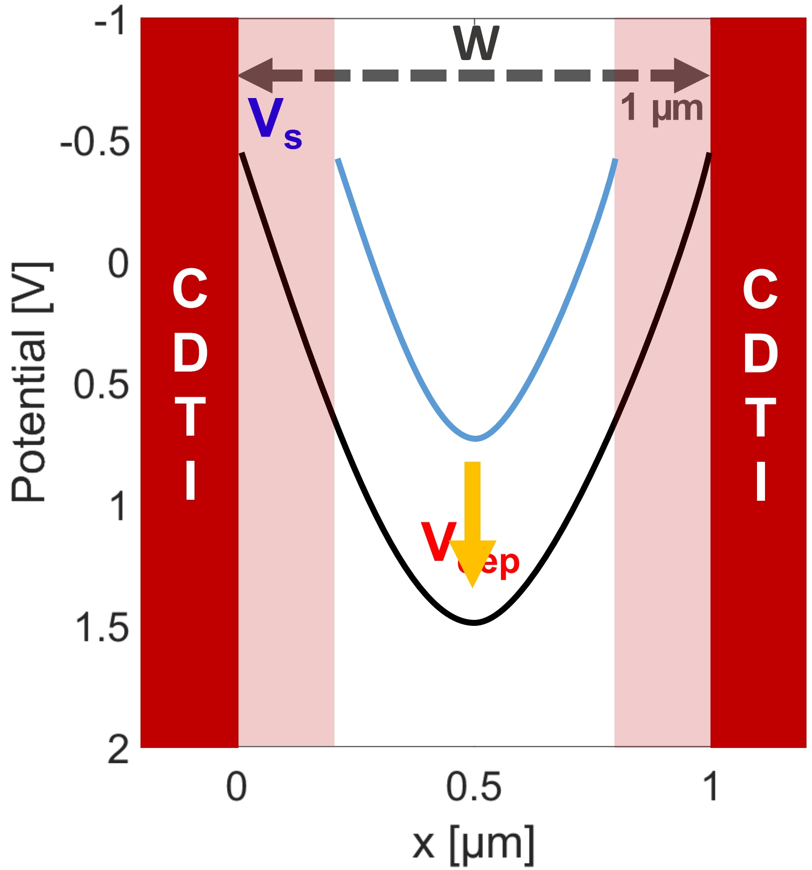
## Trapeze-shaped CDTI gates

**In-pixel voltage drop → electric field** $\simeq$ 1 kV/cm in a 6 µm phase

$$\mathrm{E}(z) = \frac{-N_d q}{4\epsilon}\left(\boldsymbol{\alpha}^2 z + \boldsymbol{\alpha} \boldsymbol{W_0}\right)$$



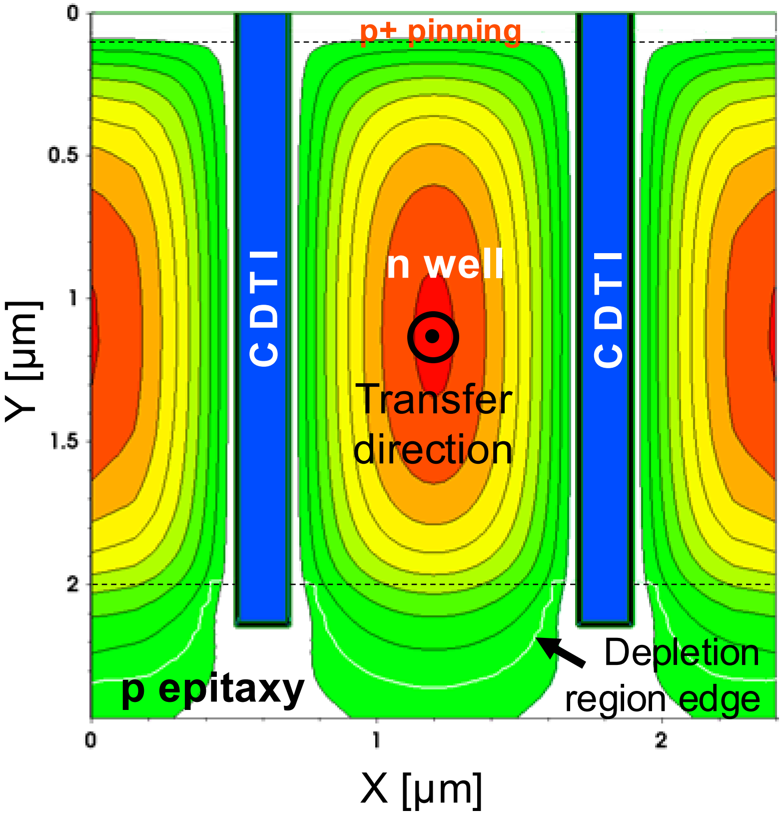
* *Not to scale*



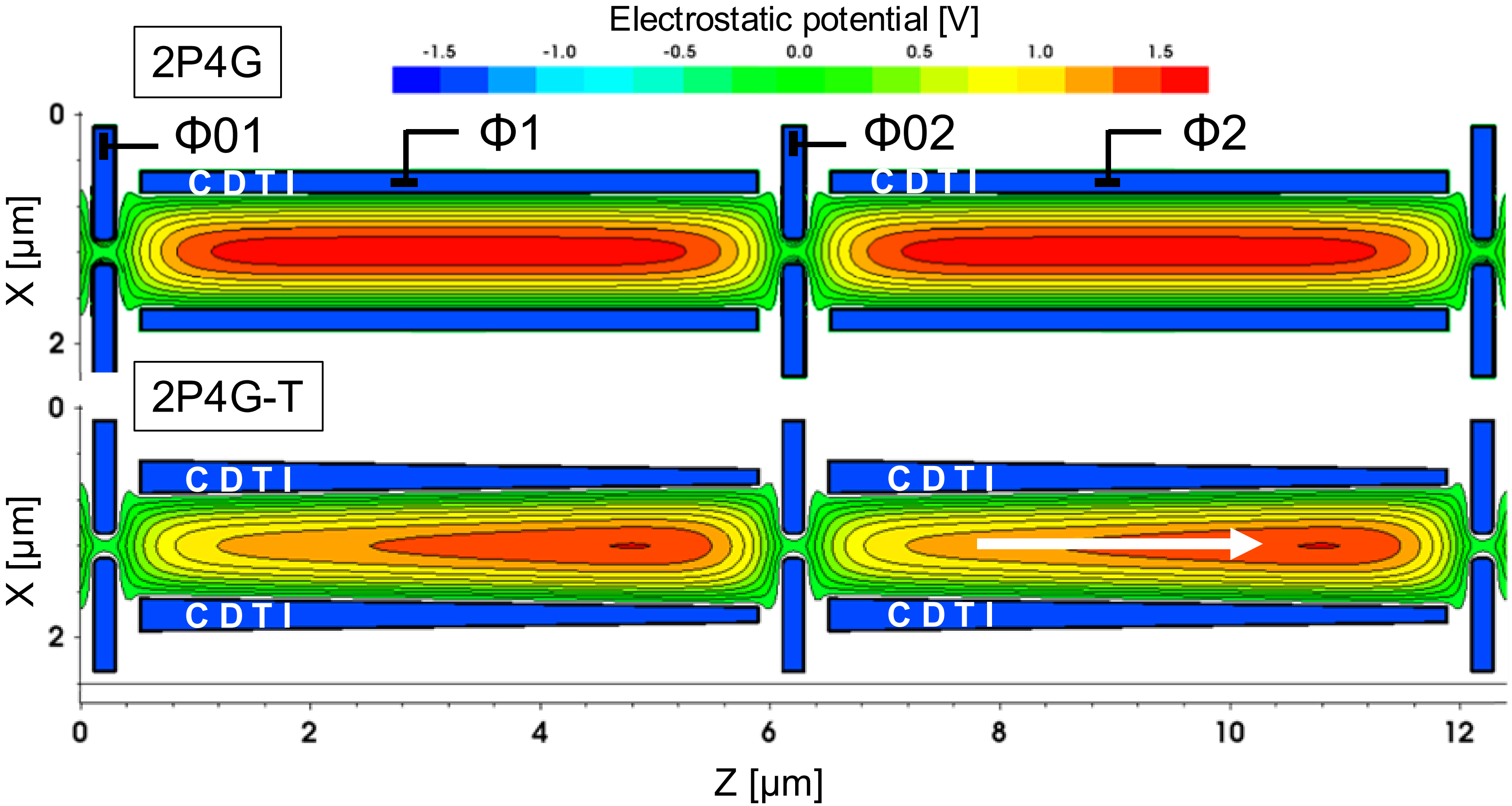
# 2 – Device Description

## TCAD potential cross-section views

**Cross-section view**



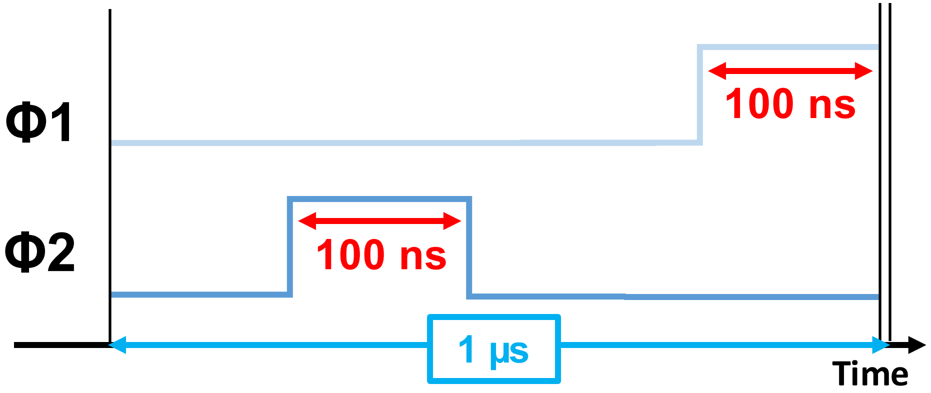
**Top view**

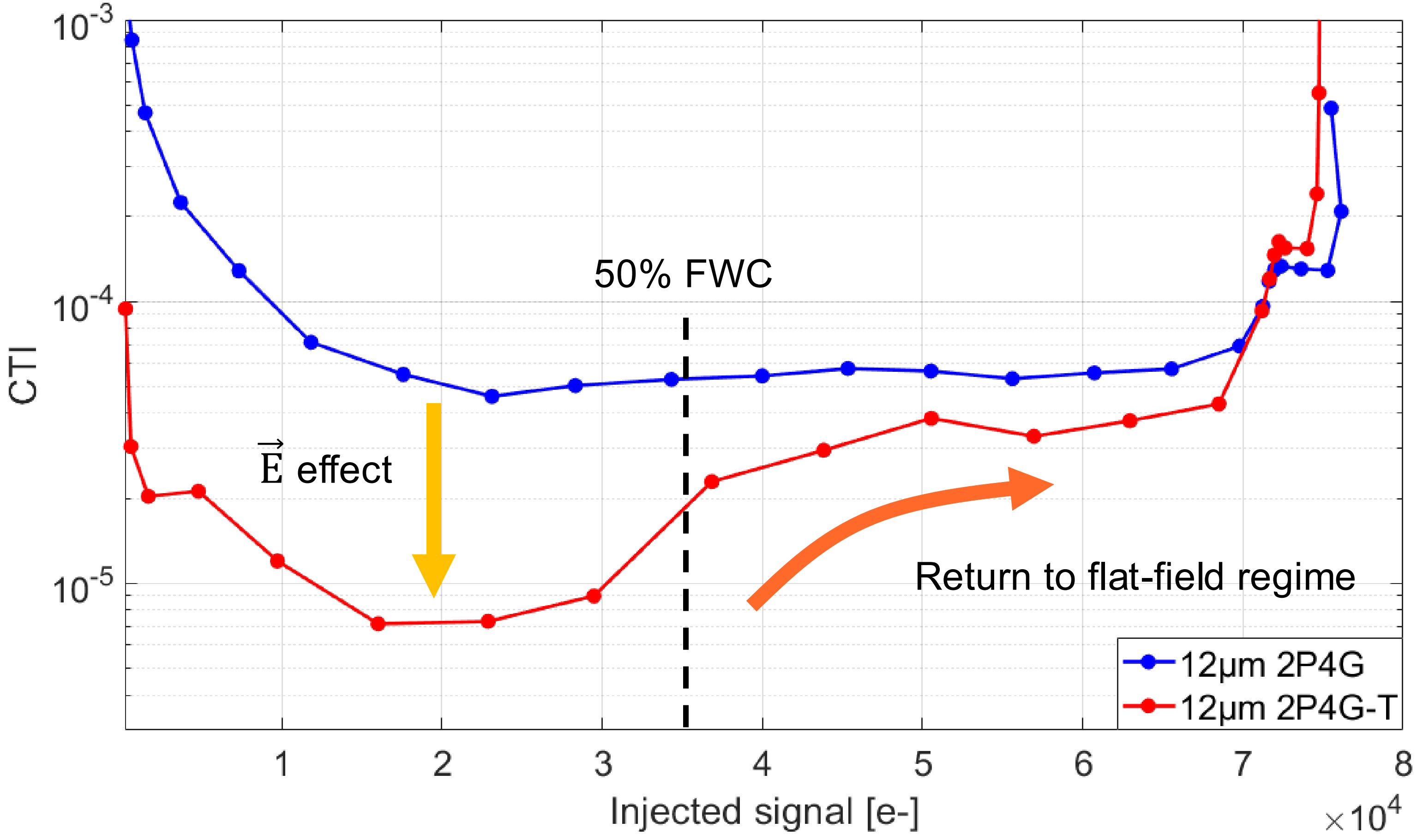


# 3 – Results

## CTI vs Signal improvements

- Line frequency : 100 kHz
  - **T0** = 1 µs ; **PW** = 100 ns
- Pixel pitch : **12 µm**



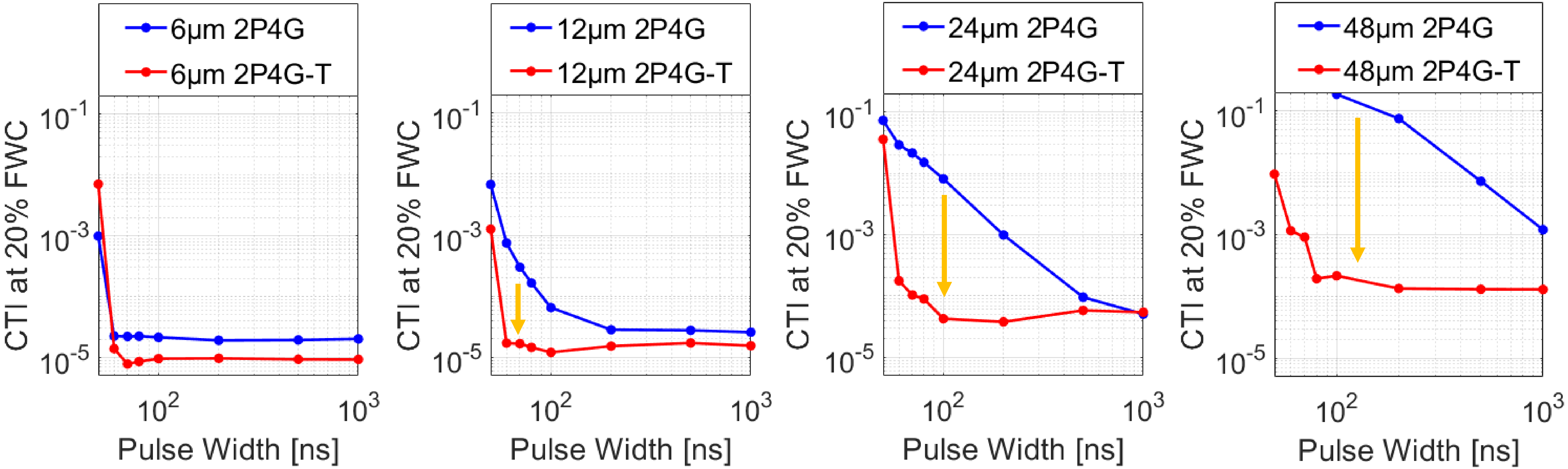


○ With **trapeze-shaped CDTI**, the CTE improves significantly for signals below 50% FWC. Then, as the pixel fills-in with electrons, the **electric field** fades out and CTI returns to a typical value.

# 3 – Results

## CTI vs Pulse Width

- Signal injection at <u>20% FWC</u>



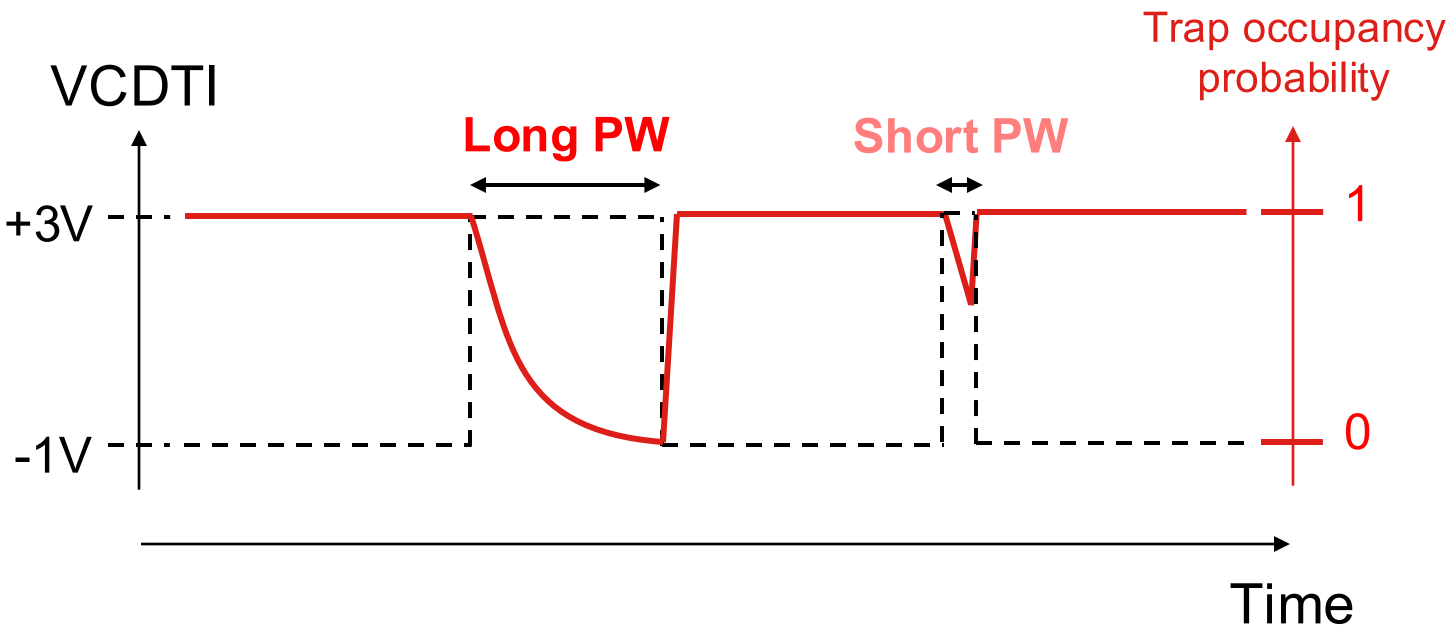
○ **In pixels ≥ 12 µm**, charge transfer appears limited by transfer time (**PW**). However, with trapeze-shaped CDTI, efficient charge transfer can be achieved at a **much faster rate**, particularly in larger pixels.

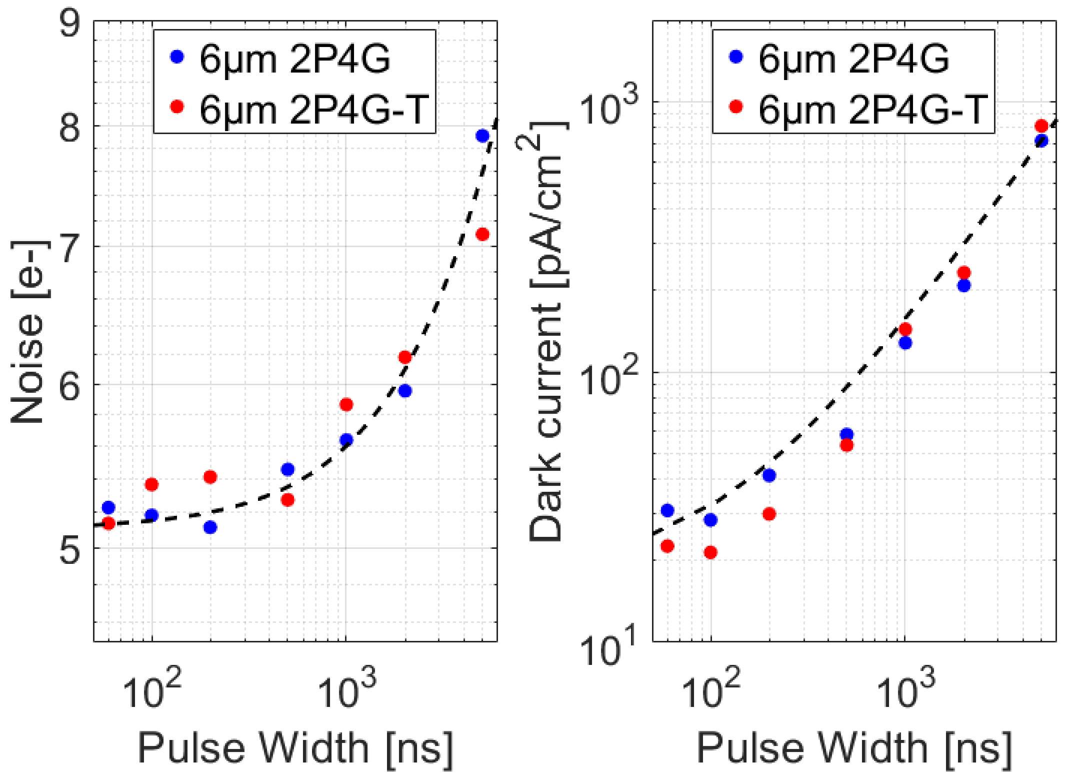
# 3 – Results

## Dark current and Noise vs Pulse Width

- Transfer speed is also a matter of dark current

➔ *dynamic trench interface passivation.*

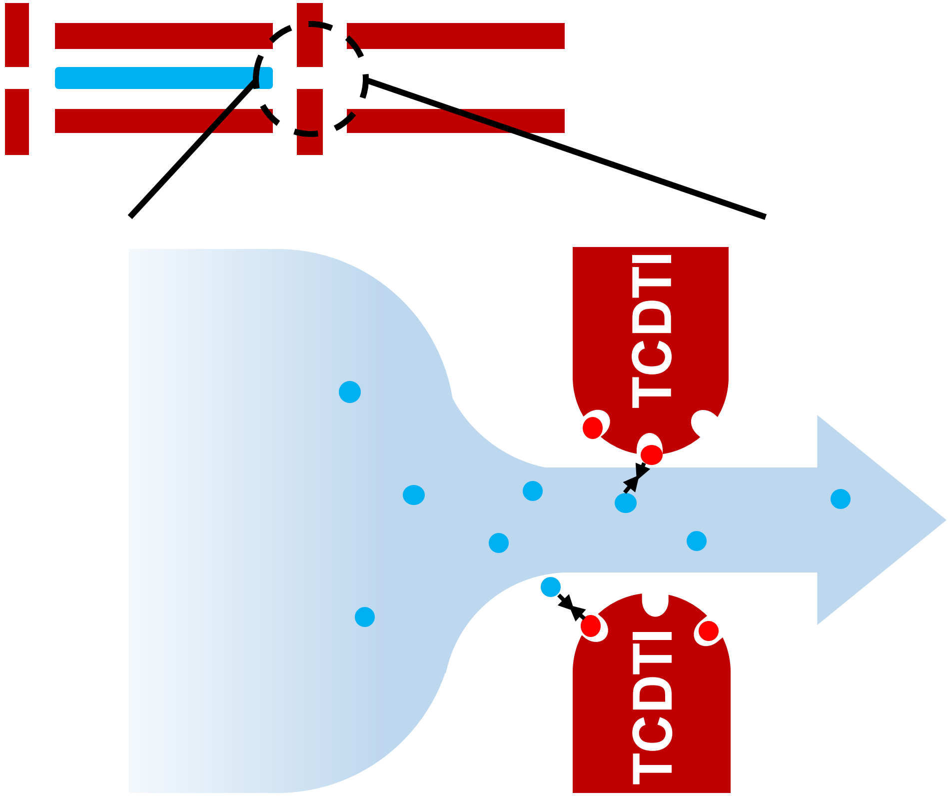




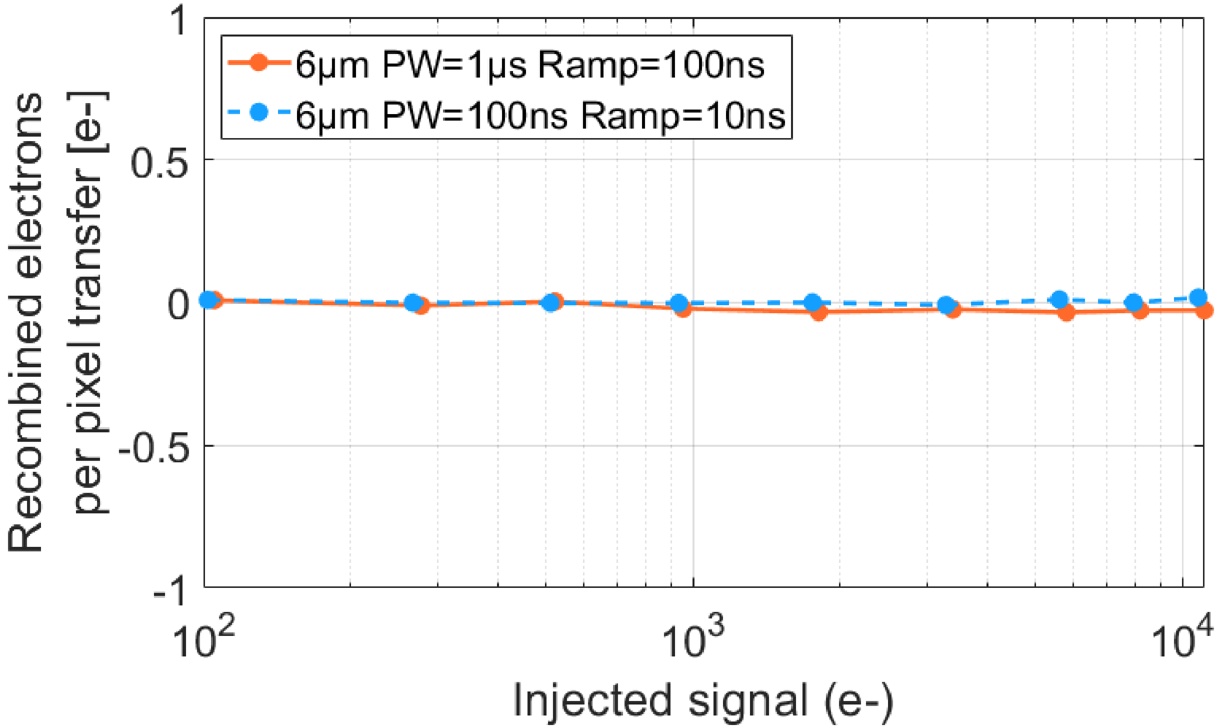
○ With very **short PW (≤ 100 ns)**, interface trap occupancy remains high (no detrapping). As such, **minimum noise and dark current** is achieved together with **efficient charge transfer**.

# 3 – Results

## Interface charge recombination



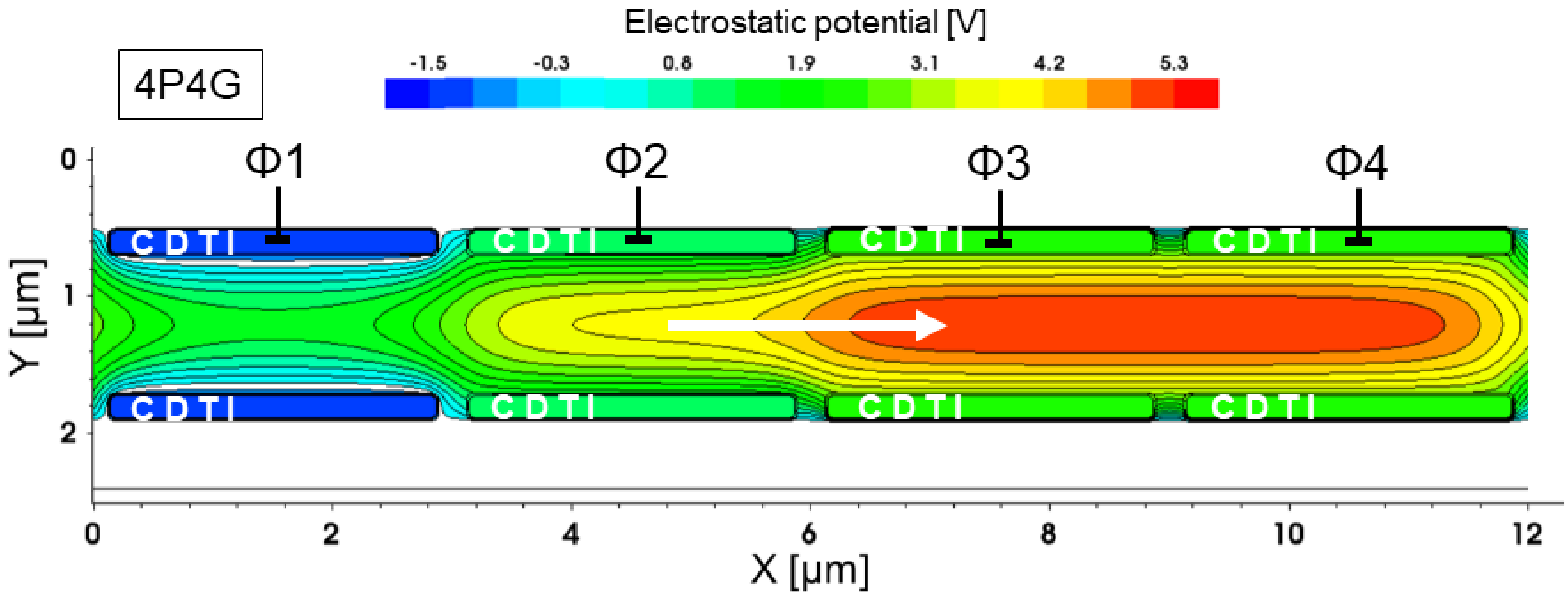
- TCDTI Recombination ? ➔ Comparison of the output signal in **Inverted Mode (IMO)** and **Non-Inverted mode (NIMO)** :



○ The use of very short PW raises concerns about possible spurious interface trap recombination at the TCDTI interface. However, a comparison between **IMO** and **NIMO** shows no signal output difference.

# 4 – Perspectives

## Toward a four-phase buried channel alternative



# 5 - Conclusion

- Trapeze-CDTI CCD-on-CMOS designs show strong potential for **high line rate, high dynamic range** applications:
  - Improvements in CTI for transfer time below 1 µs, especially for large pixels ➔ **TDI Remote sensing**.
  - Multi-MHz charge transfer achievable ➔ **TDI machine vision**.
  - Low noise, low dark current and negligible interface charge recombination.

| | 2P4G<br>PW = 1 µs | 2P4G<br>PW = 100 ns | 2P4G-T<br>PW = 100 ns | Teledyne Dalsa<br>[IISW 2023] | IMEC<br>[IISW 2017] |
|---|---|---|---|---|---|
| Nb. pixels | 220 | 220 | 220 | 256 | 256 |
| Pixel pitch [µm×µm] | 3×12 | 3×12 | 3×12 | 2×5 | 5.4×5.4 |
| Nb. phase | 2 | 2 | 2 | 4 | 4 |
| Line rate [kHz] | 100 | 100 | 100 | Up to 3000 | Up to 200 |
| Minimum CTI | $2\times10^{-5}$ | $5\times10^{-5}$ | $7\times10^{-6}$ | $< 10^{-5}$ | $< 10^{-5}$ |
| Full well charge [ke-] | 70 | 70 | 68 | > 60 | LG 12.8 / HG 31.6 |
| Dark current [nA/cm$^2$] | 0.13 | 0.025 | 0.025 | < 4 | 5.6 |
| Noise [e-] | 5.6 | 5.2 | 5.2 | 20 | LG 10 / HG 40 |
| Dynamic range [dB] | 81.9 | 82.6 | 82.3 | 69.5 | LG 62 / HG 60 |

# Thank you for your attention

## IISW 2025

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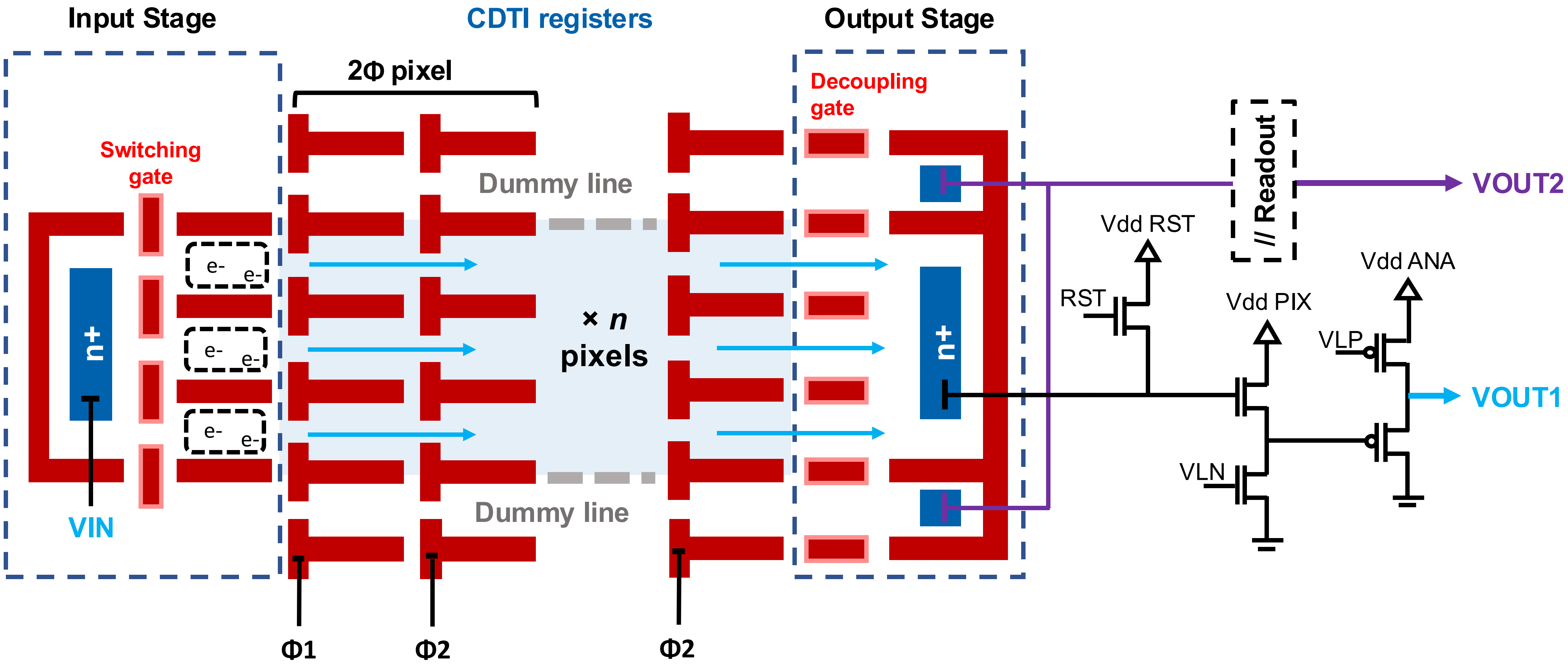
# Backup Slides

# Experimental details

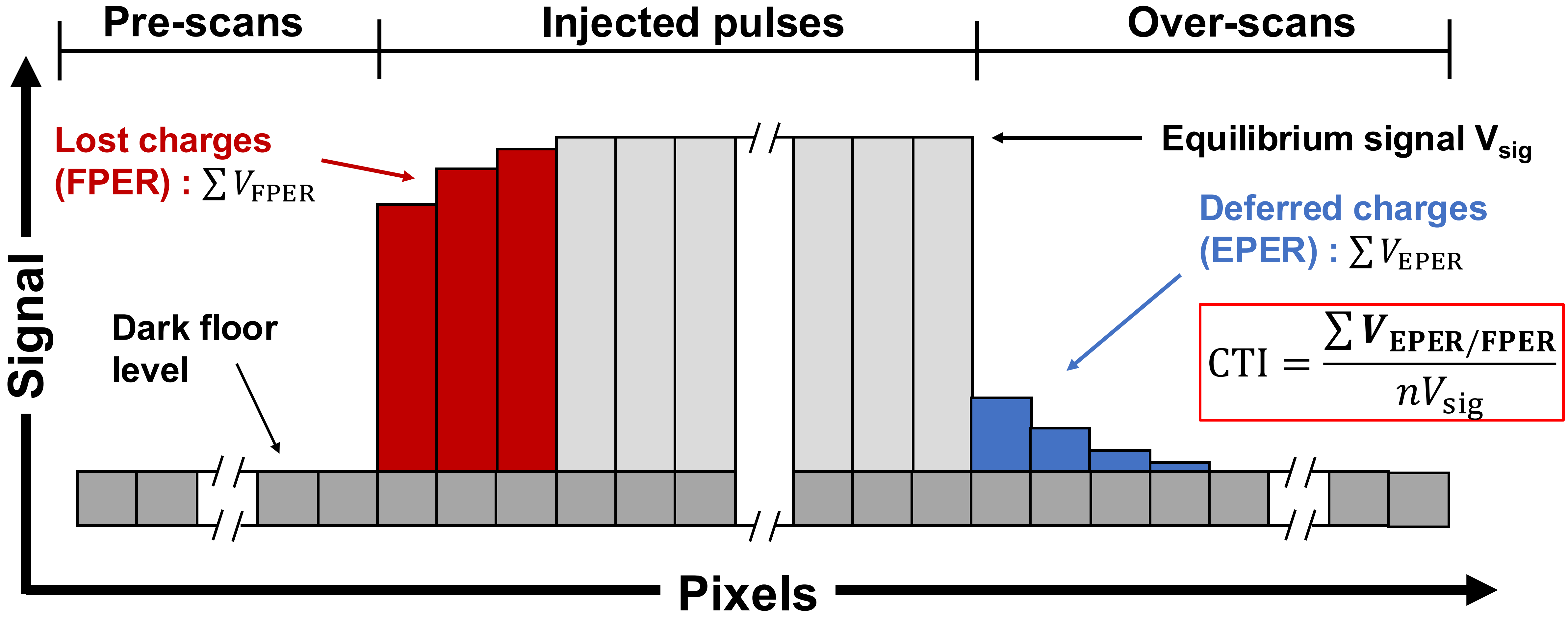
## The complete test structure



- The test structure is composed of 3 paralell rows of ***n* pixels** enclosed in between an **input stage** and an **output stage** followed by a simple readout circuit. The structure is also equipped with dummy lines.

# Experimental details

## Charge Transfer Inefficiency (CTI)



$$\mathrm{CTI} = \frac{\sum V_{\mathrm{EPER/FPER}}}{nV_{\mathrm{sig}}}$$

- Charge Transfer Inefficiency is measured using the missing charges in the edge of the pulses (**FPER**) and the deferred trail following the pulses (**EPER**) in a single sequence.