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An 8.7 Mpixel 240fps CMOS Image Sensor with 4 × 4 Pixel-Block Local Adaptation of Resolution, Frame Rate, and Exposure Time for Scene Adaptive Imaging

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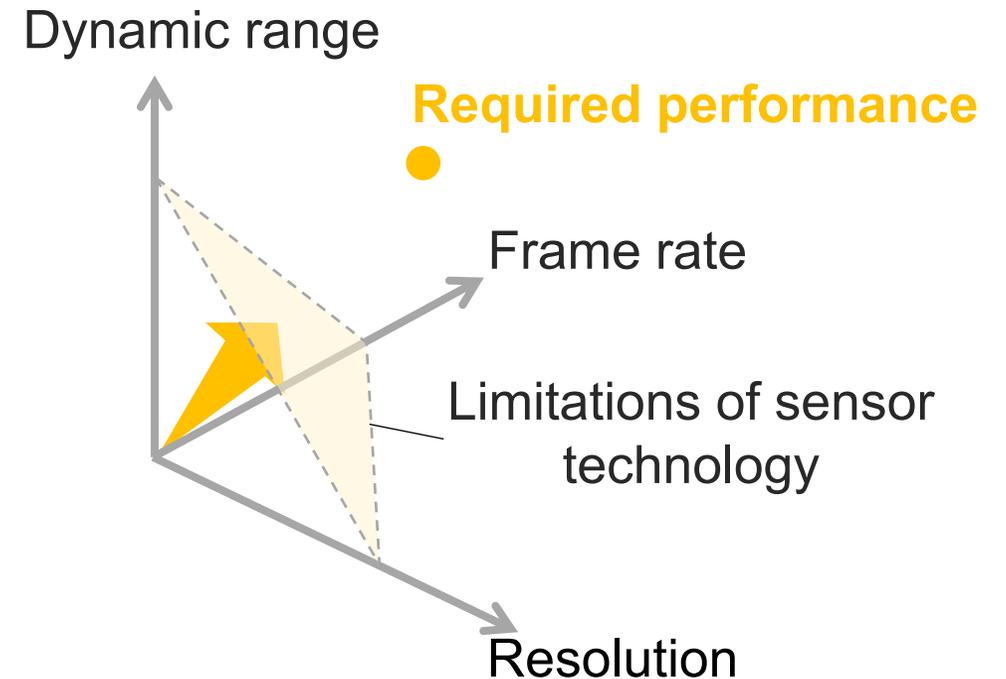1 NHK Science & Technology Research Laboratories, Tokyo, Japan
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Challenges in Capturing High-Quality Wide Field of View Video

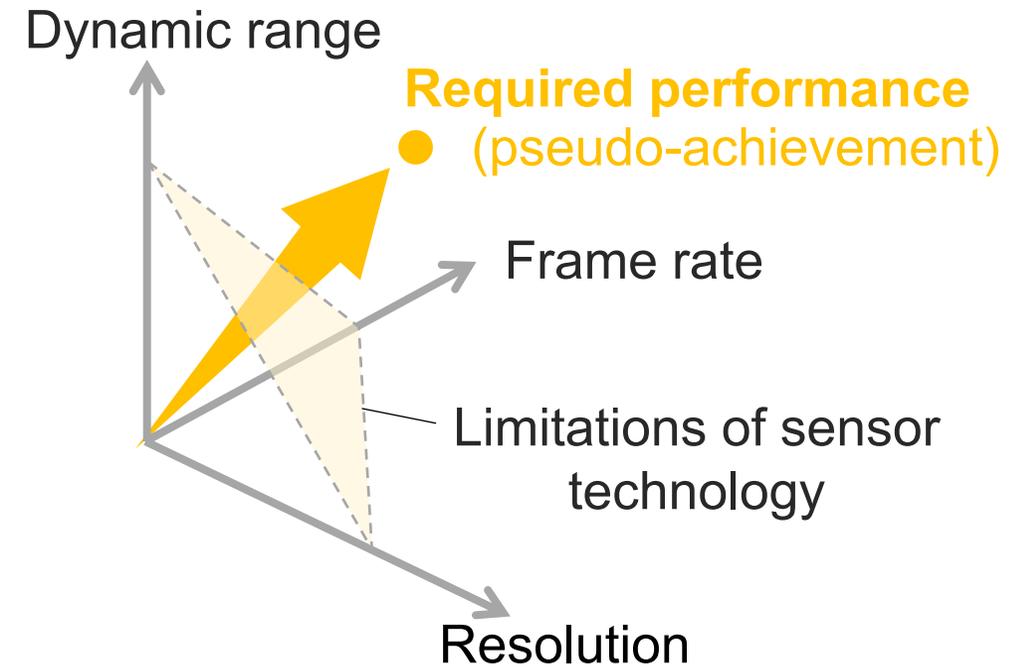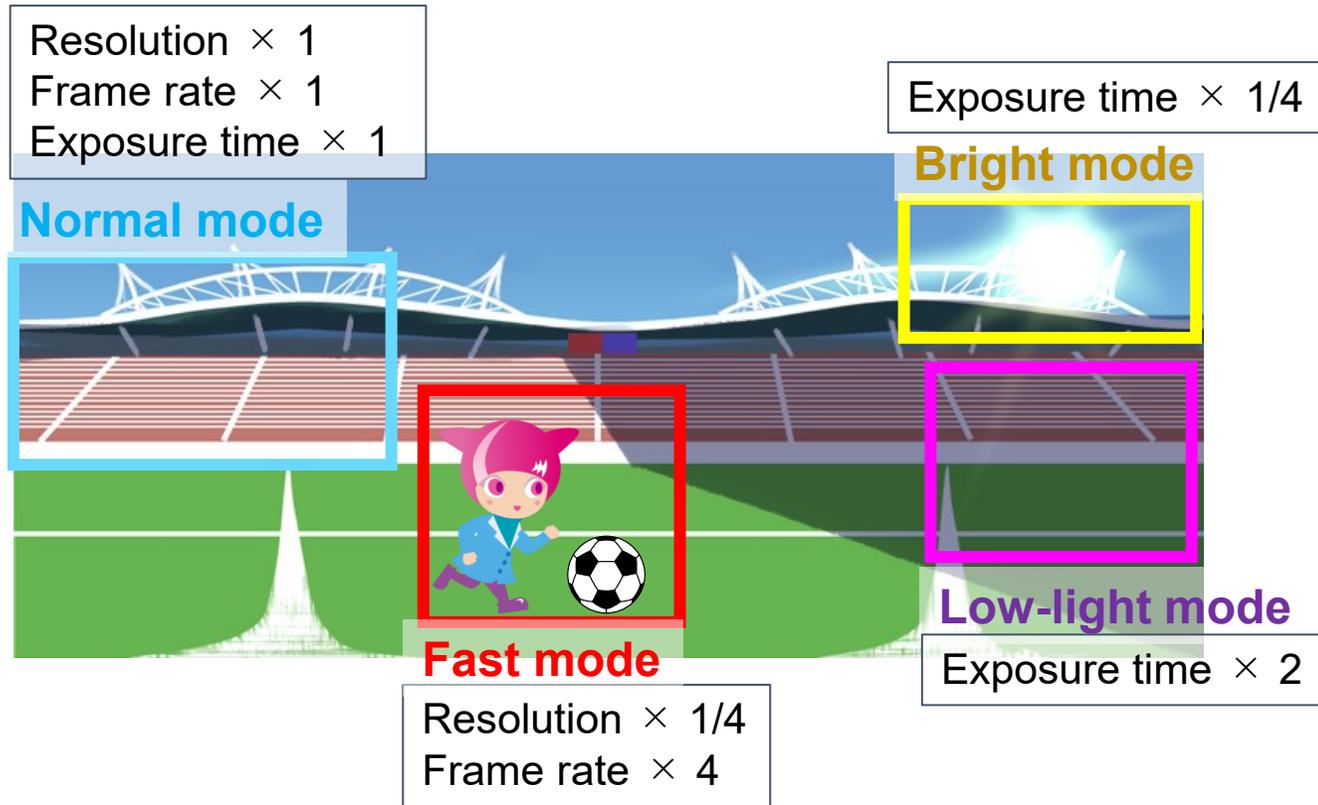Need for integrating high resolution, frame rate, and dynamic range
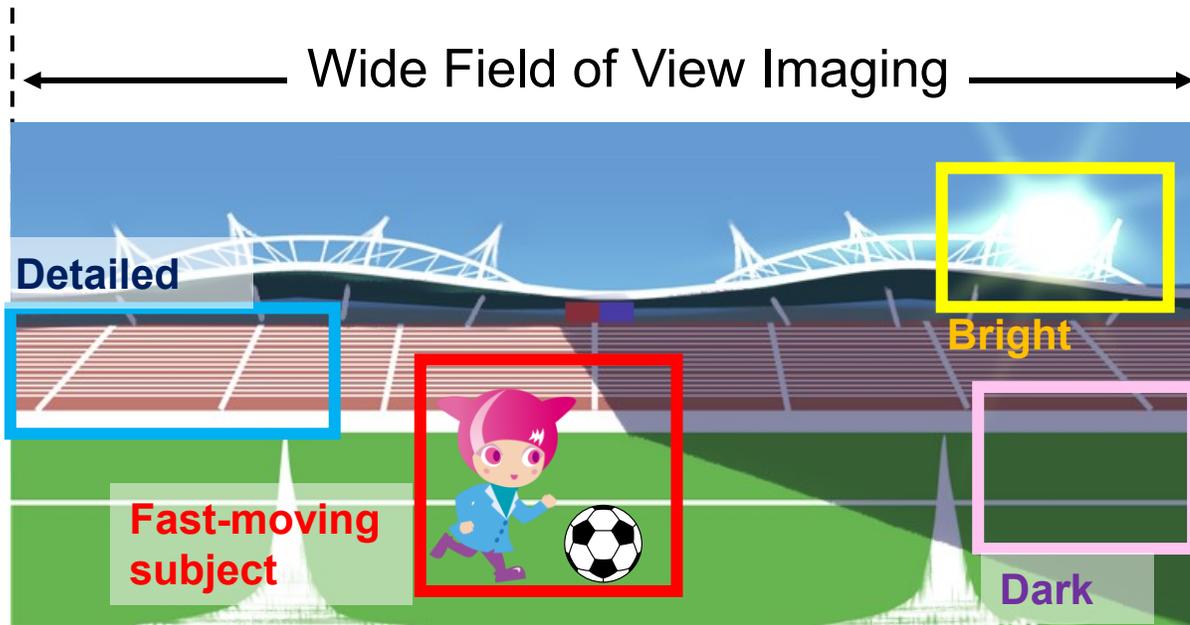
Coexistence of diverse movements and brightness levels in the same frame

Trade-offs of imaging parameters limit the performance of image sensors

Scene-adaptive imaging technology

Image quality improvement through subject-based area control of imaging parameters

Resolution × 1
Frame rate × 1
Exposure time × 1

Normal mode

Bright mode

Exposure time × 1/4

Low-light mode

Exposure time × 2

Fast mode

Resolution × 1/4
Frame rate × 4

Controls the imaging parameters locally, area-by-area

Dynamic range

Required performance
(pseudo-achievement)

Frame rate

Limitations of sensor technology

Resolution

Pseudo-improvement of image quality with data rate suppression

Key Features of Our CIS

- Imaging mode is assigned to each 4×4 pixel block based on feedback signals.
- Exposure time, frame rate, and resolution are controllable per block.

| SLVS Driver |
| Logic Block |
| ADC Array |
| PGA Array |
| Mode Controller |
| VOB 16(V) |
| Effective Area 3904(H) × 2224(V) pixel (976(H) × 556(V) block) |
| VOB 16(V) |
| Mode Controller |
| PGA Array |
| ADC Array |
| Logic Block |
| SLVS Driver |

Feedback Signal

13.5 MHz SPI × 38 ch

Pixel Driver

HOB 128(H)

HOB 128(H)

4 × 4 pixel block

Mode Controller

4 Lines

Readout Pulse

Control Signals

Readout Line

A   B

Pixel

C   D
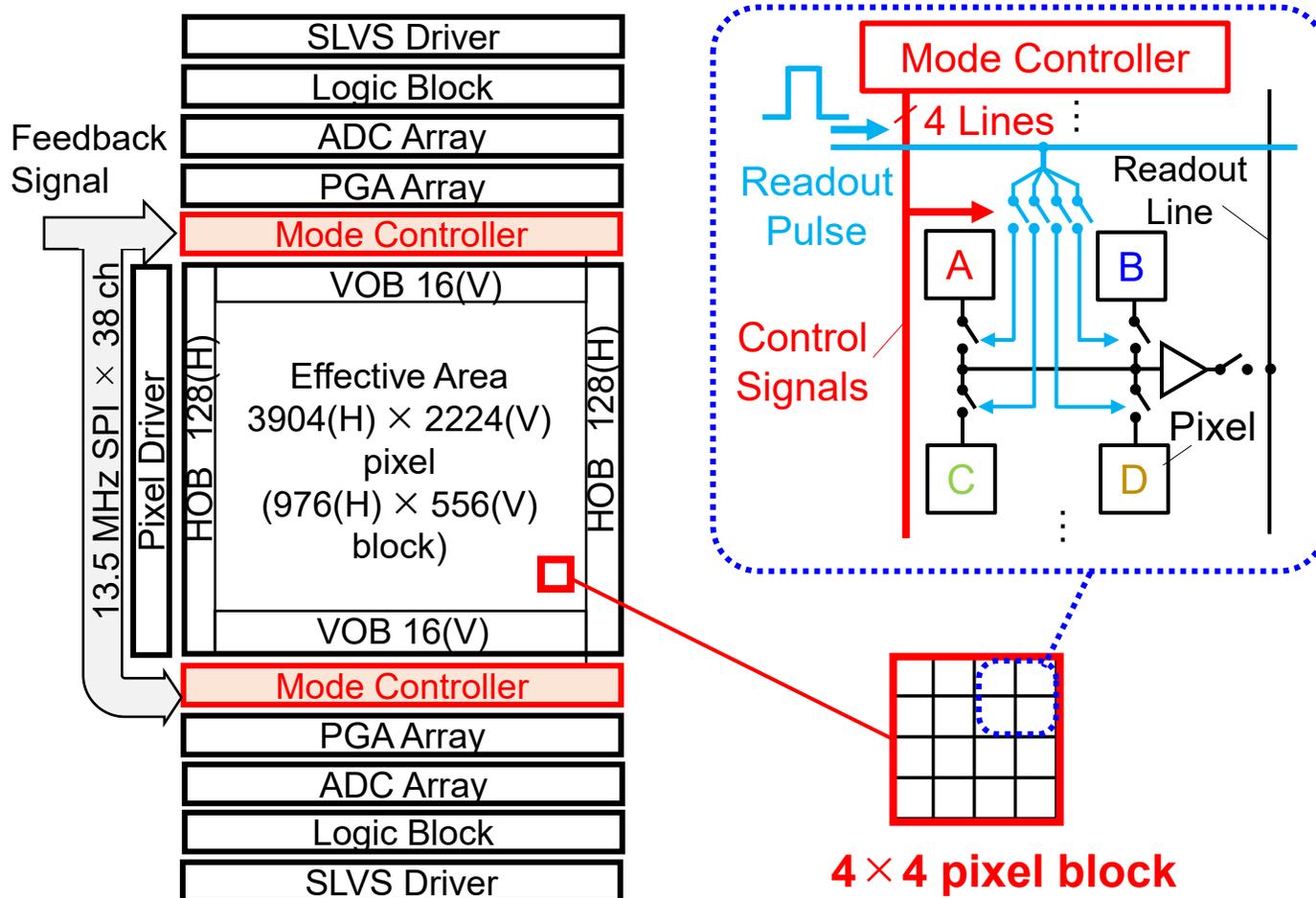
✓ Control the signal readout timing from each of the A, B, C, and D pixels.
✓ Select "readout for each pixel", "binning", "electronic shutter", and "skip readout".

Imaging Modes

| Mode	Pixel Number Per Block		Frame Rate (fps)	Exposure Time (s)
Normal		4×4	60	1/60
Bright		4×4	60	1/240
Low-Light		4×4	30	1/30
Fast		2×2	240	1/240

Pixel Readout Architecture

- PD(A)–PD(D) share a floating diffusion (FD) and a source follower (SF)

- Mode-dependent TXC(A–D) control exposure time and pixel binning

  - ✓ **Only one TXC(A–D) ON:**
    Selective charge transfer
    PD(A) → PD(B) → PD(C) → PD(D)
    are read out sequentially every 1/240 s.

  - ✓ **All TXC ON:**
    Pixel binning via charge summation
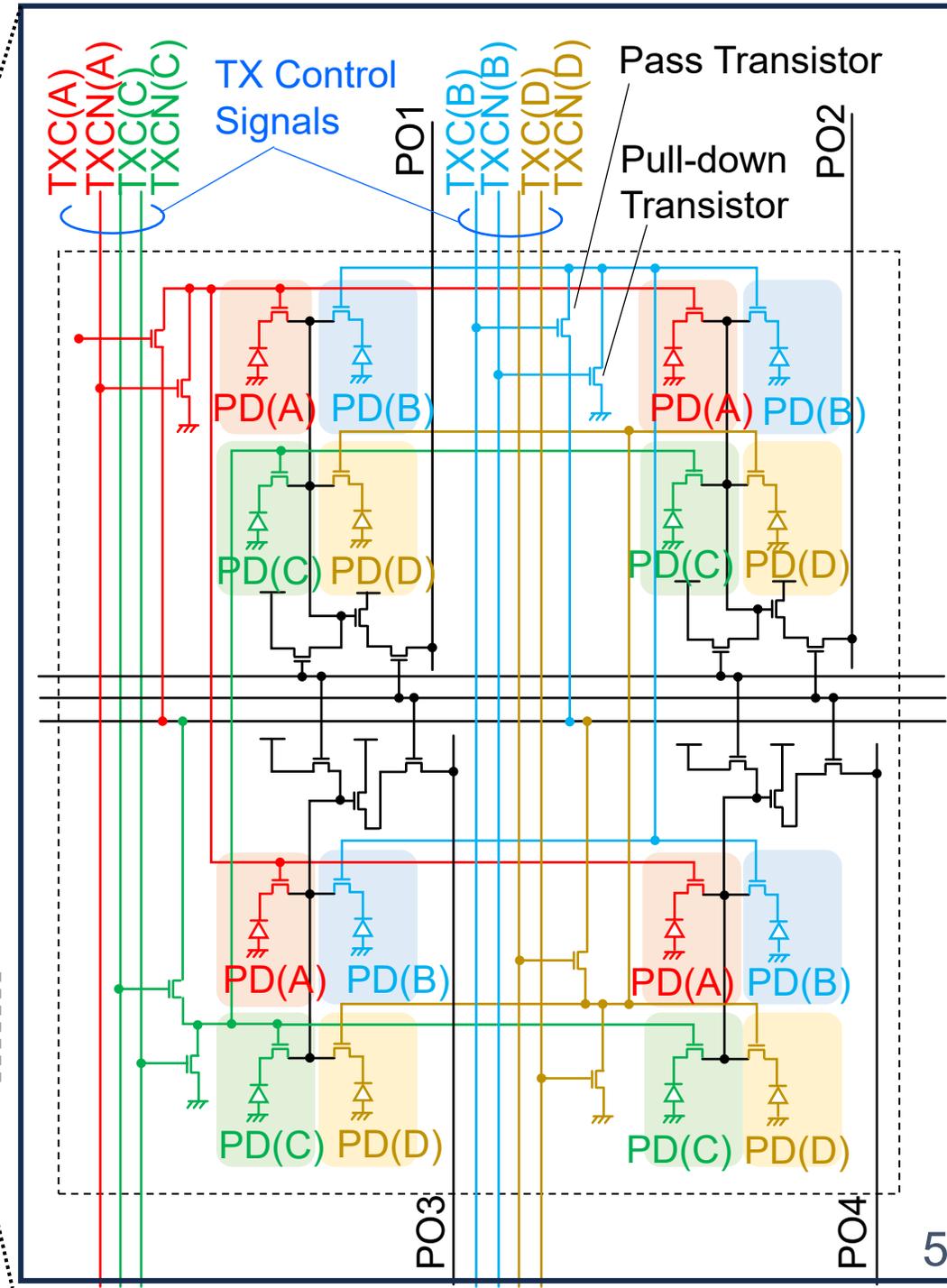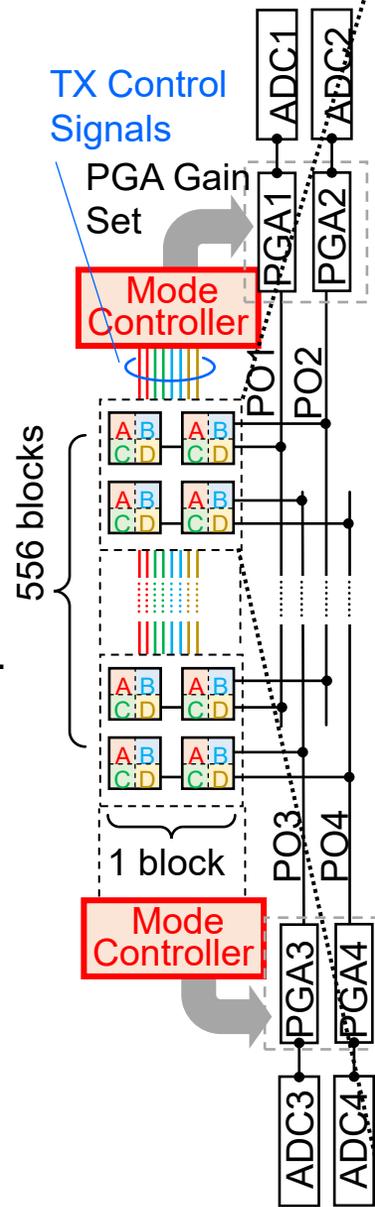
Imaging Mode Assignment Method

- Imaging mode is controlled by mode-dependent TXC(A–D) .
- All pixel-block rows are scanned by the pixel driver every 1/240 second.
- SPI feedback signals update TXC patterns, synchronized with pixel-block row selection.
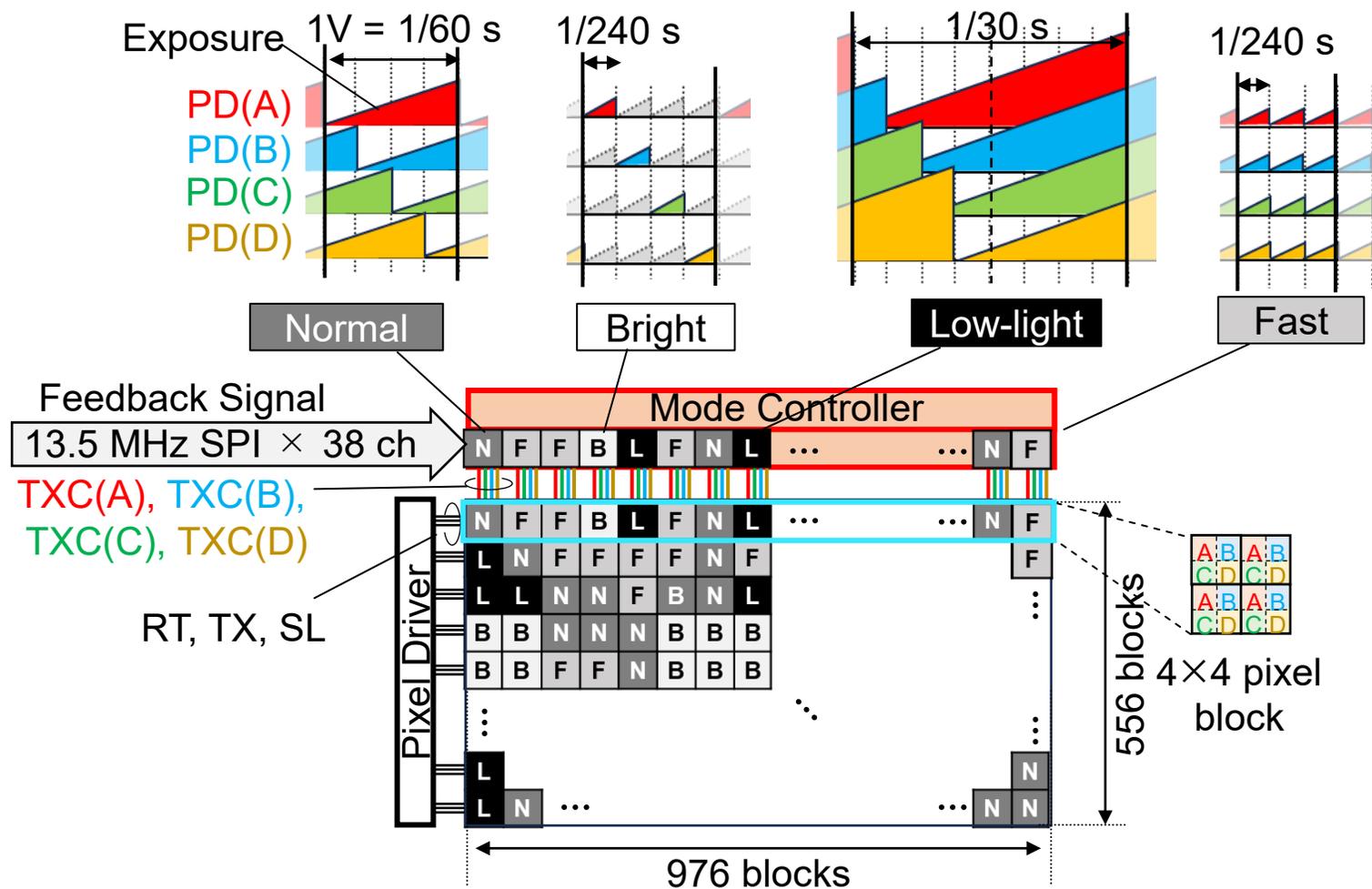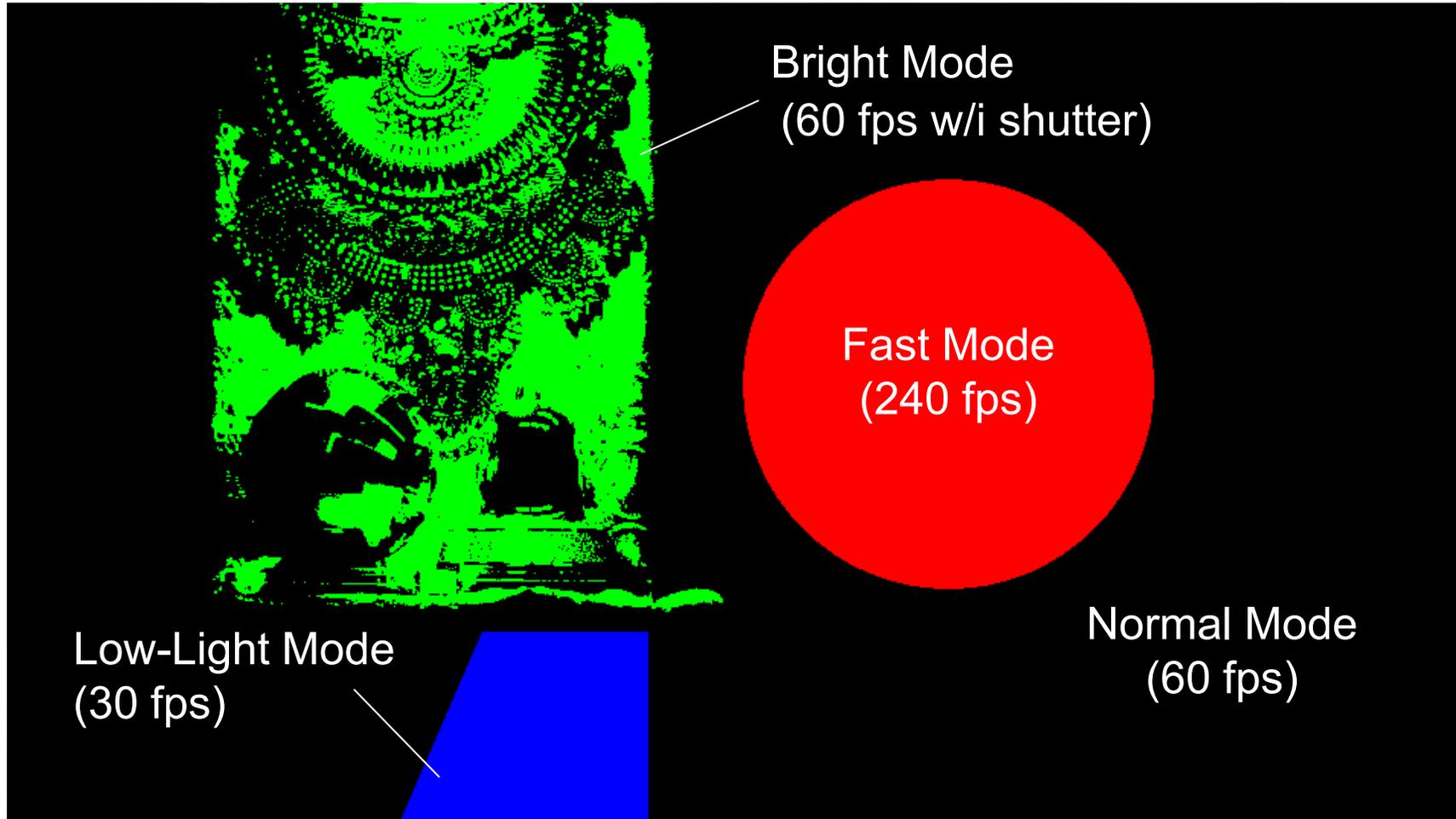
Local adaptation for each 4 × 4 pixel block

Acquired image

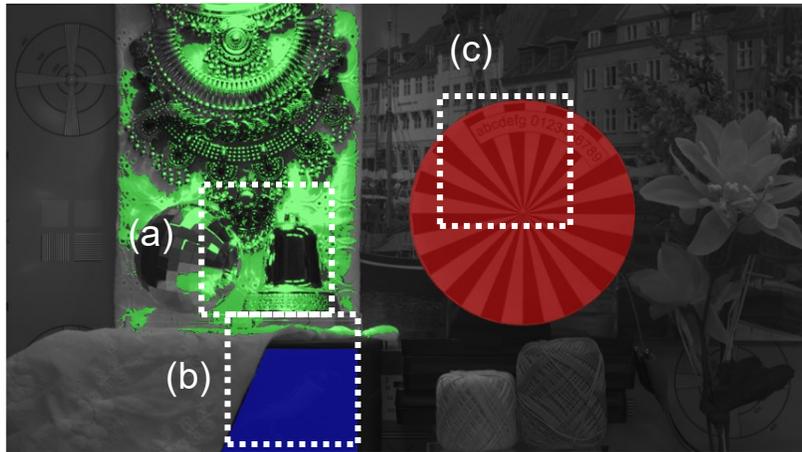3840(H) × 2160(V)

Local adaptation for each 4 × 4 pixel block

Mode Setting

Bright Mode
(60 fps w/i shutter)
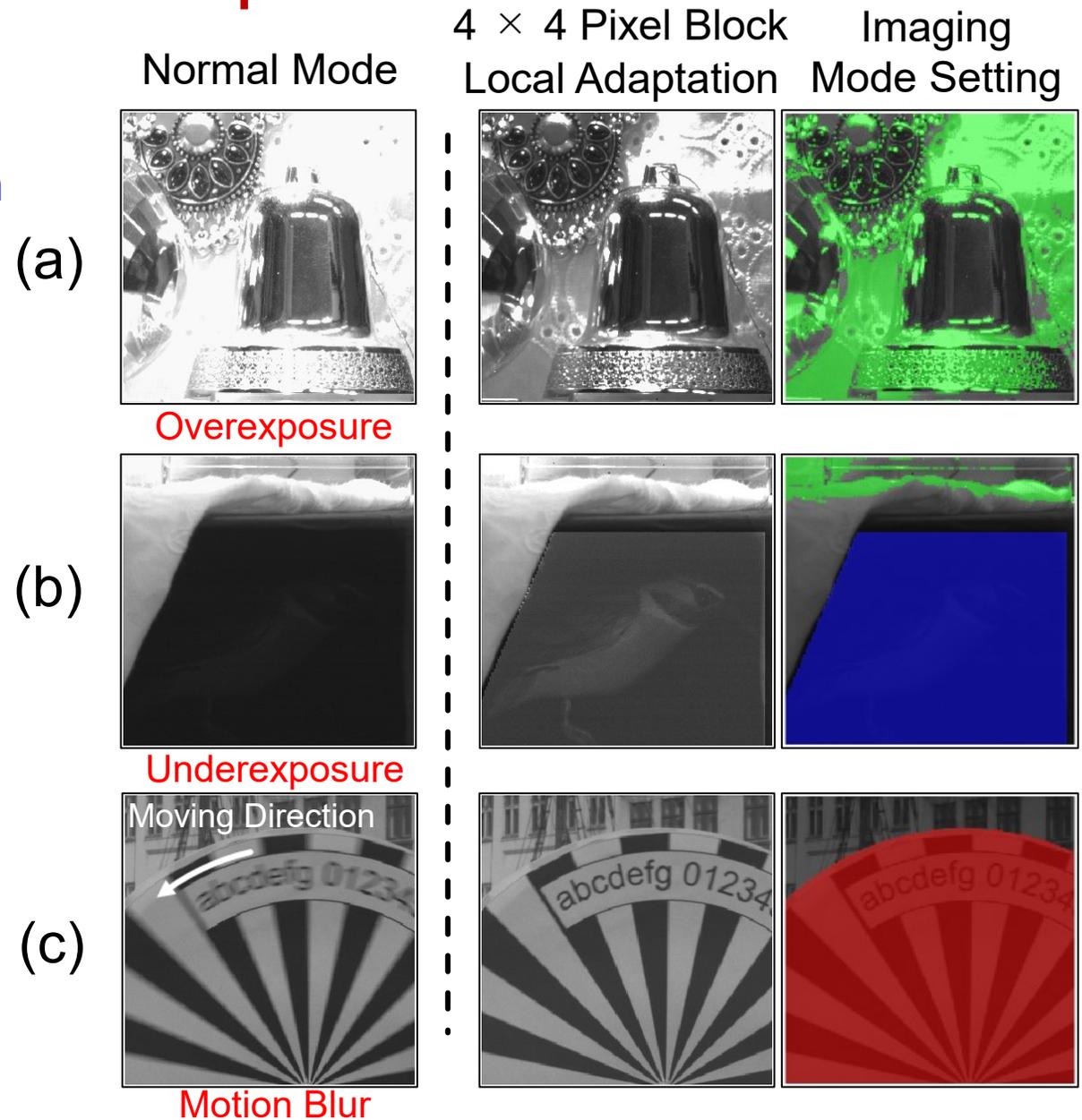
Fast Mode
(240 fps)

Low-Light Mode
(30 fps)

Normal Mode
(60 fps)

976 (H) × 556 (V) Blocks

Local adaptation for each 4 × 4 pixel block

✓ Subjective image quality is improved through local adaptation of imaging parameters.

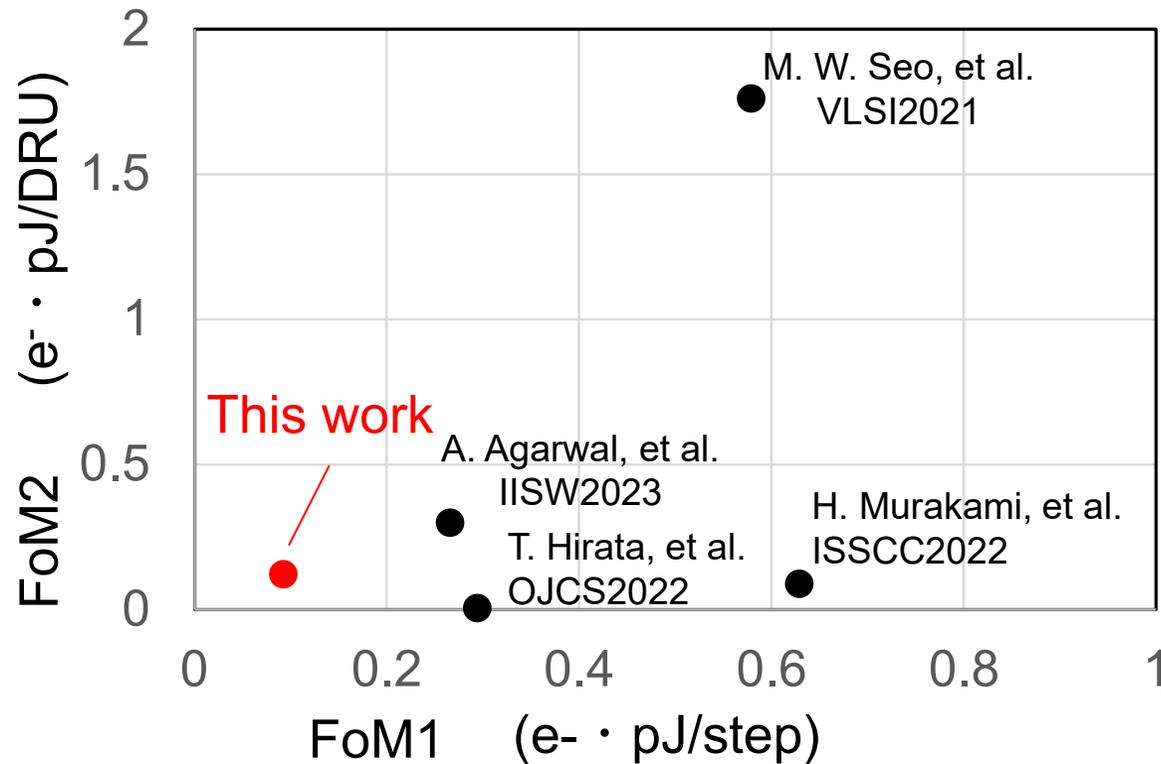- ⬛ Normal
- 🟩 Bright
- 🟦 Low-Light
- 🟥 Fast

Normal Mode | 4 × 4 Pixel Block Local Adaptation | Imaging Mode Setting

(a) Overexposure

(b) Underexposure

(c) Moving Direction — Motion Blur

FoM comparison with recent CIS

✓ Our CIS is superior and well-balanced in both FoMs due to the local adaptation of imaging parameters.
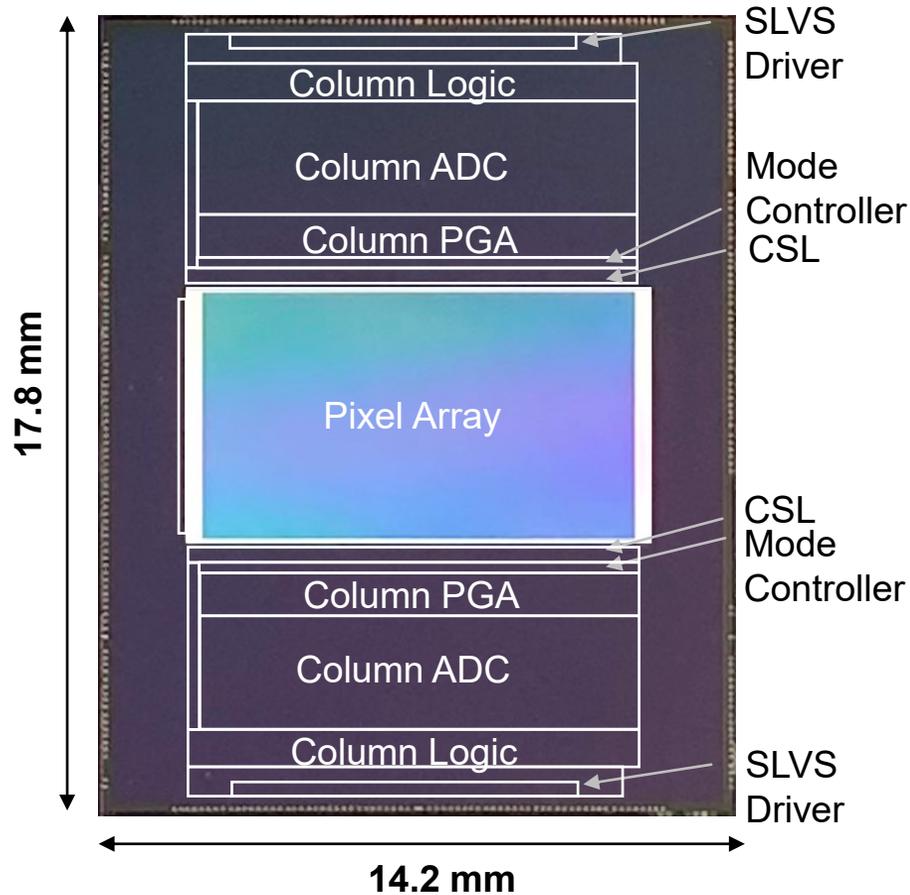

FoM Definition

$$FoM1 = \frac{Power \times Noise}{Number\ of\ Pixels \times Frame\ Rate \times 2^{ADC\ Bit\ Depth}}$$

$$FoM2 = \frac{Power \times Noise}{Number\ of\ Pixels \times DRU}$$

$$DRU = \frac{Saturation}{Number\ of\ Pixels \times DRU}$$

Conclusion

- An 8.7 Mpixel CMOS image sensor with local adaptation per 4×4 pixel block
- Resolution, frame rate, and exposure time are adjustable per block
- Achieves enhanced image quality while suppressing the data rate
- Demonstrated performance: 4K resolution, 240 fps, and expanded dynamic range

The proposed CIS balances resolution, frame rate, and dynamic range for high-quality wide field of view imaging.

CIS Specifications

Fabrication Process	BSI 90nm 1P6M	
Supply Voltage	3.3 V / 1.2 V	
Pixel Size	2.5 μm × 2.5 μm	
Pixel Number	3,904 (H) × 2,224 (V)	
Block Number	976 (H) × 556 (V), 4 × 4 pixels/block	488 (H) × 278 (V), 8 × 8 pixels/block
Frame Rate	240 fps (Fast mode) 60 fps (Normal mode) 30 fps (Low-light mode)	480fps (Fast mode) 120fps (Normal mode) 60fps (Low-light mode)
Feedback Signal Interface	13.5 MHz SPI, 38 data lanes, 1 clock lane	
A/D Conversion	14-bit Digital CDS with 6 Times Multiple-Sampling	12-bit Analog CDS
RMS Random Noise	2.4 e⁻rms (Gain = 2)	4.4 e⁻rms (Gain = 2)
Output Interface	48 data lanes, 4 clock lanes, 576 MHz/lane, SLVS	
Conversion Gain	68.2 μV/e⁻	
Full Well Capacity	7,750 e⁻	
Power Consumption	2,640 mW	
Die Size	14.2 mm (H) × 17.8 mm (V)	