A 640x480 Resolution 326,000fps Continuous-Mode Ultra-High Speed Global-Shutter CMOS BSI Imager with Exceptional Light Sensitivity

IISW, June 5th, 2025

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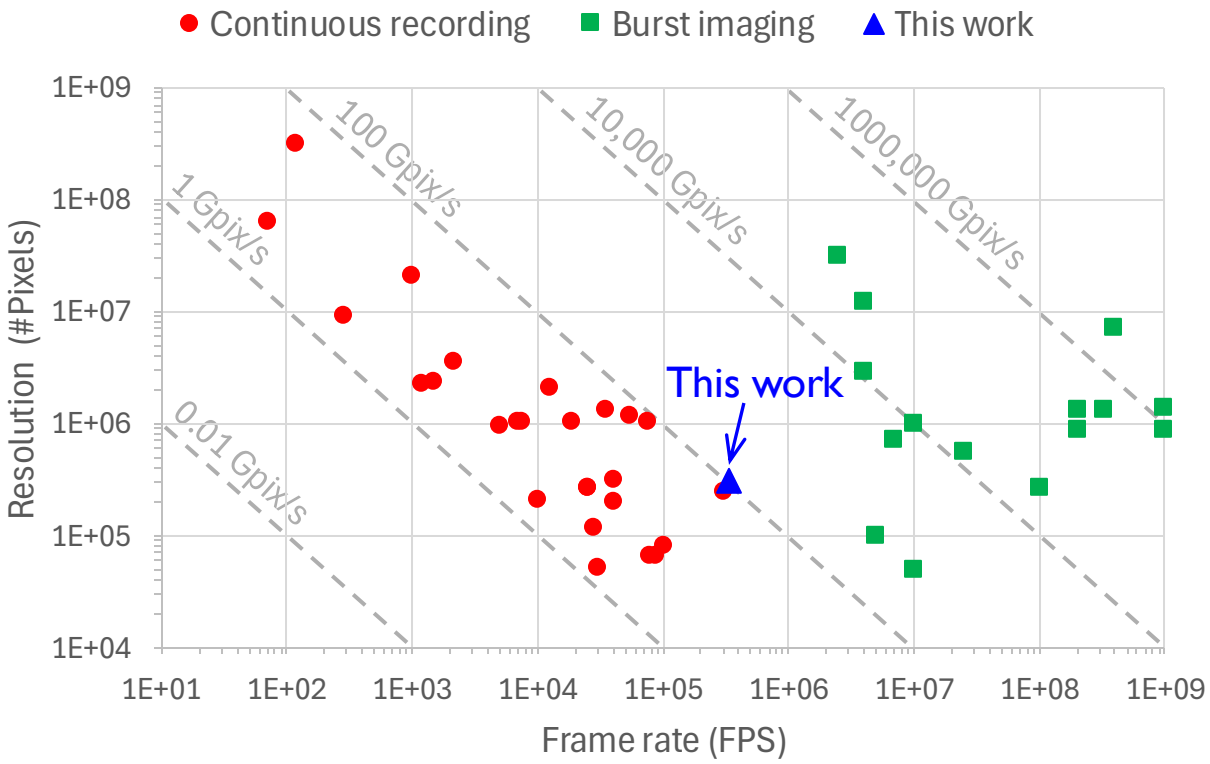
State-of-the-art in high-speed imaging ↔ Our sensor



Data from the last two decades

Our sensor

- CMOS monolithic imager
- Global shutter **BSI**
- VGA format
- Up to **326,000 fps continuous** recording at full ROI
- **59 ns** minimum integration time
- **100 Gpix/s** sensor throughput

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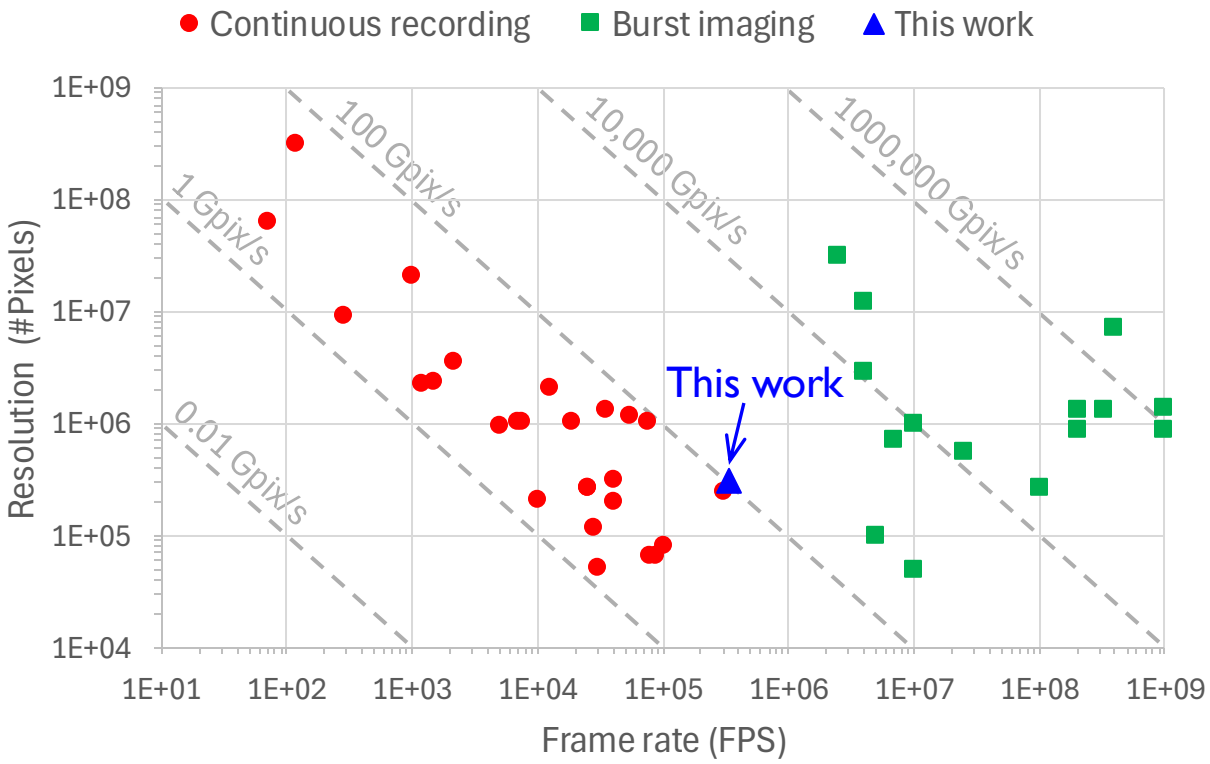


Data from the last two decades

BSI Technology

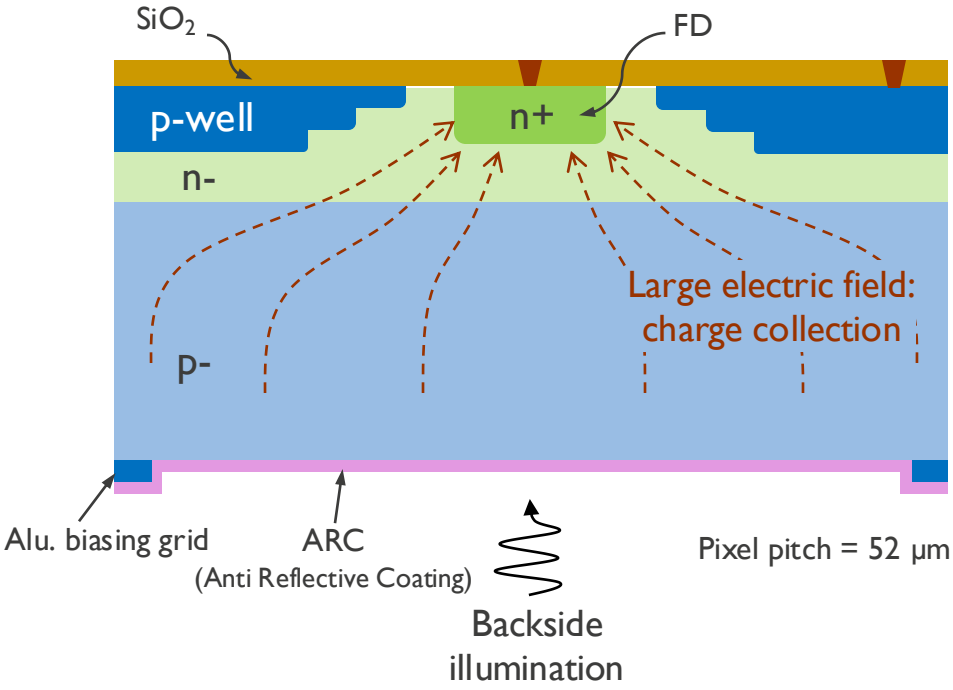
+

Ultra High-speed Pixel

+

Advanced Circuits

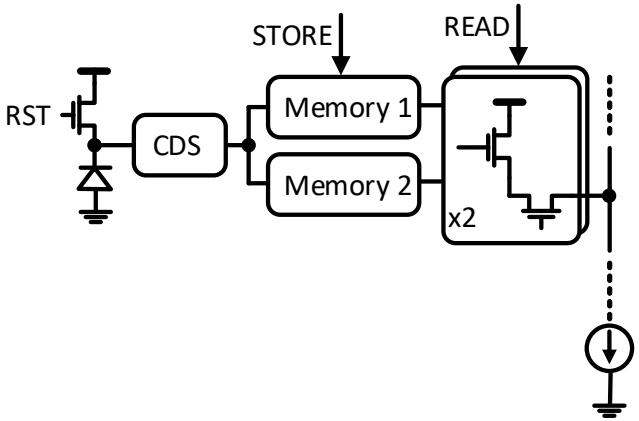
Ultra fast and sensitive pixel

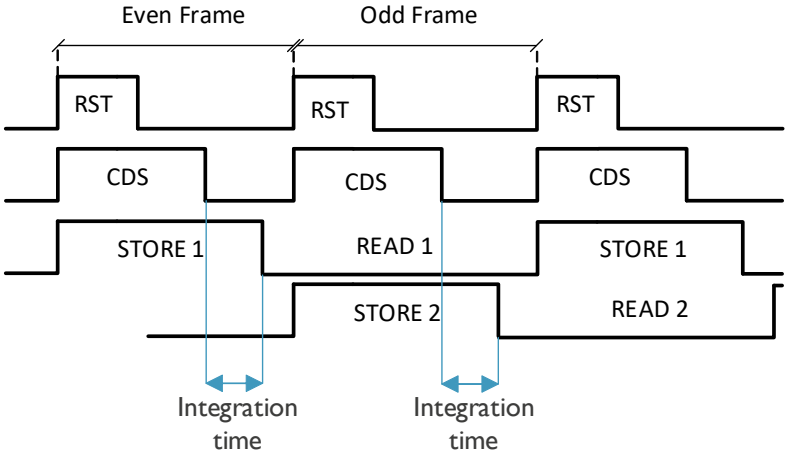


- Fully depleted substrate ⇒
  - Fast photocarrier transport ☺
  - Minimal lateral crosstalk ☺
- BSI with anti-reflective coating ⇒
  - High fill-factor and quantum efficiency ☺
- Enables **59ns** min. integration time

More details in IMEC poster P03
"Fully Depleted CIS Pixel Using Reverse Substrate Bias without Undesirable Leakage Currents"

Enabling high speed readout

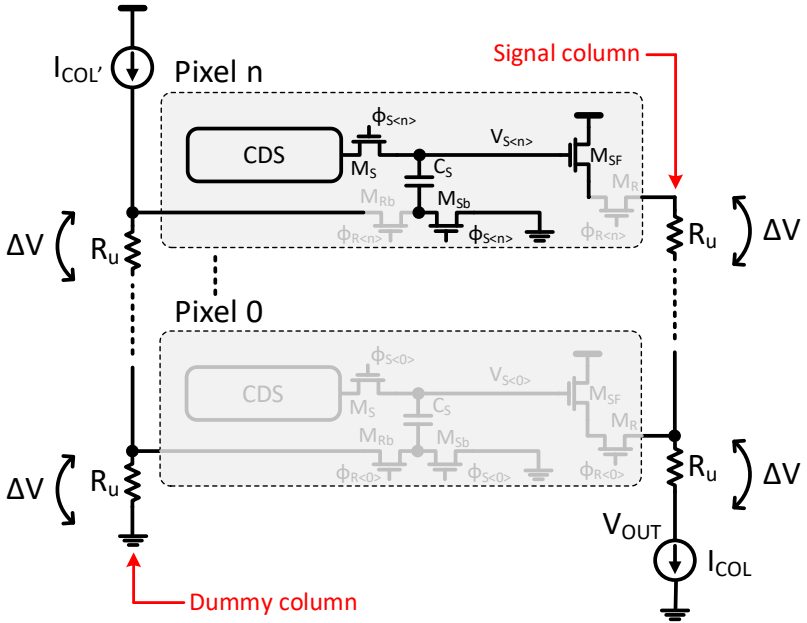




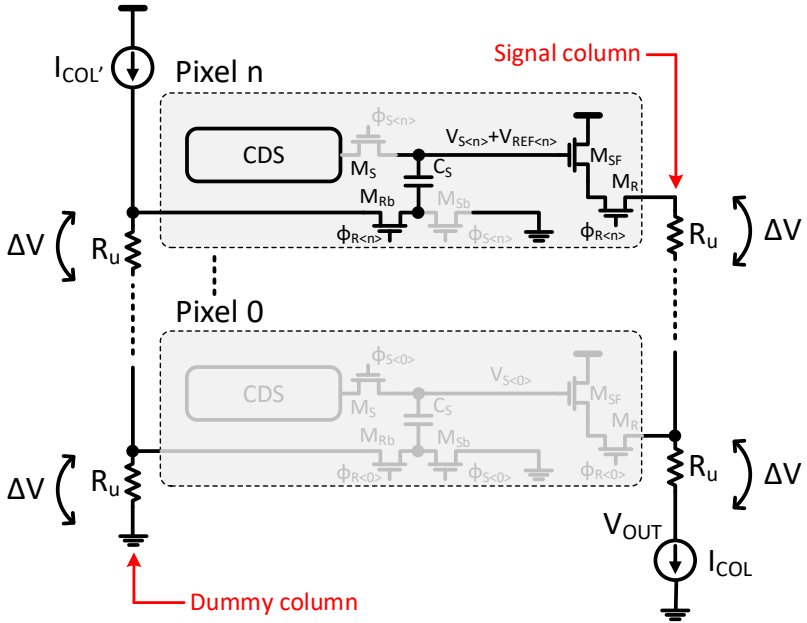
- In-pixel CDS
  - Analog CDS within single readout ⇒ **relaxed noise-speed tradeoff** ☺
- Dual in-pixel storage
  - Global shutter operation
  - Simultaneous integration and readout ⇒ **higher throughput** ☺

Optimizing dynamic range

Sample phase: $\phi_{S<n>} = 1$, $\phi_{R<n>} = 0$



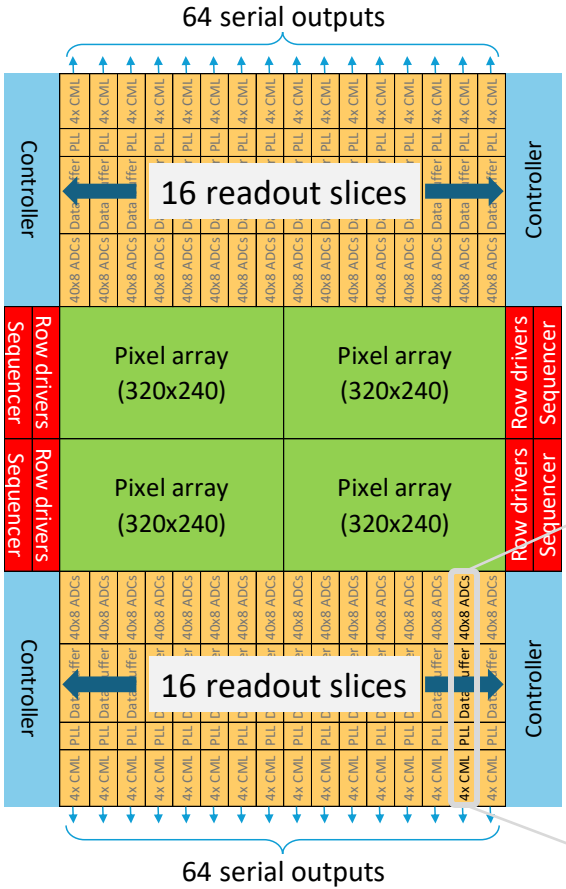
Read phase: $\phi_{S<n>} = 0$, $\phi_{R<n>} = 1$



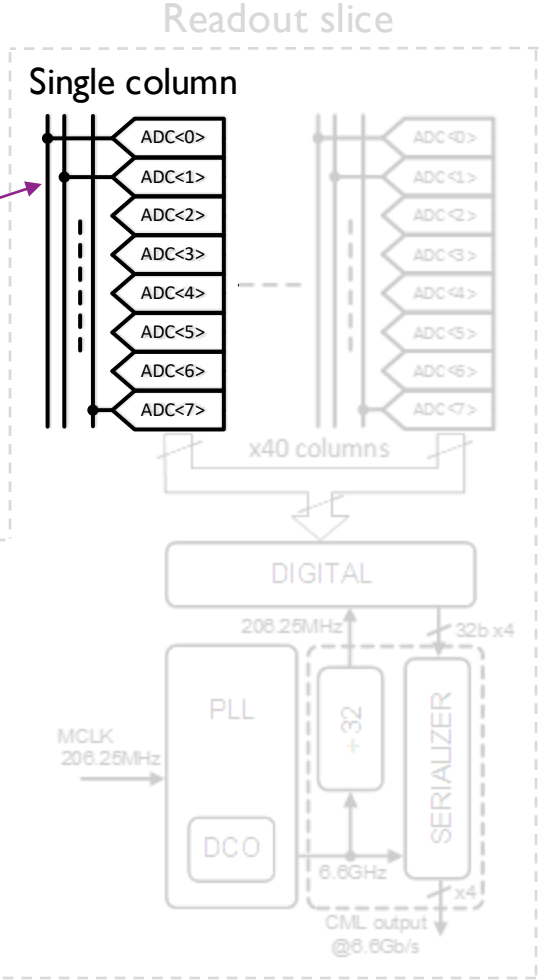
- Technique to remove FPN due to column IR drop
- Readout phase: switch the sampling capacitor bottom plate from **ground** to **dummy column**
- Dummy column line IR drop = signal column line IR drop

***Patent**: US10778926B2*

Sensor architecture

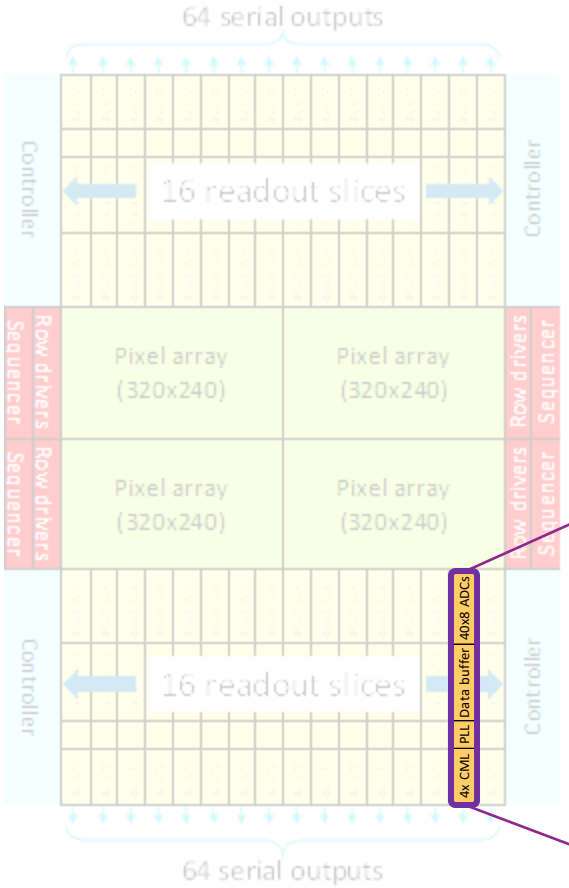


- Effective row time = **6.4 ns**
- Top and bottom readout + 8 ADCs per pixel column
  ⇒ **16x** row readout time relaxation
- Left and right row drivers
  ⇒ Global shutter accuracy for **59 ns** min. exposure time
- Die size = 5 cm x 4 cm



- 40x8, 9-bit, 15 MSps SAR ADC
- Digital = raw data compression + 64/66b Aurora protocol framing
- Integer digital PLL generating 6.6 GHz serializer clock
- 4 x 6.6 Gb/s CML outputs

Sensor architecture



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Readout slice

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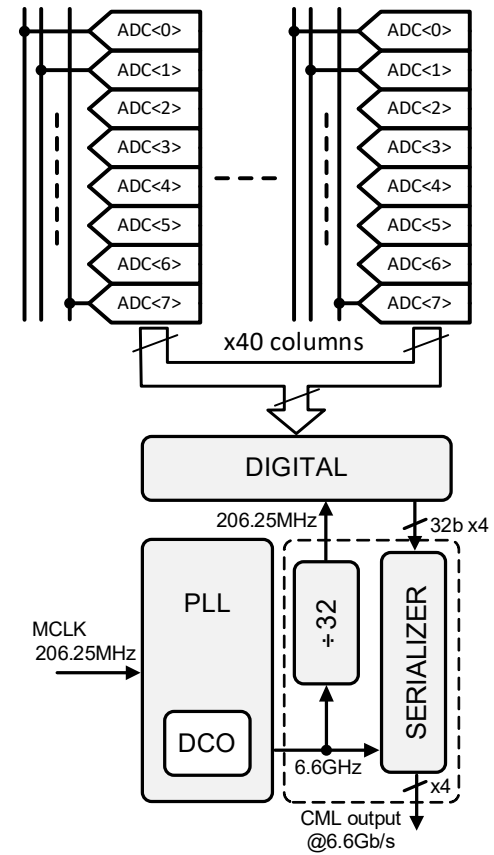
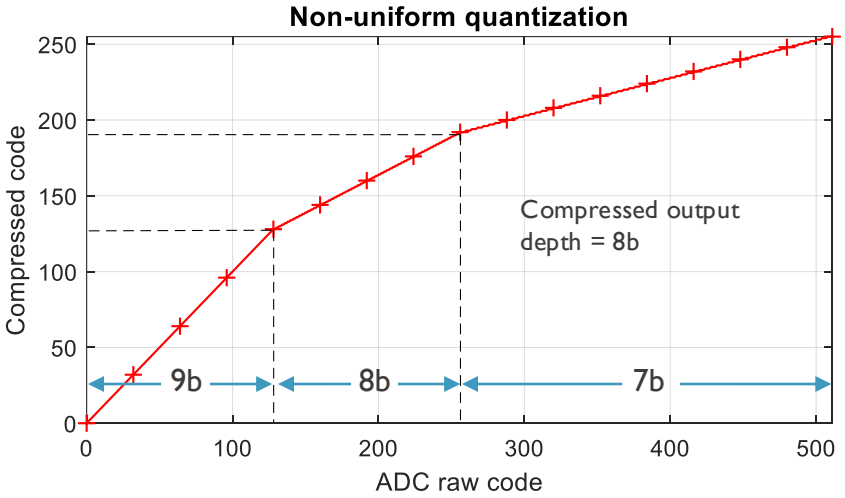
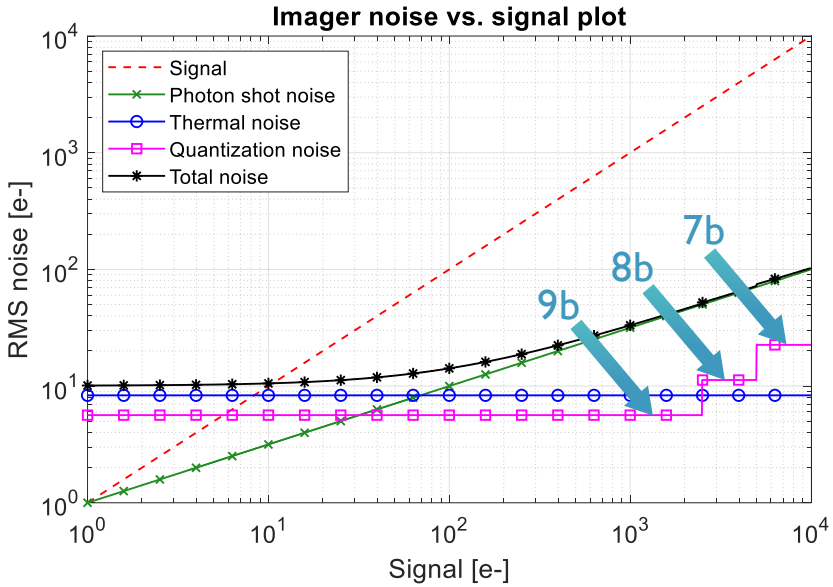


PTC inspired raw data compression





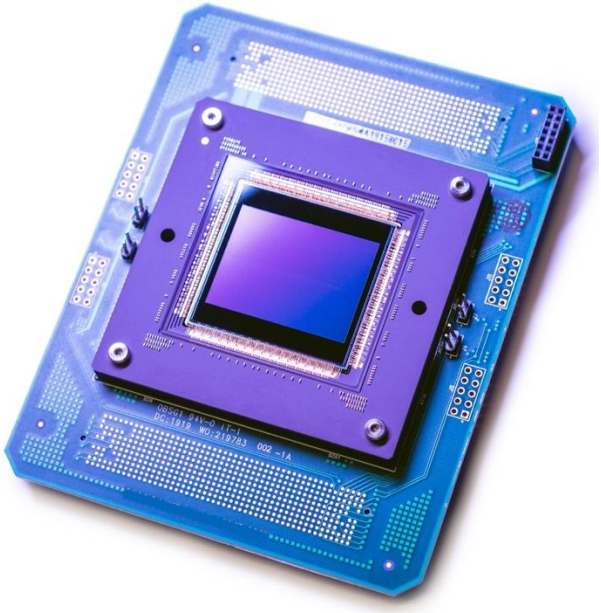
- Non-uniform 9/8/7b quantization
- 3 quantization noise levels
- Same data rate as 8b

PTC inspired raw data compression (example)

Original - 8b

Re-quantized – 8/7/6b

Packaged sensor in a product

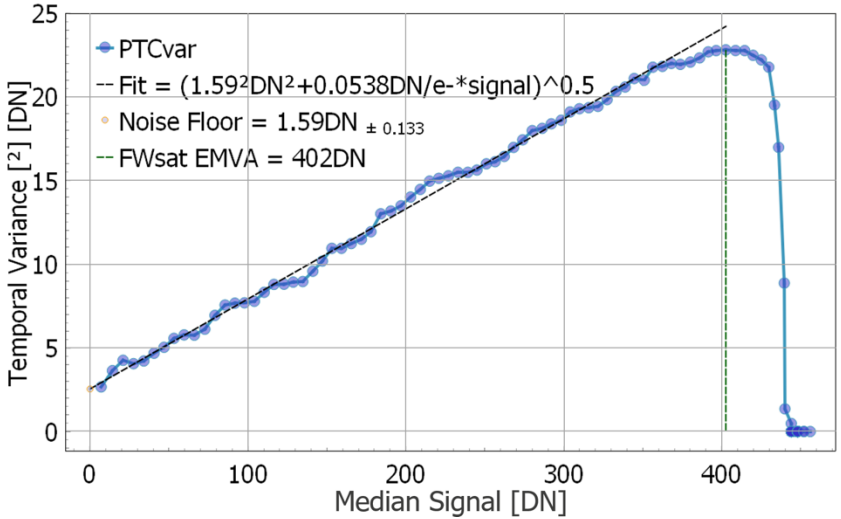


Packaged BSI sensor
PCB designed for camera
and lab testbench

Pharsighted E9•80S and E9•100S
https://photron.com/pharsighted/

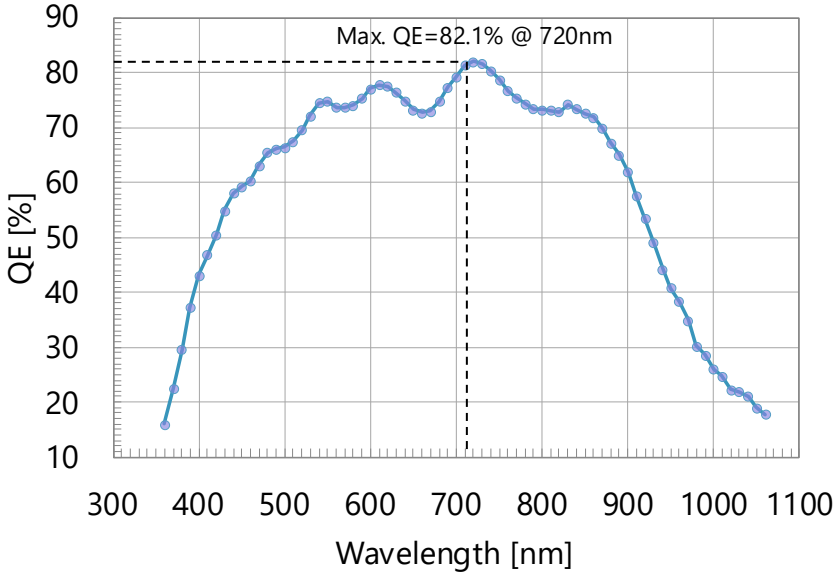
Measurement results

Photon Transfer Curve



- Sensor parameters extracted from the PTC:
  - Conversion gain = 0.054 DN/e-
  - Noise floor = 29.5 e- RMS
  - Full well capacity = 7.5 ke-

Quantum Efficiency plot



- Thanks to BSI, the sensor achieves high QE ☺

A super short event captured at 240,000 fps

- Frame size = 640 x 480
- Exposure time = 2 µs

Summary of key sensor specs

Parameter	Value
Technology	130 nm, 5 metal CMOS, **BSI**
Resolution	640 x 480 pixels
Pixel pitch	52 µm
Shutter type	**Global**
Full well capacity	7.5 ke-
Conversion gain	0.054 DN/e- (50 µV/e-)
Quantum efficiency @ 532 nm	**72.7%**
Max. FPS (max. ROI)	**326,000 fps**
Equivalent row time	**6.4 ns**
Readout noise	29.5 e- RMS (1.6 DN)

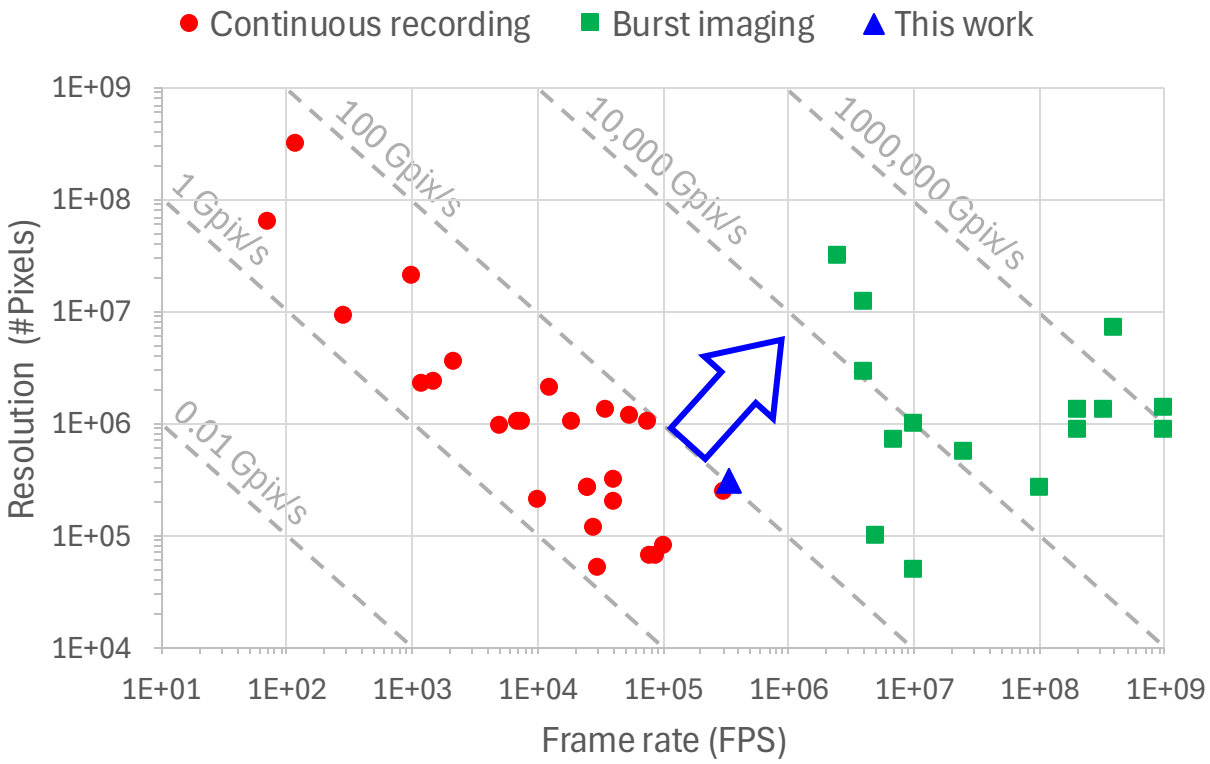
Parameter	Value
Absolute sensitivity threshold (EMVA 1288)	**0.011 e-/µm²**
Min. integration time	**59 ns**
Dynamic range	48 dB
Bit depth	9 bits
Output channels	**128 CML channels @ 6.6 Gbps**
Image lag	1 DN
Non-linearity	< 5%
Dark current @ room temperature	3.41 nA/cm²
Power consumption	25 W

Conclusion

- Continuous recording, UHS monolithic VGA imager delivering **326,000 fps**, enabled by,
  - Pixel technology for fast charge collection
  - In-pixel circuit techniques (CDS + dual capacitive storage)
  - Large parallelization of the readout circuitry (16 ADCs / column)
  - Very high data throughput (128 x 6.6 Gbps serial outputs)

- High **sensitivity**, thanks to,
  - Low input referred readout noise (29.5 e- RMS)
  - Fully depleted pixel substrate
  - BSI postprocessing

What's next



Data from the last two decades

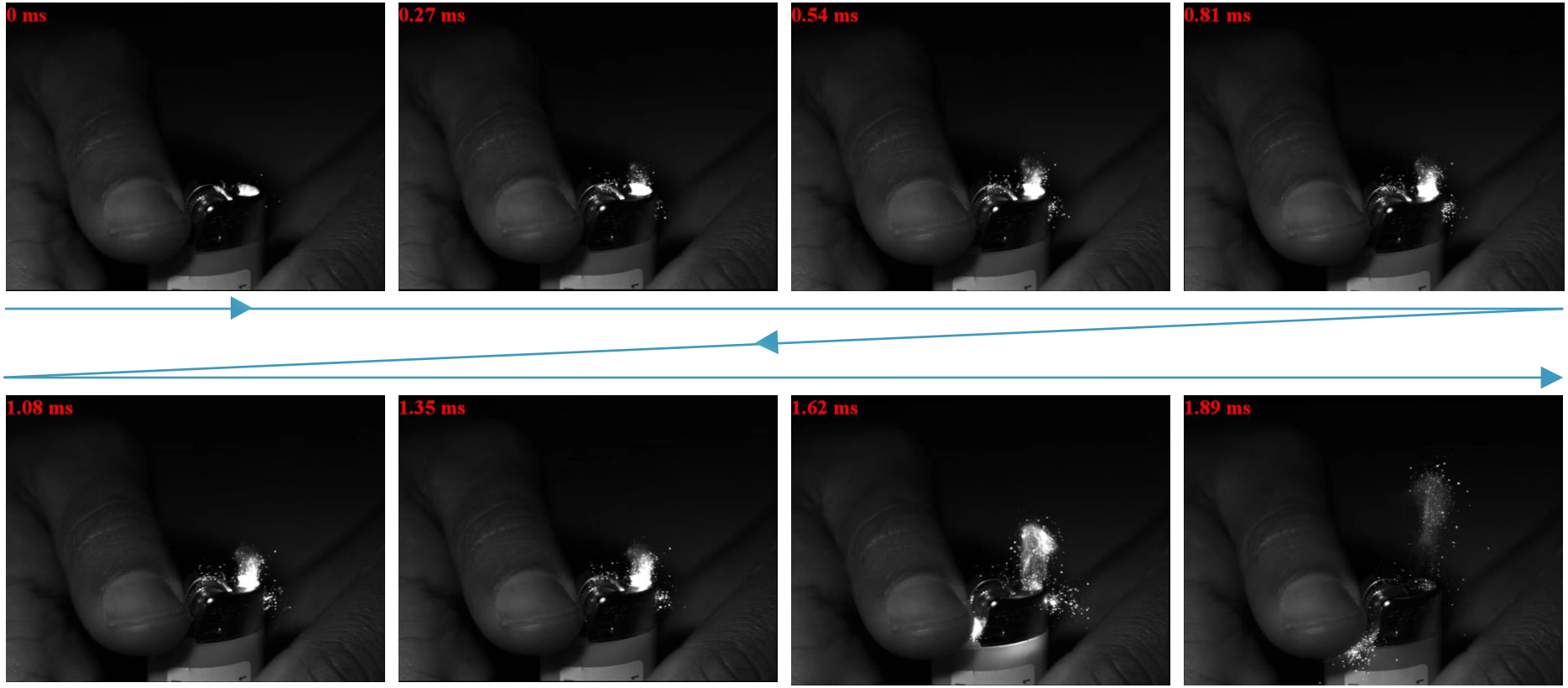
Further push the boundary of continuous high-speed imaging

Thank you!

Questions?

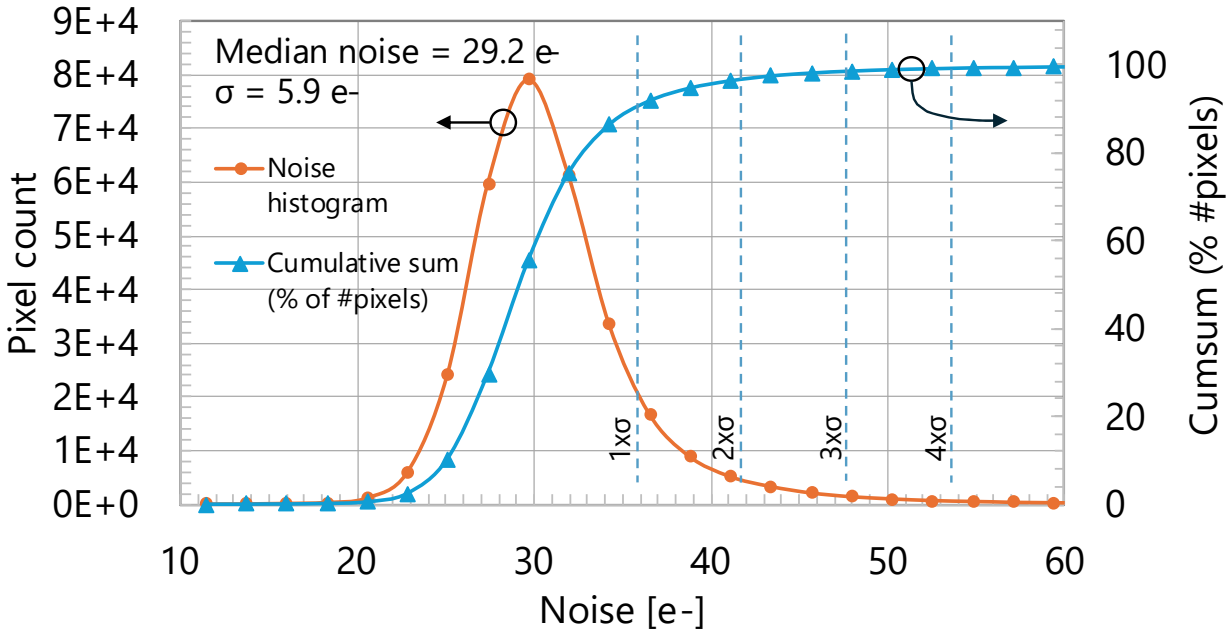
Extra slides

Non-successive 640x480 frames @ 240,000 fps



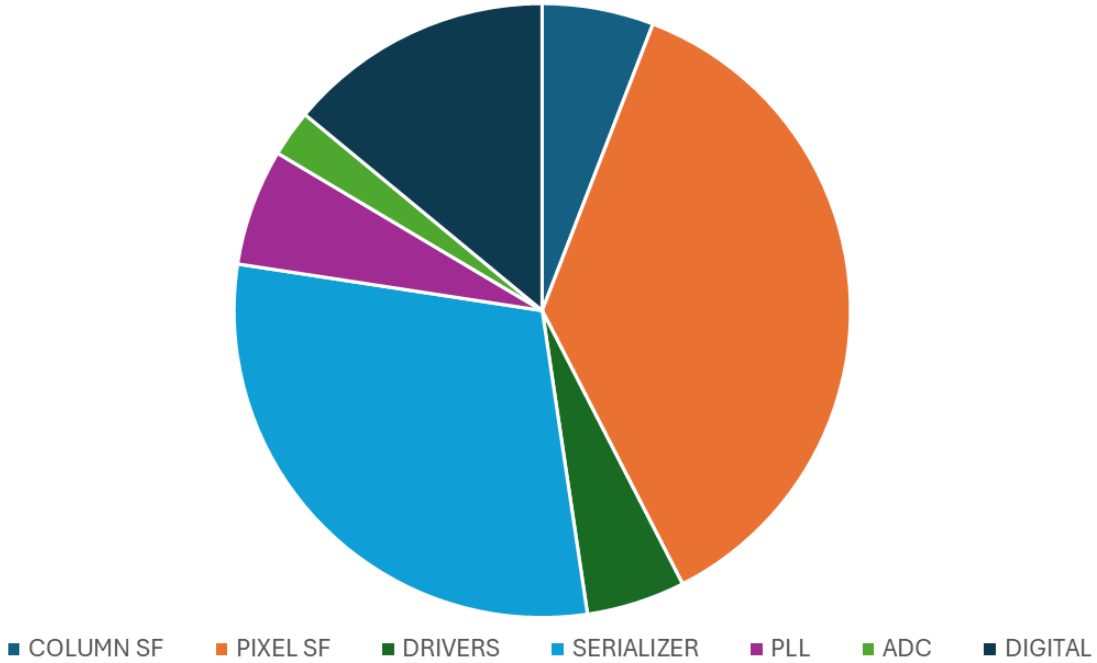
A selection of 8 frames out of the sequence of 600 frames

Readout noise histogram



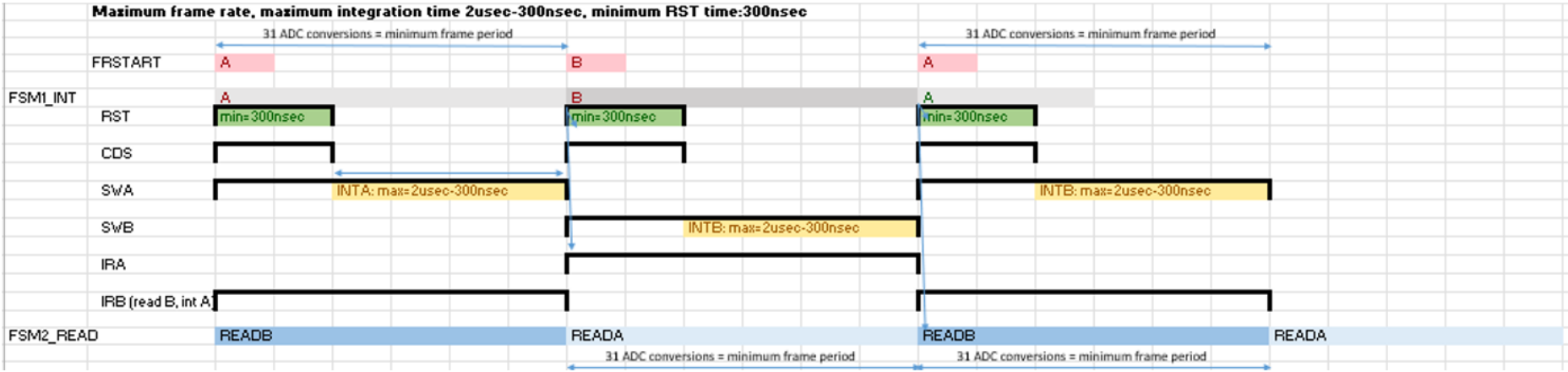
- Histogram of readout noise:
  - 99.2% of the pixels have noise within 4σ

Power consumption breakdown



SF = Source Follower

Pixel operation



- Min. reset time 300ns + Min. integration time 59ns determine the max. frame rate when ROI is less than 2*(359ns/63.03ns - 1) ~= 10 RBs (640x80 pixels)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