High-Frame Rate Low-Noise Global Shutter CMOS Image Sensor for High-Speed Machine Vision

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2025 International Image Sensor Workshop, Hyogo, Japan

Outline

- Motivation
- Sensor and Pixel Architecture
- Operating Modes and Configurability
- High-Speed Interface Design
- Summary of Measured Results
- Conclusion

High-Speed Machine Vision: Applications and Focus

Industrial Inspection

Car Crash Testing

Slow Motion Replays

- Key enabler: High frame rate, low noise, global shutter image sensor

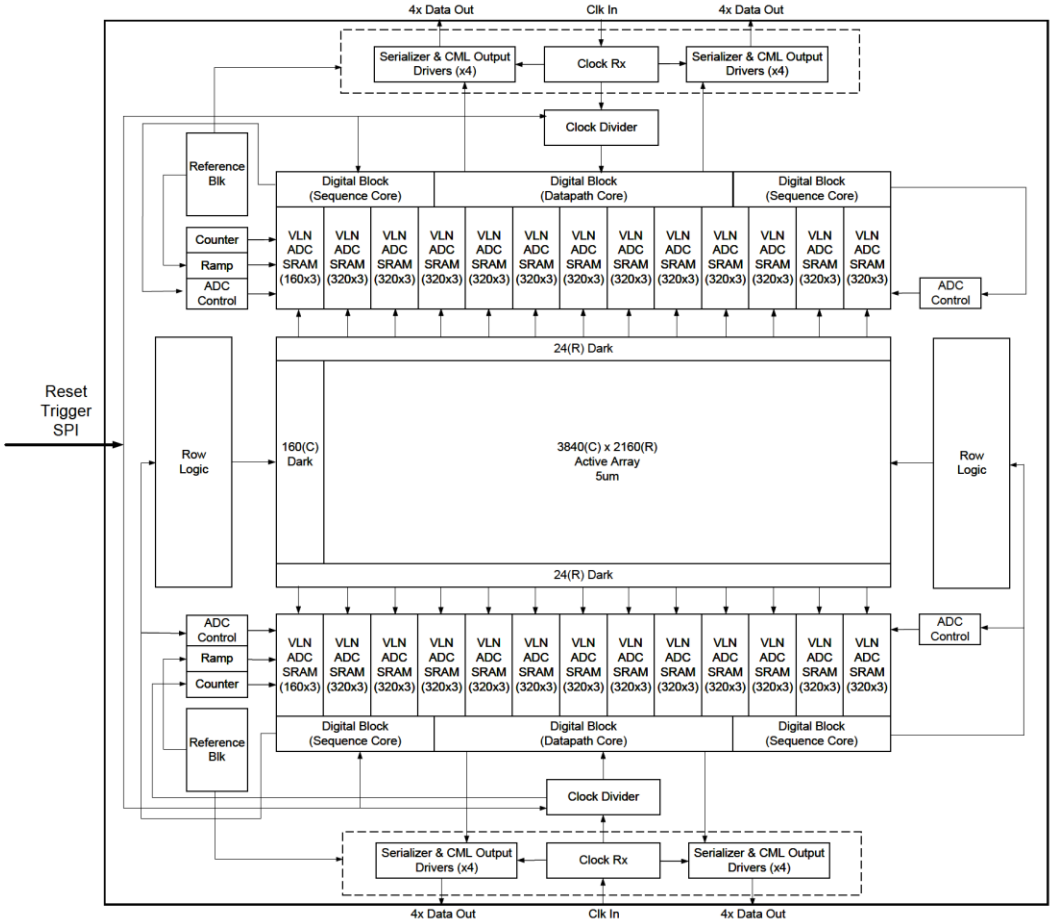
- Focus: Minimizing noise in global shutter image sensors at high-frame rates.
  - Maintain image quality at high frame rates (Minimize horizontal smearing, image lag etc.)
  - Support short integration times (~2us)
  - Increase SerDes bandwidth (reduced ports →lower power → reduced FPGAs → compact camera form factor)
  - Maximize sensor versatility (tradeoff between frame rate, resolution, noise, power)

High Level Target Specification

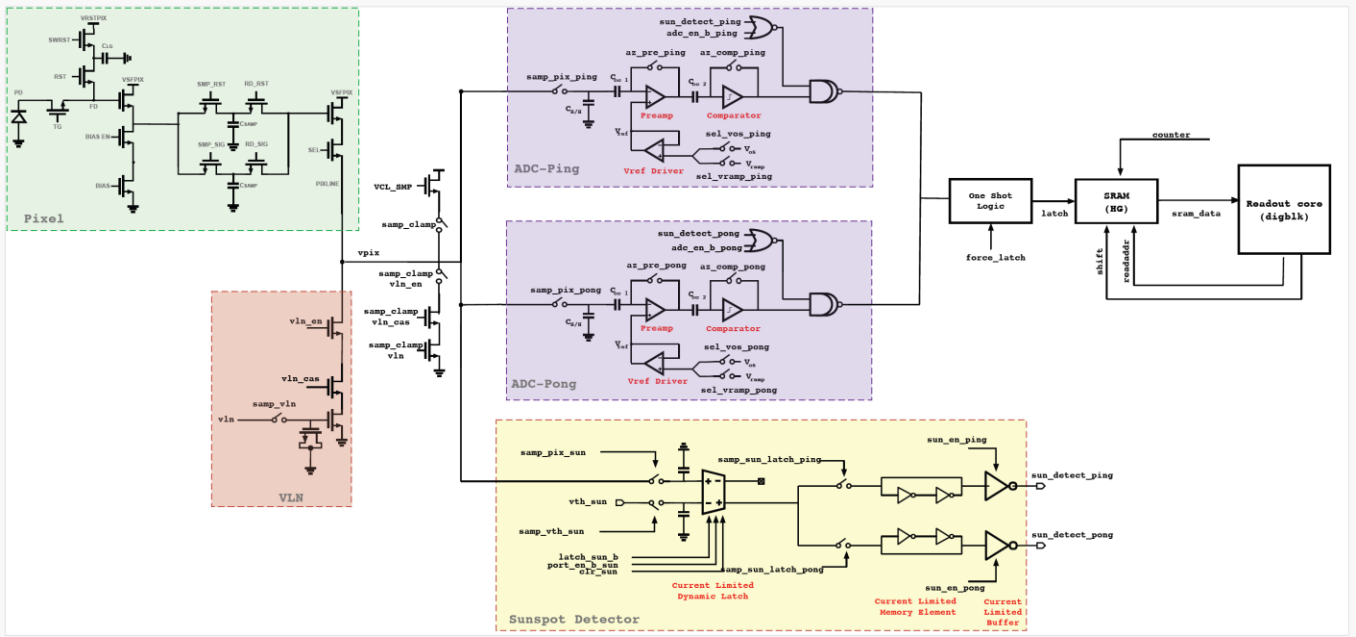
- UHD Resolution (3840 x 2160)
- Global Shutter (low PLS)
- Bit Resolution: 12/10/8b
- Frame Rate: >1000FPS@12-bits
- Total Output Ports: 16
- Temporal Noise <5e-
- Dynamic Range >66dB
- Monolithic BSI process implementation-cost sensitive market
- “Good” visual image quality- minimal artifacts (smearing, lag etc.)
- Maximum flexibility to trade-off noise, bit-depth, resolution for higher frame rate

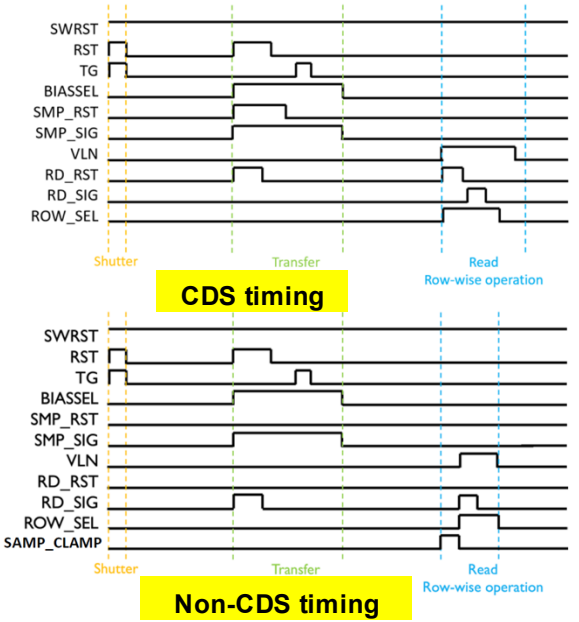
Sensor Architecture

- Top-bot readout architecture
  - 6 rows read concurrently (no pixel line cut)
- Ping-pong SS-ADC architecture to minimize row time.
  - Signal sampling and ADC conversion in parallel
- Total of 16 CML output ports @7.44Gbps
- Total of 12 superblocks per side
  - Each superblock reads 320 columns x 3 rows
- One high-speed differential input clock @ 3.72GHz as input per side



Readout Architecture and Operating Modes





- Sensors employs a 12T voltage domain global shutter pixel architecture.
- Two high-density deep trench capacitors to store reset and signal values.
  - Cap density ~26fF/μm^2
  - Capacitors optimally sized to minimize pixel kTC noise along with achieving QE & full-well targets.
- A common source follower readout to suppress FPN and reduce pixel output lines.

- Non-CDS mode allows to tradeoff noise for higher frame rates (reduced row time)
- In certain image resolutions where reset and signal sampling limits the frame rate

Additional Configurability

- Port concentration modes (Optimize power and system complexity based on application specific needs)
  - 16/12/8/6/4/2 ports

- Single sided readout (Power saving at lower frame rates)
  - Even numbered pixel lines connected to bottom readout chain
  - Odd numbered pixel lines are connected to top readout chain.
  - Dynamically programmable MUX inserted along even and odd pixel lines.
    - Dual-sided readout: VLN and ADC are on opposite sides
    - Single-sided readout: VLN and ADC are on the same side

- Programmable spatial sub-sampling modes (Increasing frame rate for lower spatial resolution)
  - Normal mode
  - Bayer skipping
  - Bayer sub-sampling

- Selectable output bit-depth (Increase frame rate for lower bit resolution)
  - 12b, 10b, 8b

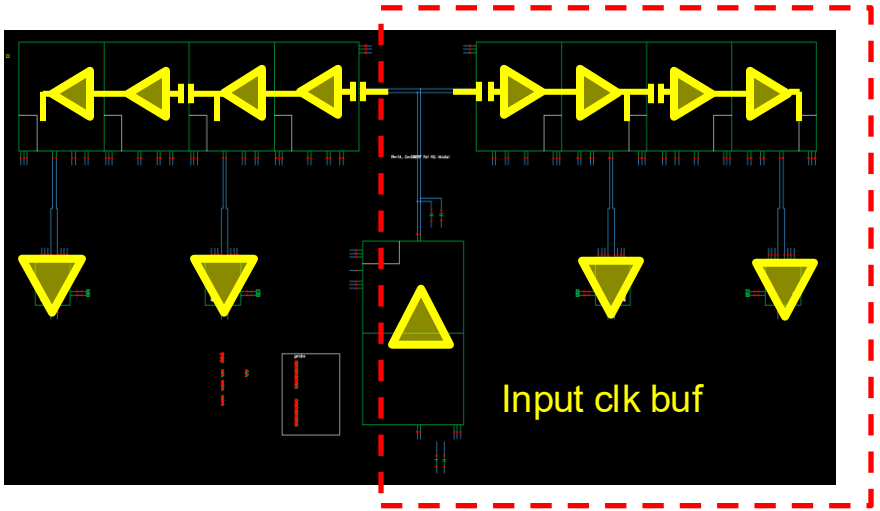
High-Speed Interface Design: Constraints and Challenges

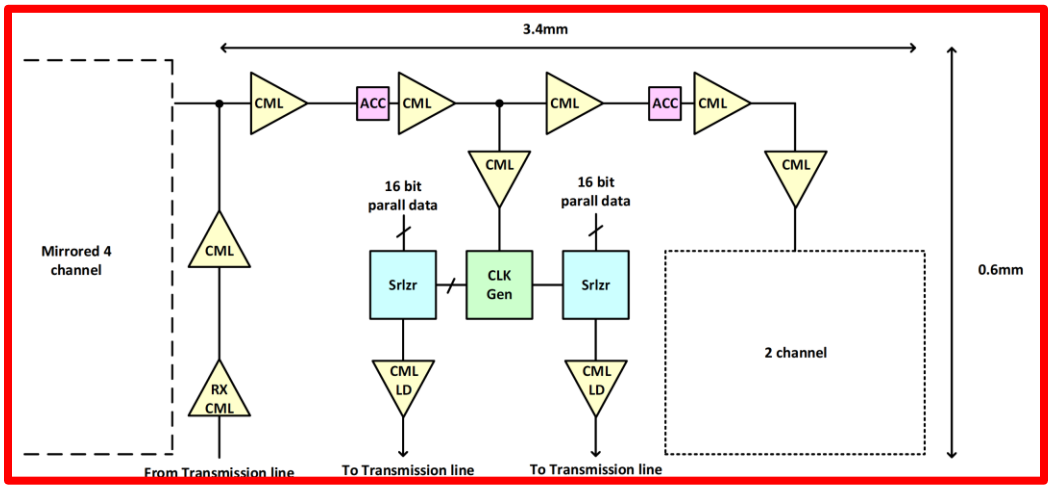
- Substantial amount of data generated at UHD resolution at high-frame rates.
  - ~100Gbps data rate to achieve 1000FPS at 12-bits at UHD resolution.
- Seamless integration with camera system imposes several constraints.
  - Compact camera form factor
  - Reduced number of FPGAs for data downlink and low power operation
- Number of high-speed CML output ports was restricted to 16
  - Focus to maximize the data bandwidth to support high frame rates.
  - Careful design, simulation and optimization is a must for high-speed signal chain.
- Only 4 metal layers available for routing in the selected 65nm process.
  - Precise impedance control.
  - Signal integrity optimization across high-speed paths.
- Key Blocks: Clock Rx, High-Speed Clock Distribution, Serializer and CML Driver

Clock Receiver and Distribution

- A differential clock at 3.72GHz is supplied externally and AC coupled to a on-chip clock receiver.

- Clock receiver is a CML buffer with multiple amplification stages.
  - Boosts a small-swing differential input clock to a sufficient level for clock distribution.
  - Placed at the center of a T-shaped clock tree.
  - Each branch spans 3.4mm





High-Speed Clock Distribution

- Total number of CML buffers and buffer to buffer spacing are carefully optimized by:
  - Theoretical analysis→ attenuation per unit length
  - Sign off through post-layout simulations (ensure clk fidelity at each CML buffer stage)

- Key challenges: random device mismatch and trace impedance variation
  - Impedance mismatch can cause common-mode imbalance → clock failure after several stages.

- Mitigation: Introduce periodic AC coupling in the clock distribution tree.
  - Helps restore common mode level
  - Filter low-frequency noise from earlier stages

- Issues with AC coupling (realized using MOS caps)
  - High-pass filter formed by AC caps and bias resistor (cutoff frequency designed for 1/4th of clock frequency)
  - Parasitic capacitance (proportional to AC cap size) causes increased signal attenuation.
  - Large bias resistors introduce thermal noise
  - This limits the number of AC coupling stages in the chain.
  - Careful sizing tradeoffs to balance signal integrity and noise performance

High-Speed Clock Distribution (contd..)

- Stable 50% duty-cycles are essential for robust DDR operation of serializer.

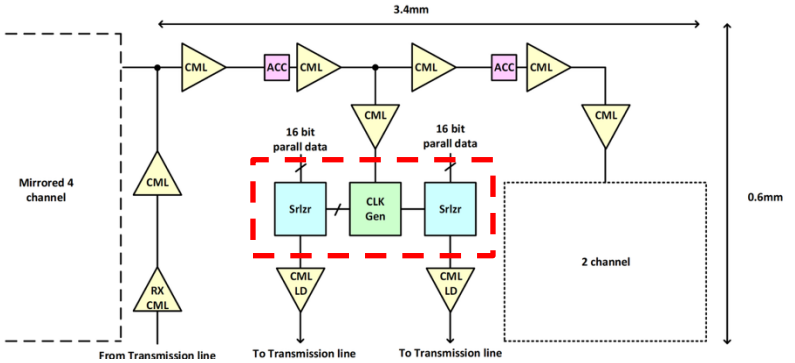
- Additional metal shielding beneath the high-speed signal traces.
  - Controlled impedance and reduction of undesired substrate coupling.
  - Extraction tools model substrate as zero-impedance ground → in reality layout geometry dependent distributed RC

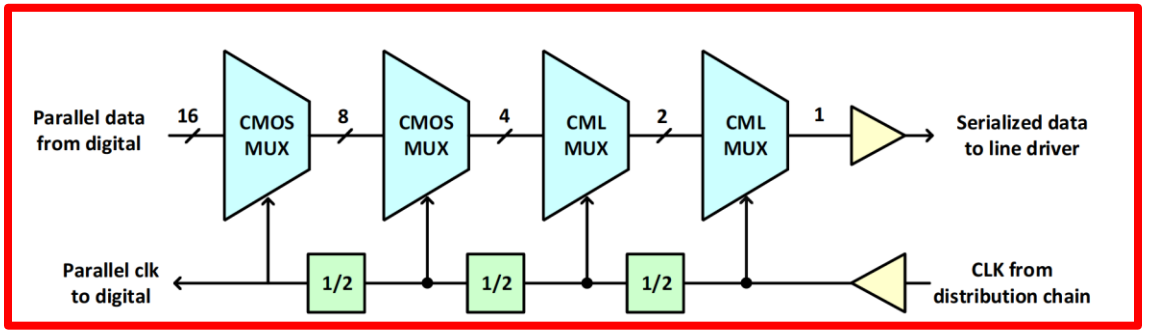
- Critical high-speed signal routing done in top-thick metal
  - To reduce trace resistance and capacitance

Serializer

- A common CML buffer from clock distribution feeds two serializers (16:1) placed symmetrically on the left and right sides.
  - High-speed clock domains employ CML-type dividers,
  - Lower-speed clock domains use CMOS TSPC-type dividers

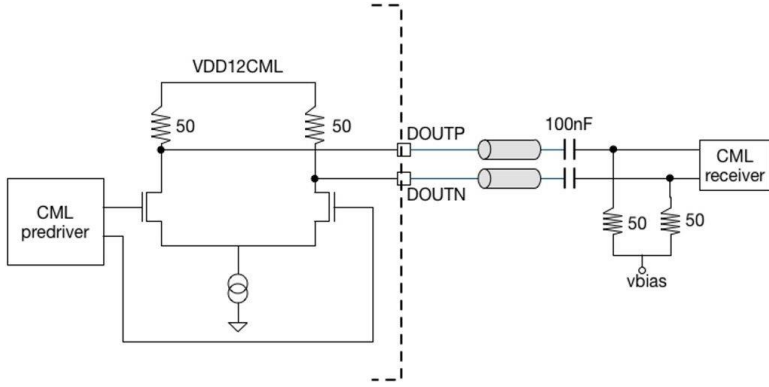
- Serializer is a multi-stage MUX tree optimized for performance and area efficiency.
  - CMOS Stages (Stage 1 and 2): TSPC logic for low-power and compact integration.
  - CML Stages (Stage 3 and 4): Uses CML MUXes with last stage with one clock delayed data path to support post-emphasis in the output driver for improved signal integrity at high data rates.



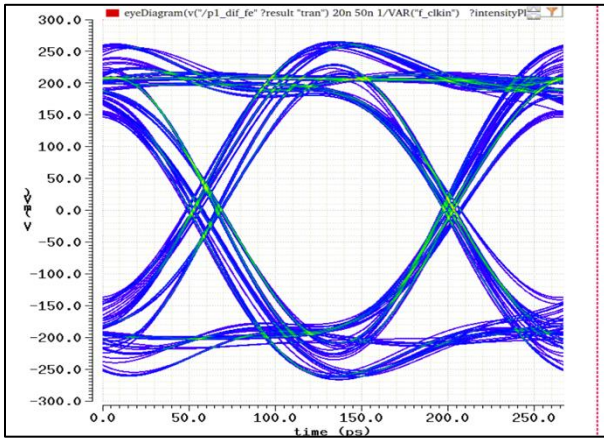


CML Output Driver

- An integrated post-emphasis with programmable coefficients to compensate for channel loss and improved signal integrity.
- Reversed bias diodes are placed at each differential output for ESD protection.
- Transmission channel is modelled with S-parameter data to accurately capture frequency dependent channel loss and guarantee signal integrity.
- The supply and ground connections are modelled with a RLC model while performing post-layout simulations to model bond wires.



- **Wo** RLC on sup/gnd
  - **Wo** noise



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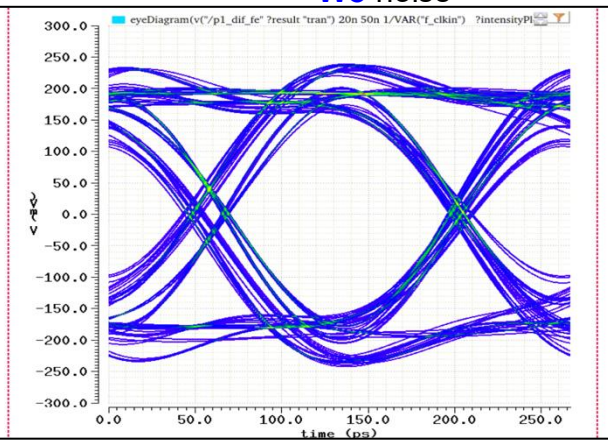

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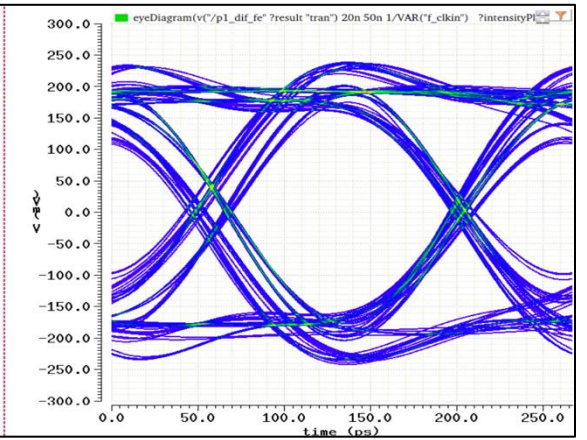
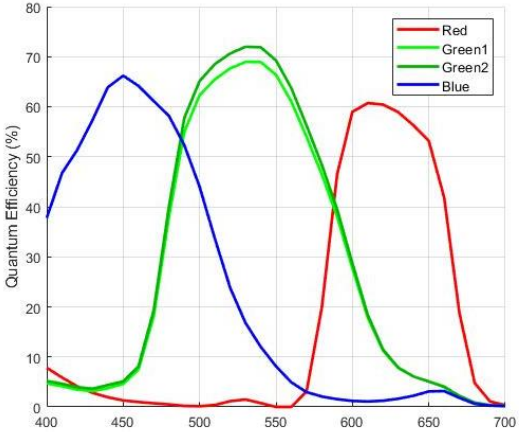


Measured Results

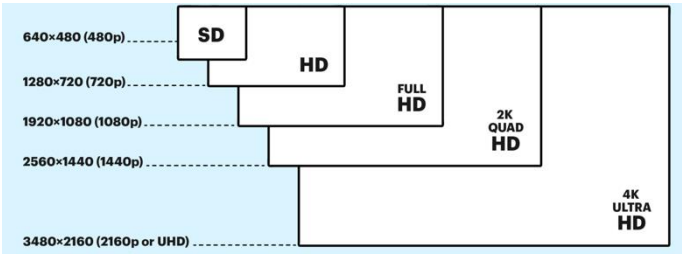
Parameter	Specification
Technology	1P4M, 65nm BSI
Resolution	3840×2160 (Mono and Color)
Pixel Pitch	5 µm
Shutter Type	Voltage Domain Global Shutter
Linear Full Well	8100 e^- (HG), 41300 e^- (LG)
Conversion Gain	170 µV/e^- (HG)
Total Dark Temporal Noise	3.04 e^- (HG)
Row Noise Correction	On-Chip
Max Frame Rate	73,809 FPS (640×6)
ADC Resolution	8b / 10b / 12b
PRNU	2.2% (HG), 2.1% (LG)
DSNU	14.6 e^- (HG), 128 e^- (LG)
Dynamic Range	68 dB (HG)
Max SNR	39 dB (HG)
Quantum Efficiency	67%@430 nm (blue) 73%@530 nm (green) 61%@620 nm (red)
PLS	< −100 dB
Power Consumption	5.5 W
Data Ports	16×outputs @ 7.44 Gbps
Die Size	23.55 mm (H) × 25.6 mm (V)

Format	Bit-Depth	Max FPS
3840×2160 (UHD)	12-bit	**1114**
	10-bit	**1348**
	8-bit	**1680**
2560×1440 (QHD)	12-bit	**2172**
	10-bit	**3000**
	8-bit	**3000**
1920×1080 (Full HD)	12-bit	**2873**
	10-bit	**3968**
	8-bit	**3968**
1280×720 (HD)	12-bit	**4241**
	10-bit	**5857**
	8-bit	**5857**
640×480 (VGA)	12-bit	**6214**
	10-bit	**8582**
	8-bit	**8582**



Resolution vs Frame Rate vs Output Ports

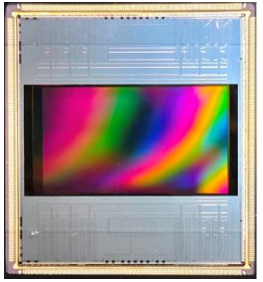
Resolution	Bit-Depth	8top+8bot	6top+6bot	4top+4bot	2top+2bot	8[one-side]	6[one-side]	4[one-side]	2[one-side]
3840×2160 (UHD)	12-bit	**1114**	840	563	283	561	423	283	142
	10-bit	**1348**	1018	680	340	679	513	343	171
	8-bit	**1680**	1267	850	426	847	639	428	214
2560×1440 (QHD)	12-bit	**2172**	1853	1250	630	1099	938	632	318
	10-bit	**3000**	2266	1514	760	1518	1147	766	385
	8-bit	**3000**	2812	1886	948	1518	1423	954	480
1920×1080 (Full HD)	12-bit	**2873**	2192	1108	1108	1460	1460	1114	563
	10-bit	**3968**	2653	1339	1339	2016	2016	1348	680
	8-bit	**3968**	3306	1673	1673	2016	2016	1680	850
1280×720 (HD)	12-bit	**4241**	4241	4241	2440	2172	2172	2172	1250
	10-bit	**5857**	5857	5857	2957	3000	3000	3000	1514
	8-bit	**5857**	5857	5857	3683	3000	3000	3000	1886
640×480 (VGA)	12-bit	**6214**	6214	6214	6214	3219	3219	3219	3219
	10-bit	**8582**	8582	8582	8582	4446	4446	4446	4446
	8-bit	**8582**	8582	8582	8582	4446	4446	4446	4446



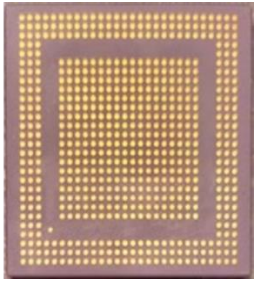
First Video Capture from Camera

First video capture from camera: 2560x1440 @1100FPS

- Weight: Camera=300gram; Cable 5m=200gram
- Size 6cm x 6cm x 5cm
- 32G memory



ForzaFAST581 Sensor



268-pin LGA

Conclusion

- A low-noise high-frame-rate global shutter CMOS Image Sensor is UHD resolution(3840x2160) targeting high-speed machine vision applications is presented.

- The sensor supports video capture at up to 1100FPS at 12-bits and 1600FPS at 8-bits at full resolution achieving 3e- read noise while maintaining image quality.

- For compact camera integration and low-power operation, the sensor is designed to stream videos through 16 CML data ports, each operating at 7.44Gbps achieving a 119Gbps data throughput.

- Sensors offer several configuration options to optimize frame rate at the expense of noise, image format, and bit resolution for various applications.

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Thank You!
Questions?

Rowtime for various modes

Rowtime for Various Port Configurations (us)									
Column Width	Bit Depth	8 top + 8 bot	6 top + 6 bot	4 top + 4 bot	2 top + 2 bot	8 one side	6 one side	4 one side	2 one side
3840 Columns	12-bit	2.45	3.24	4.84	9.64	2.45	3.24	4.84	9.64
	10-bit	2.04	2.70	4.03	8.03	2.04	2.70	4.03	8.03
	8-bit	2.04	2.70	4.03	8.03	2.04	2.70	4.03	8.03
2560 Columns	12-bit	1.63	2.17	3.24	6.43	1.63	2.17	3.24	6.43
	10-bit	1.35	1.81	2.70	5.35	1.35	1.81	2.70	5.35
	8-bit	1.35	1.81	2.70	5.35	1.35	1.81	2.70	5.35
1920 Columns	12-bit	1.63	1.63	2.45	4.84	1.63	1.63	2.45	4.84
	10-bit	1.35	1.35	2.04	4.03	1.35	1.35	2.04	4.03
	8-bit	1.35	1.35	2.04	4.03	1.35	1.35	2.04	4.03
1280 Columns	12-bit	1.63	1.63	1.63	3.24	1.63	1.63	1.63	3.24
	10-bit	1.35	1.35	1.37	2.70	1.35	1.35	1.35	2.70
	8-bit	1.35	1.35	1.35	2.70	1.35	1.35	1.35	2.70
640 Columns	12-bit	1.63	1.63	1.63	3.24	1.63	1.63	1.63	3.24
	10-bit	1.35	1.35	1.35	2.70	1.35	1.35	1.35	2.70
	8-bit	1.35	1.35	1.35	2.70	1.35	1.35	1.35	2.70

For rowtimes less than or equal to	1.65	us
Reset Sampling	0.57	us
Signal Sampling	0.61	us

For rowtimes less than or equal to	1.65	us
Reset Sampling	0.83	us
Signal Sampling	0.83	us

Transfer Time	4.65	us