A Flexible 14-bit Column-Parallel ADC Concept for Application in Wafer-Scale X-ray CMOS Imagers

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Henk Derks, Daniel Verbugt, Laurens Korthout, Wim de Haan, Wasim Muhammad, Pierluigi Albertini
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Why a column parallel ADC?

• For reasons of *performance*
  – No sensitive analog off-chip connections needed resulting in less induced crosstalk and noise
  – Parallel conversion of columns resulting in high-speed and high resolution readout of large pixel arrays

• For reasons of *costs*
  – No separate discrete ADCs and PCB area required
Key specifications

- Technology node: **0.35μm**, four metal, dual poly CMOS
- Dimensions single ADC: **67 (100) μm x 2800 μm**
- Conversion time: total 58 cycles with a clock period of 100ns (10MHz clock) results in a conversion time of **5.8μs**
- Conversion gain: **~110μV/DN** @ ADCref 2.8V
- Total noise: 1.6DN / **175μVRMS**
- (Single) ADC current consumption **90μA** @ 3.5V
Converter principle

- Principle of ADC is based on a multi-slope thermometer code search methodology: this is a variant of successive approximation
- This architecture has been selected for reasons of size, speed, resolution and power consumption
- 14 bits are determined in 4 scans consisting of repetitive charge redistribution between unit capacitors

Scan 1, caps charged to Vref

Scan 2, caps charged to 0;1/16Vref;......;15/16Vref

Scan 3, single cap charged to 0;1/16Vref;......;15/16Vref

Scan 4, cap charged to 0;1/64Vref;………; 3/64Vref
Block diagram 14-bit col parallel ADC

Operating principle based on (capacitor) matching: 14 bit is limit for resolution
Conversion process

- ADC input
- 4-bit idle
- 4-bit idle
- 4-bit idle
- 2-bit idle
- 1 step back
- Scan 1
- Scan 2
- Scan 3
- Scan 4
Overall dimensions and block ratios

- ~2.8mm
- 67 μm
- 100 μm

to accommodate various pixel dimensions; shielding has been added for 100μm variant
Critical design aspects

Charge injection of switches

Crosstalk between inputs

Non-linear capacitance of switch

Correct switch Timing and settling

Crosstalk from switch control signals to sensitive analog nodes: lay-out is critical!

Non-linear (voltage dependent) input capacitances

Reference part

Logic

V_{\text{REF}}

V_{\text{PIXEL}}

SHS

SHR

C_1

C_2

C_3

C_4

Comp.

Count

Shadow Register

SCAN 1

SCAN 2

SCAN 3

SCAN 4

Clk

V_{\text{REF}}

14 bit

Clk

Rst

EoC

Clk

14 bit

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One ADC serves multiple pixel dimensions required for multiple applications
Block diagram binning implementation

1:2 binning is basically averaging the output of two vertically adjacent pixels implemented by using the offset compensation capacitors as capacitive divider.
DFT implementations

Artificial pixel

Analog test bus

14 bit
Conclusions

- An on-chip column-parallel ADC is attractive for cost and performance reasons
- The presented successive approximation ADC concept is power efficient, flexible and serves various applications