NIR SPADs and fast-gating circuits

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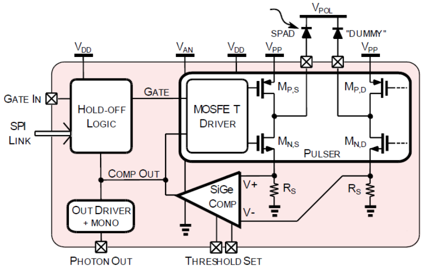
1st International SPAD Sensor Workshop – ISSW 2018
Les Diablerets, February 26th, 2018

Outline

- InGaAs/InP SPAD
  - Device structure
  - Performance

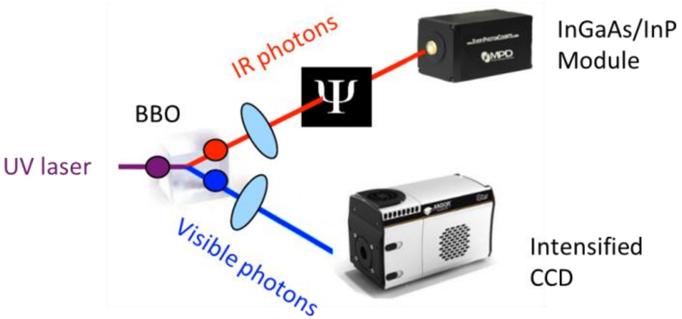


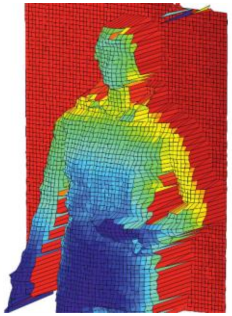
- Circuits for InGaAs/InP SPAD
  - SPAD with integrated quenching resistor
  - GHz sinusoidal gating
  - Integrated fast-gated active quenching circuit (ASIC)

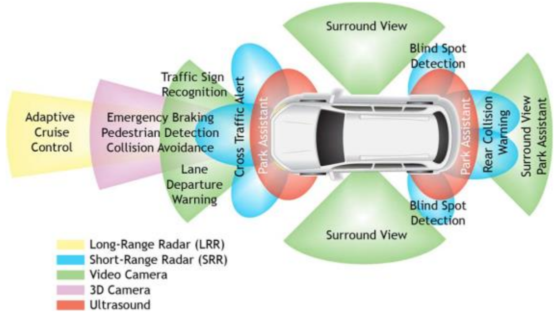
InGaAs/InP SPAD

Single-photon counting in the NIR (1 – 1.6 µm)

- Quantum Information Processing and Communication
- Quantum Key Distribution (QKD)
- Eye safe ranging (LIDAR)
- Unconventional (ghost, non-line-of-sight, …) imaging
- Time-resolved diffused optical spectroscopy
- Photodynamic therapy (PDT) for cancer treatment
- Optical testing of VLSI circuits
- Photonics research in the 1 µm – 1.6 µm range







Detector + electronics tailored for the specific application!

InGaAs/InP SPAD

Photons up to ~ 1.6 µm → E_g < 0.8 eV → **InGaAs** (E_g ~ 0.75 eV)

But low E_g means:

- higher noise → **cooling** is mandatory (T ~ 230 K)
- strong tunneling → higher E_g material is required for avalanche → **InP** with E_g ~ 1.35 eV

Separate Absorption, Charge and Multiplication (SACM)

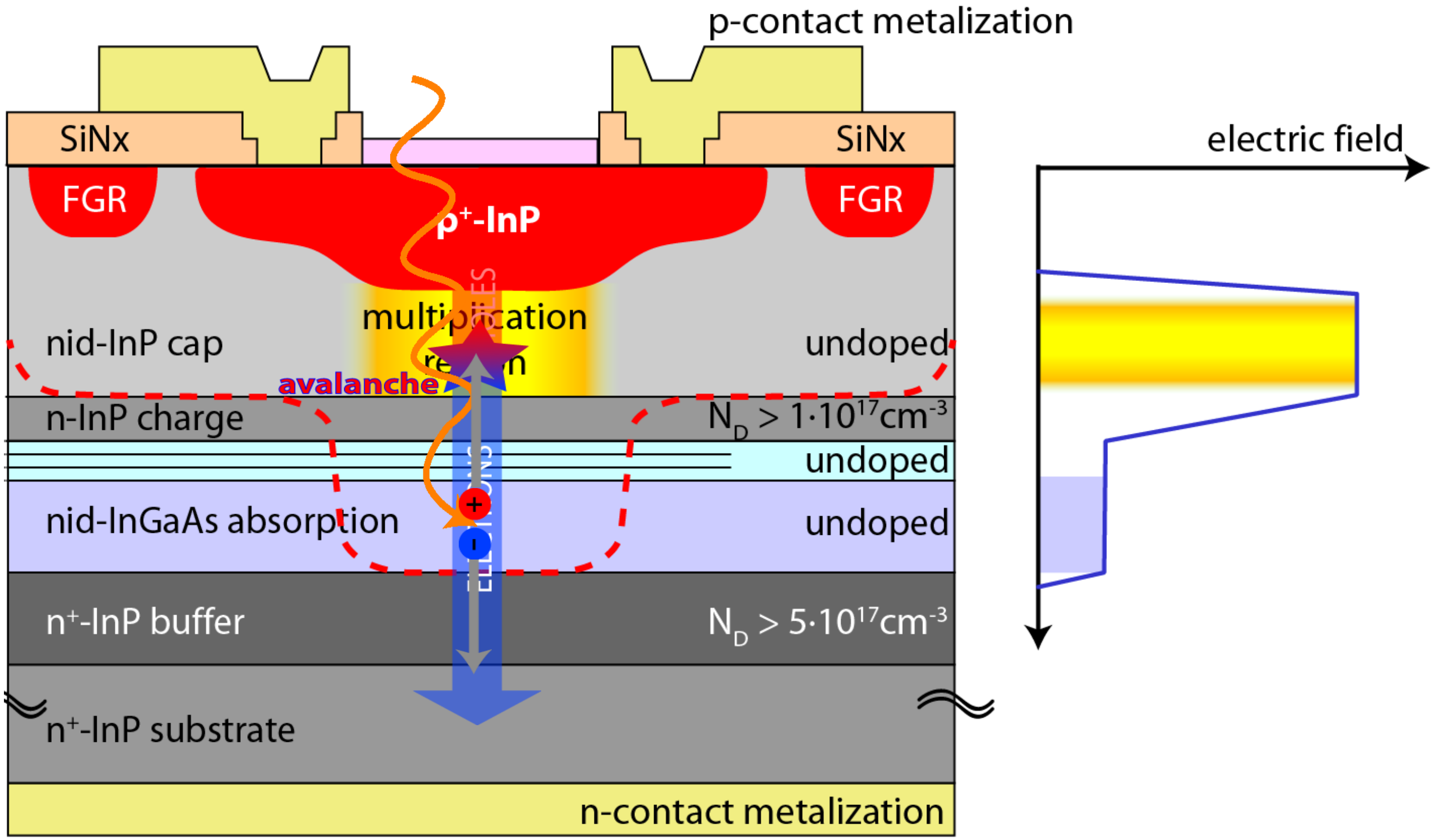
Absorption:	**$In_{0.53}Ga_{0.47}As$**	(E_g ~ 0.75 eV)
Charge:	**highly-doped InP**	(E_g ~ 1.35 eV)
Multiplication:	**InP**	(E_g ~ 1.35 eV)

Planar technology (no MESA) for lower noise and higher reliability

Front-illuminated structure → Well-defined collection area

Back-illuminated structure → Suitable for arrays

InGaAs/InP SPAD



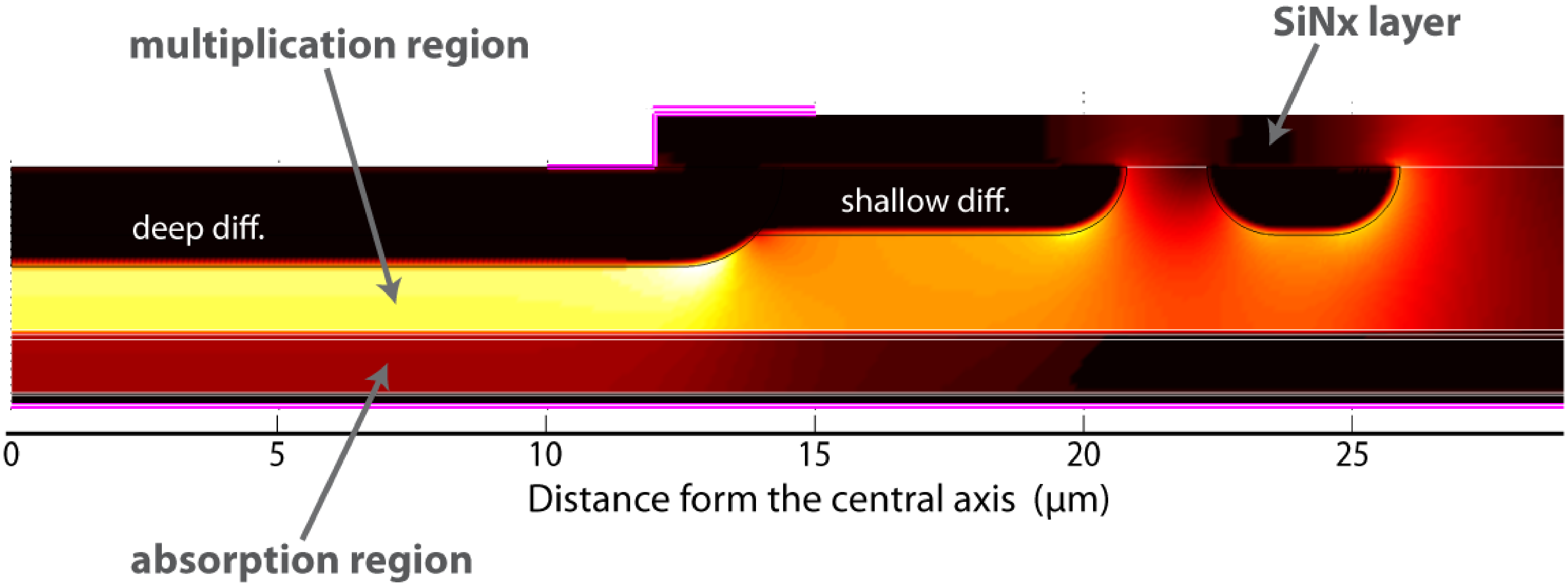
(Front-illuminated structure)

Design of InGaAs/InP SPAD

Optimized double Zn diffusion (depths and diameters)

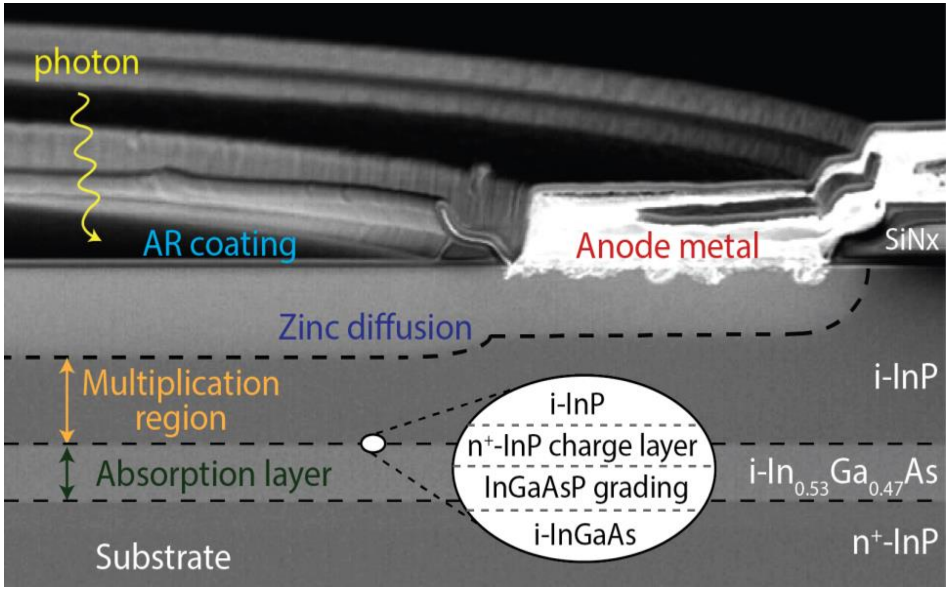
- good uniformity in the active area ($\Delta V_{BD} < 4\%$)
- no activation in the periphery

→ **Uniform sensitivity and low timing jitter**

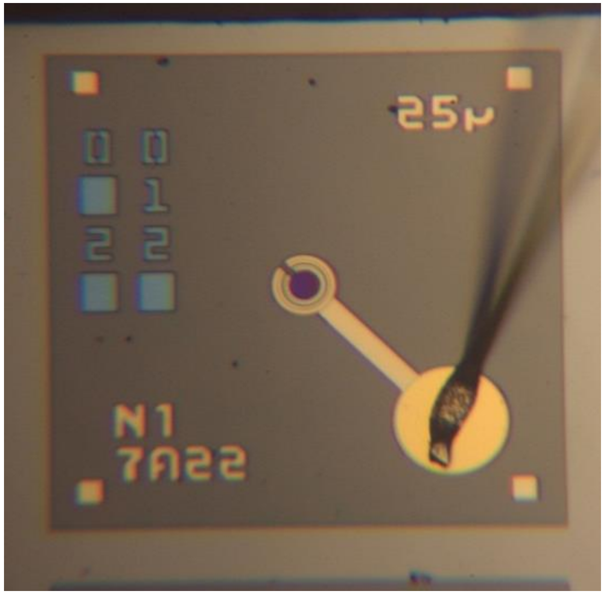


(Electric field simulation at 200 K & V_{EX} = 5 V)

Fabricated InGaAs/InP SPAD

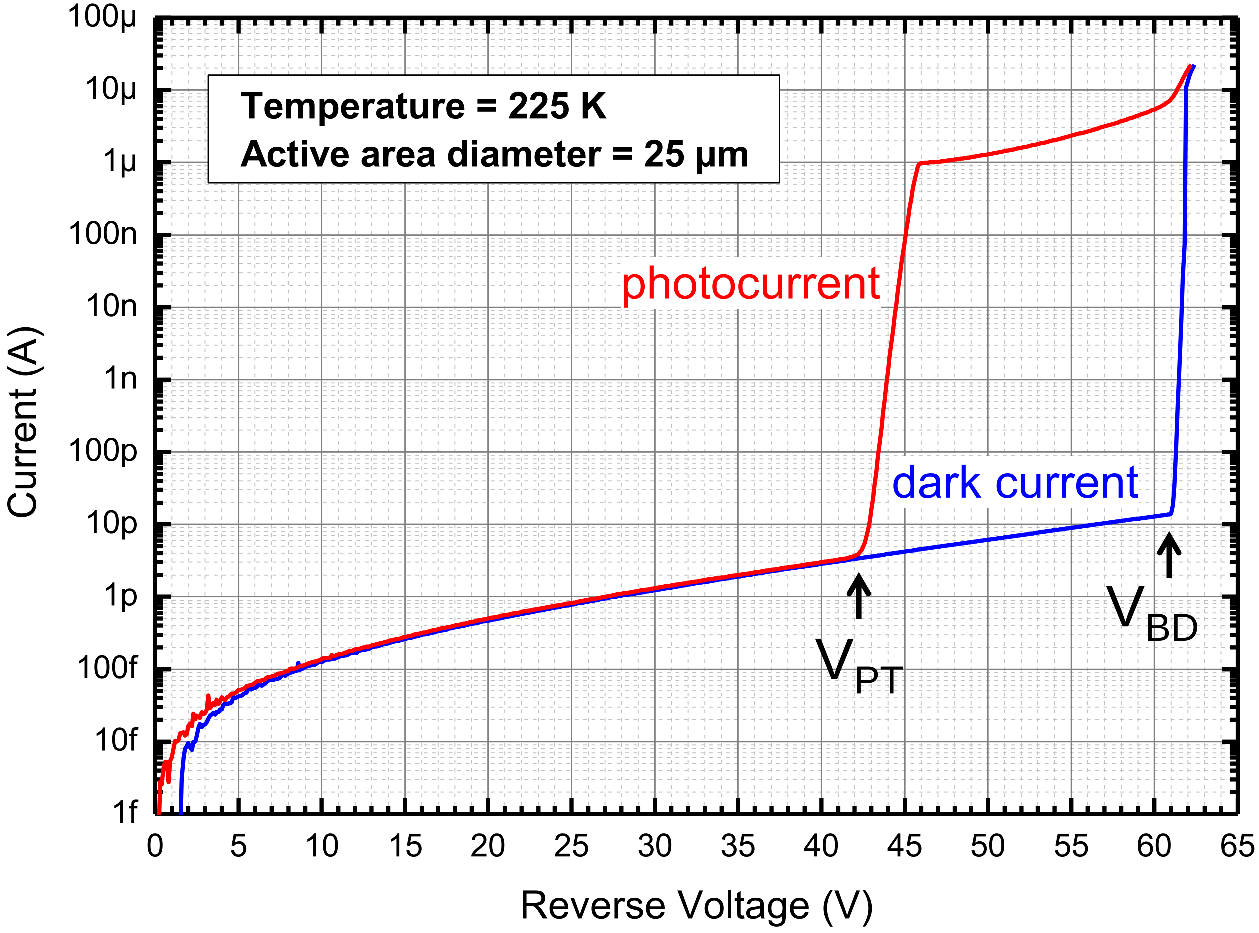


(SEM cross-section)



(top view)

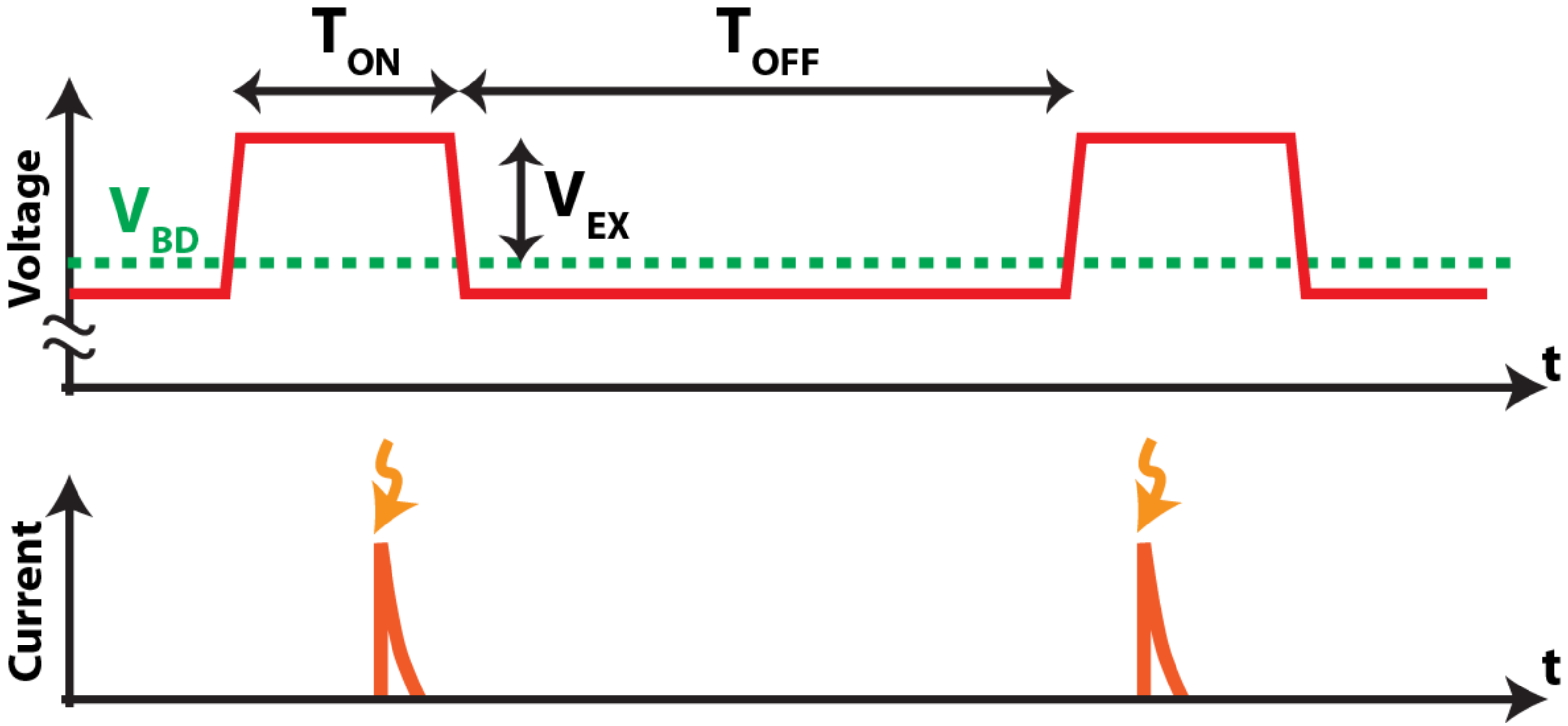
I-V curve at low temperature



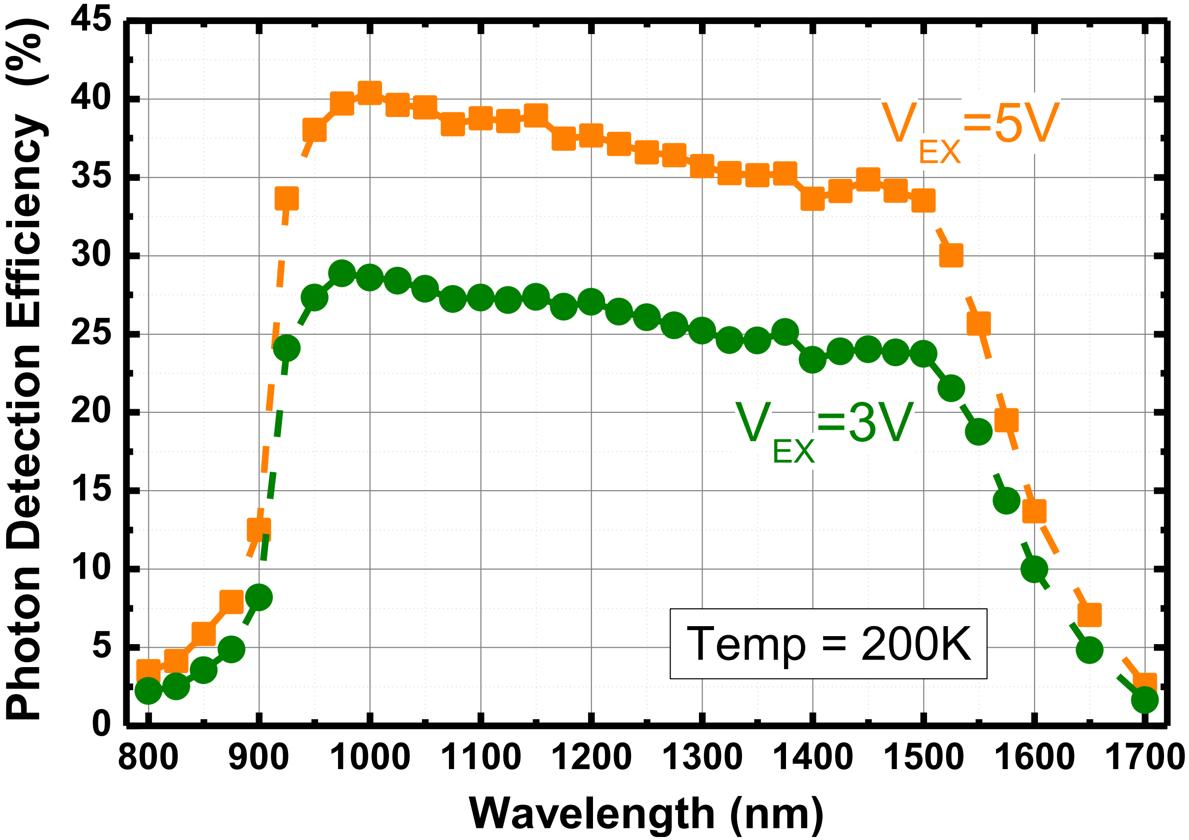
Low dark current: I_{dark} ~ 10 pA @ V_{BD} – 1 V, sharp breakdown knee, large V_{BD} – V_{PT} difference

Gated-mode operation

- SPAD is enabled during **Gate-ON time**
- SPAD is held OFF to empty traps → reduce afterpulsing
- **Gate period T_{GATE}** = $T_{ON} + T_{OFF}$



Photon detection efficiency

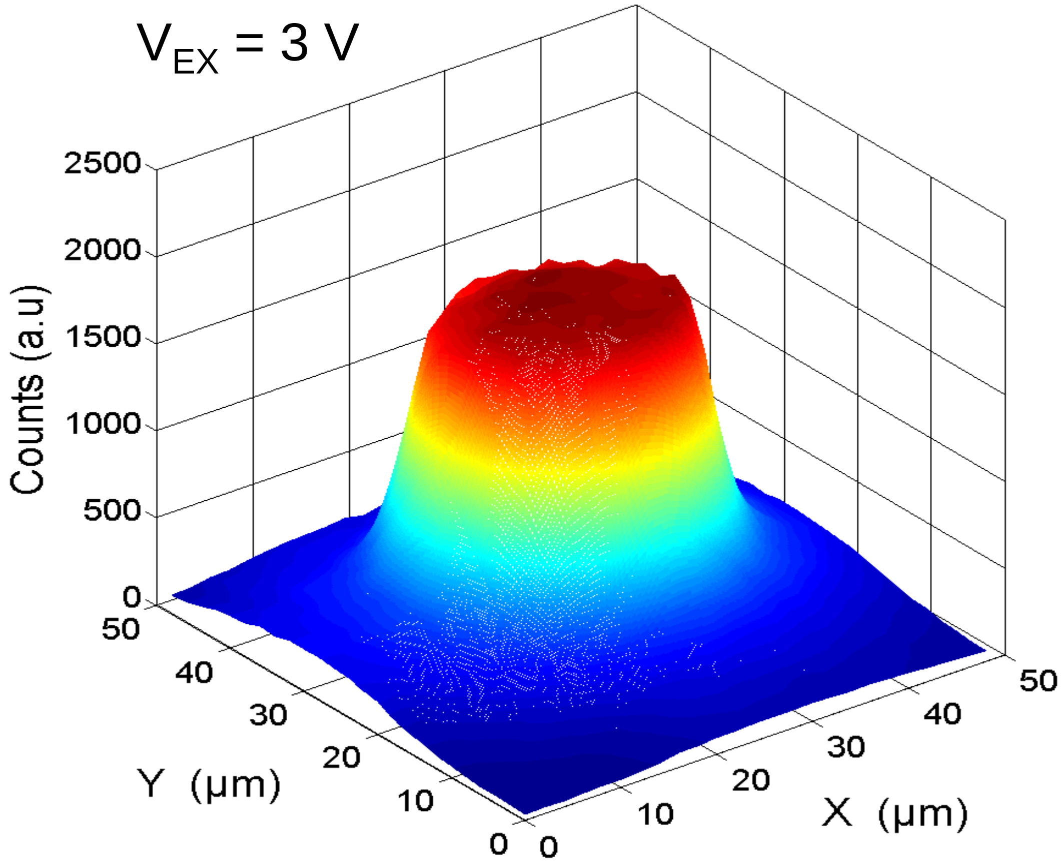


Good photon detection efficiency:

- 40% @ λ = 1000 nm, V_{EX} = 5 V
- 25% @ λ = 1550 nm, V_{EX} = 5 V
- still 3% @ λ = 1700 nm, V_{EX} = 5 V

Active area uniformity

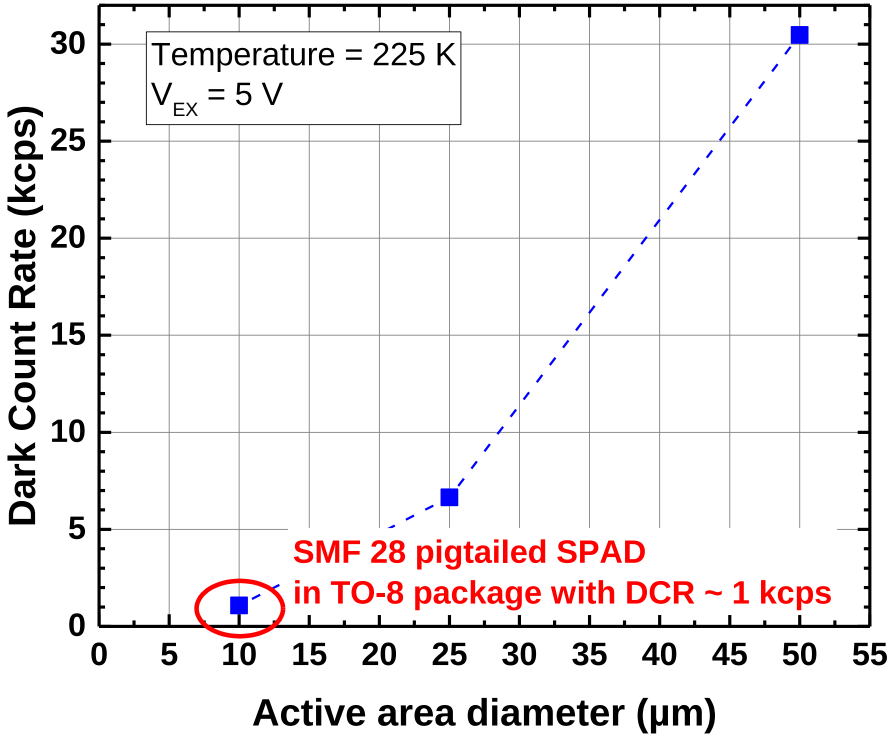
V_{EX} = 3 V



- Uniform sensitivity within the active area
- Sharp edges

Uniformity improves at higher excess bias
(due to saturation of avalanche triggering probability)

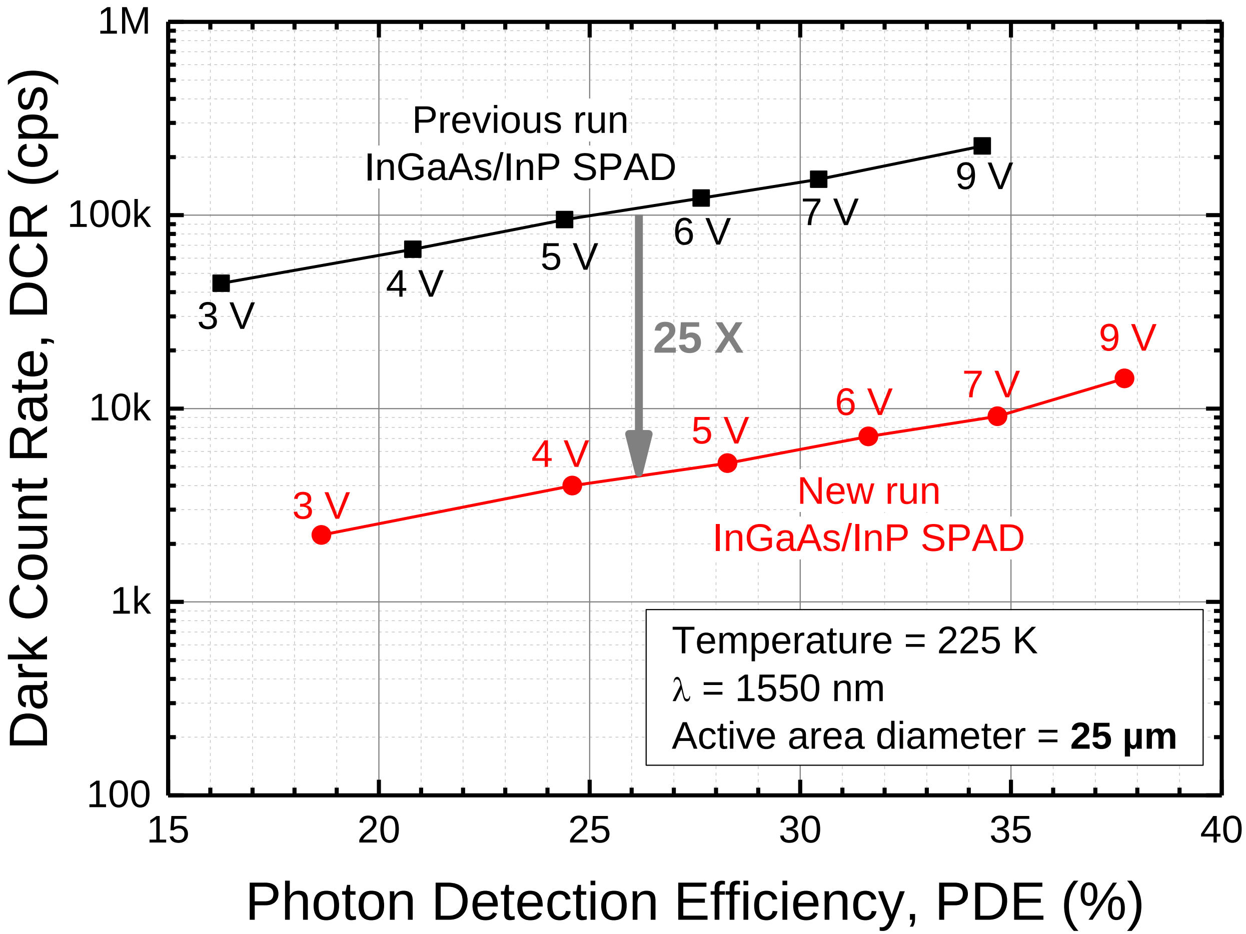
Low dark-count-rate InGaAs/InP SPAD



SMF 28 pigtailed SPAD in TO-8 package with DCR ~ 1 kcps

- DCR scales with active area → bulk origin
  (while dark current scales with perimeter, i.e. it is peripheral leakage)
- 10 µm InGaAs/InP SPAD with DCR of few kcps
- 10 µm SPADs have been fiber pigtailed (Micro Photon Devices – MPD)

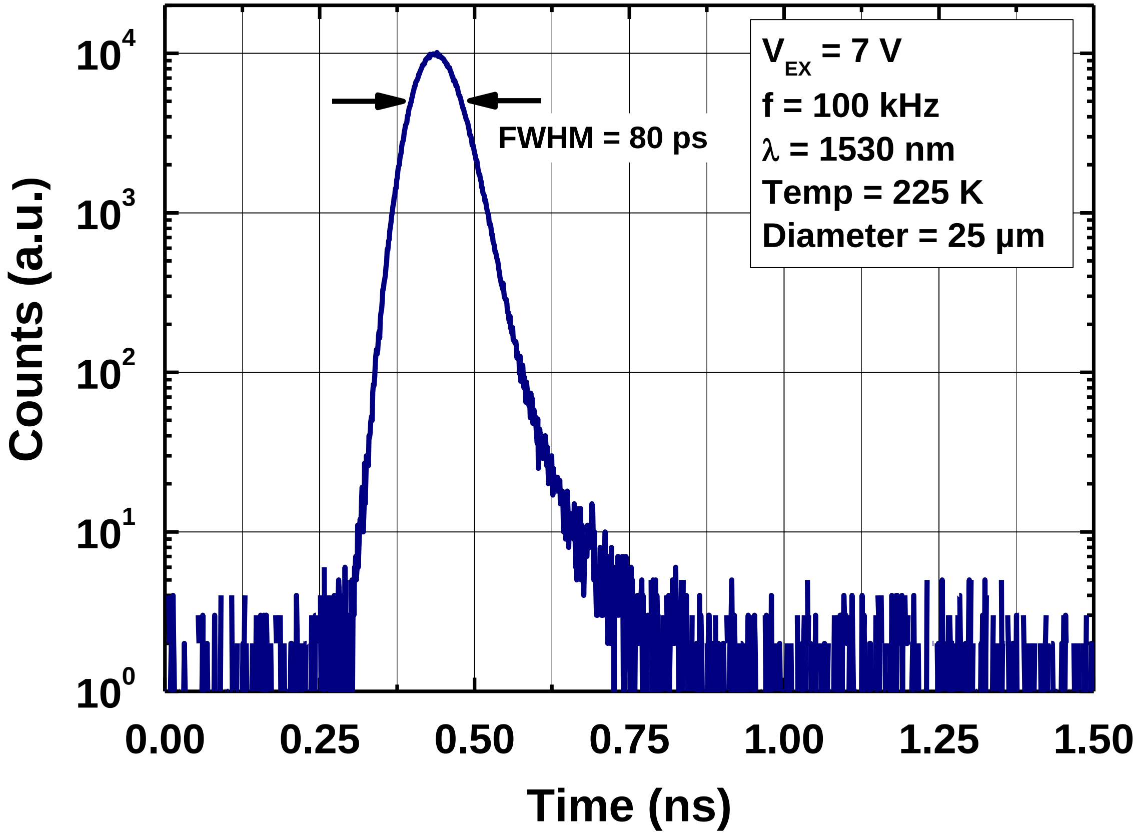
Impact of design on dark count rate



25 times lower DCR at a given PDE by improving SPAD design

→ There is room for further improvement!

Temporal response



Sharp and "clean" time response FWHM < 80 ps @ 7 V

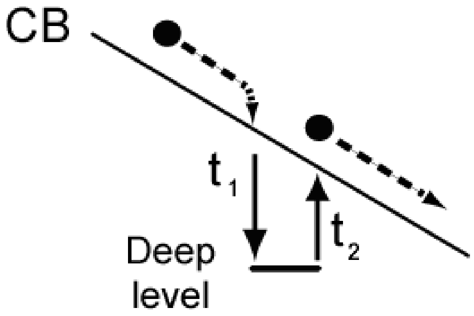
- Near **Gaussian** distribution
- **Short exponential tail** (τ = 58 ps)

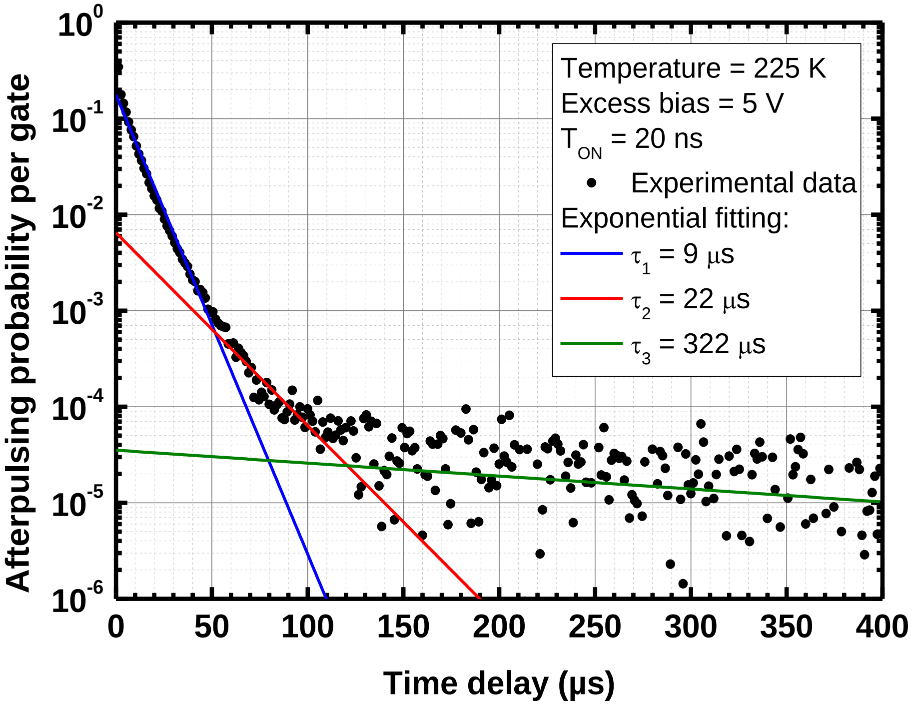
Afterpulsing

Main drawback of InGaAs/InP SPADs: **afterpulsing**

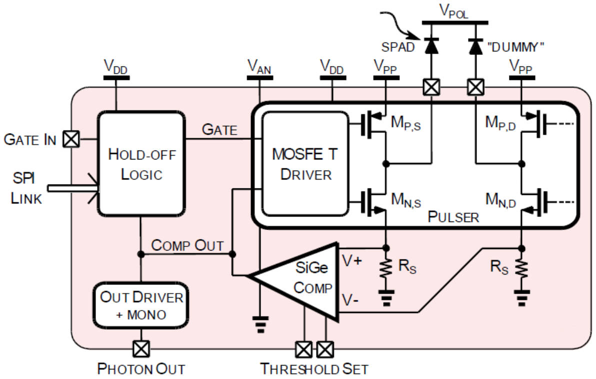
- Some avalanche carriers get trapped in deep levels in InP multiplication region
- Delayed release triggers “afterpulse” avalanches

➔ **Limitation to maximum count rate**





Here is an example where different traps release carriers with different time constants (10’s or even 100’s μs!)



Circuits for high count rate InGaAs/InP SPAD systems

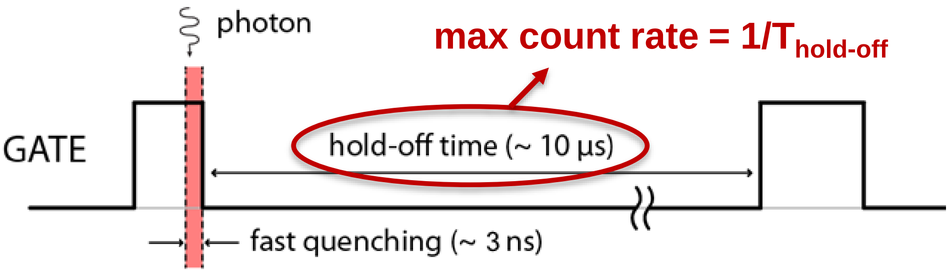
Afterpulsing reduction techniques for higher count rate

Reduce concentration of deep levels

→ challenging task (improved fabrication process)

Long hold-off time before re-arming

→ not an option at high rates



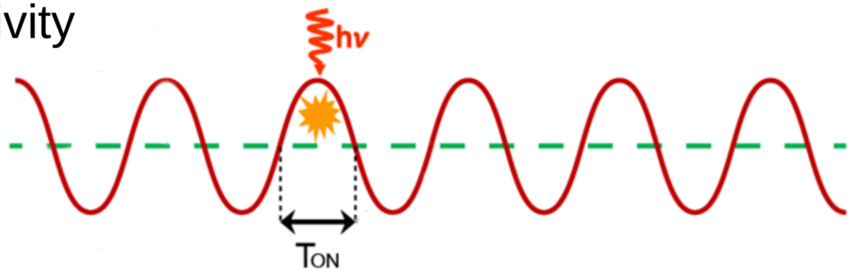
max count rate = $1/T_{\text{hold-off}}$

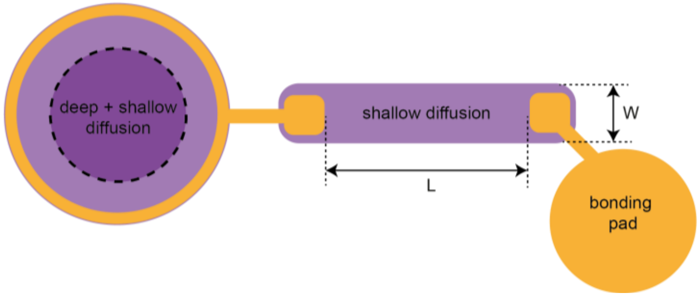
Reduce avalanche carriers

fast quenching (monolithically integrated passive quenching or ASIC)

→ either gated or free-running mode
→ moderately high count rates (1–10 MHz)

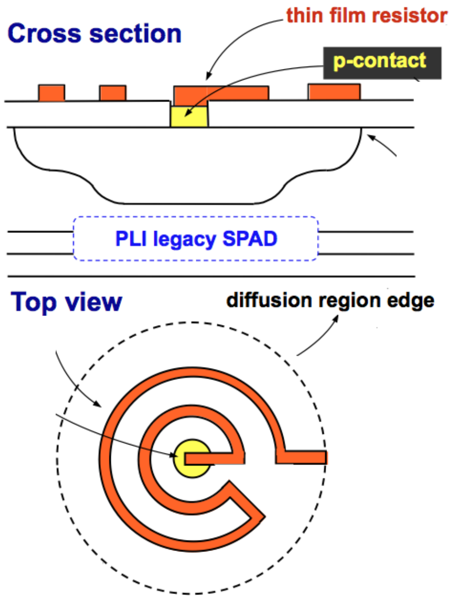
short gates (<< 1 ns): → very high (> 100 MHz) count rates
→ complex RF transients suppression
→ non-flat sensitivity

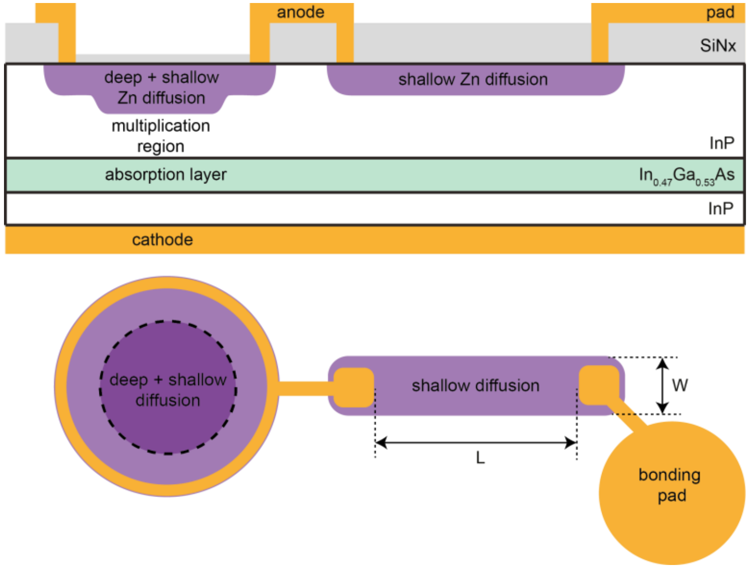




SPAD with integrated quenching resistor

SPAD with integrated quenching resistor





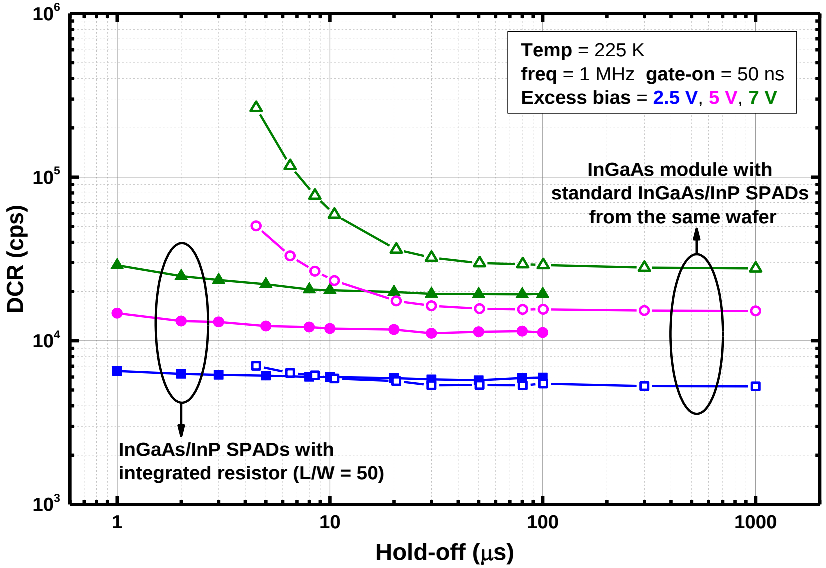
Others' implementation (PLI NFAD):

- Thin film resistors (up to MΩ)
- Additional fabrication steps and masks required
- Slow re-arm (100 ns ÷ 1 μs)

PoliMi implementation:

- No additional fabrication steps: Zn shallow diffusion exploited
- kΩ resistor: - quasi-quenching
  - faster re-arm (< 100 ns)

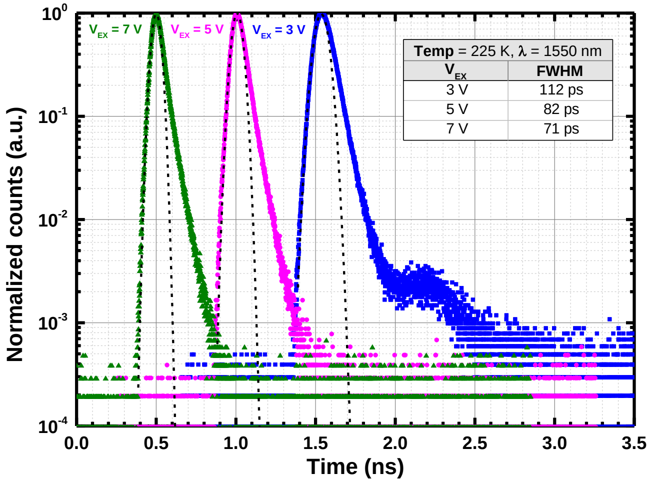
Afterpulsing of InGaAs/InP SPAD with integrated resistor



InGaAs module with standard InGaAs/InP SPADs from the same wafer

InGaAs/InP SPADs with integrated resistor (L/W = 50)

Significant afterpulsing reduction

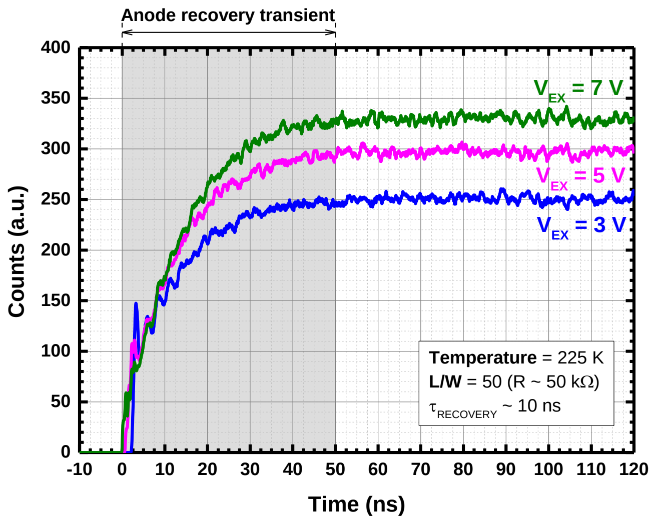


Temp = 225 K, λ = 1550 nm

V_{EX}	FWHM
3 V	112 ps
5 V	82 ps
7 V	71 ps

Good temporal response

Faster recovery time with τ = 10 ns

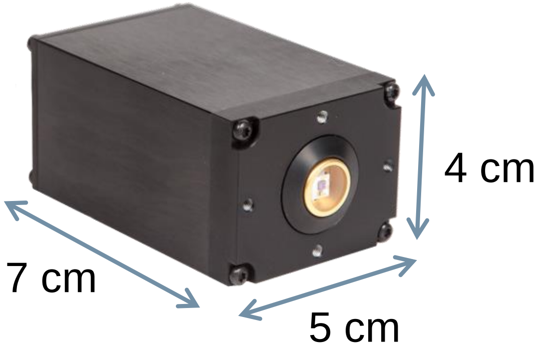


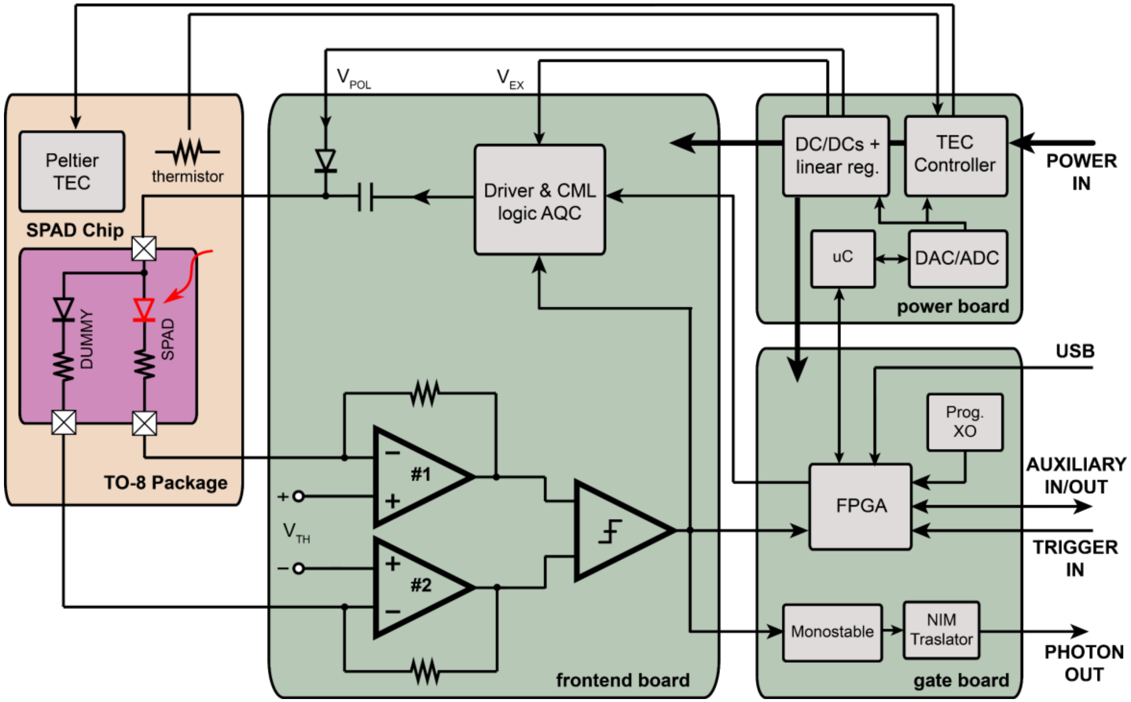
Temperature = 225 K
L/W = 50 (R ~ 50 kΩ)
$\tau_{RECOVERY}$ ~ 10 ns

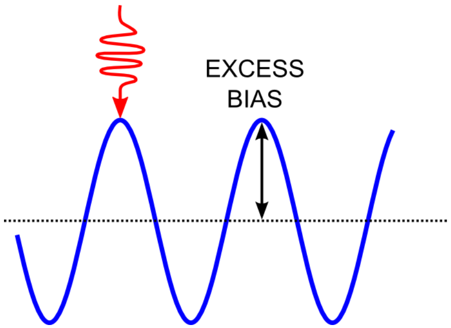
Design of a compact module

Detector, front-end electronics and cooling housed in a small case

- Easy integration in optical setups
- Easy to use and configurable



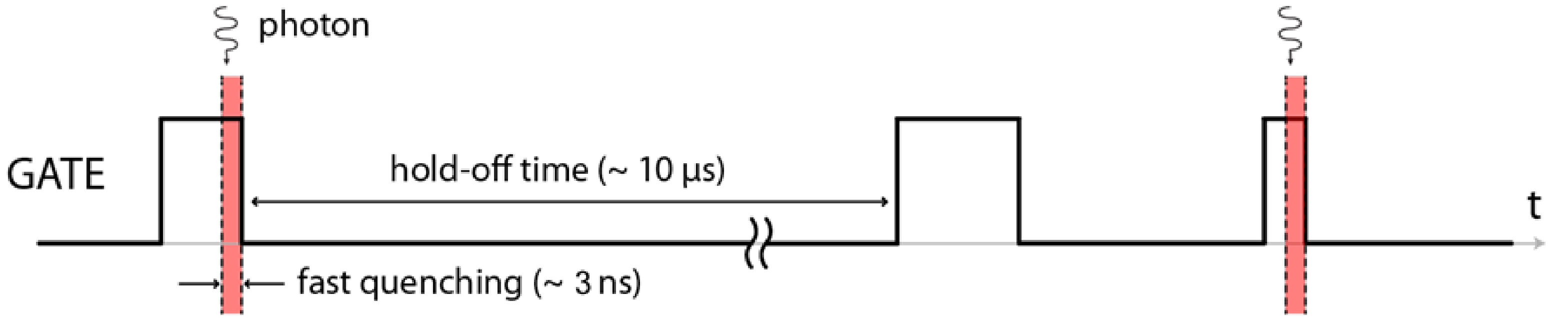




GHz sinusoidal gating with SPAD-dummy balancing approach

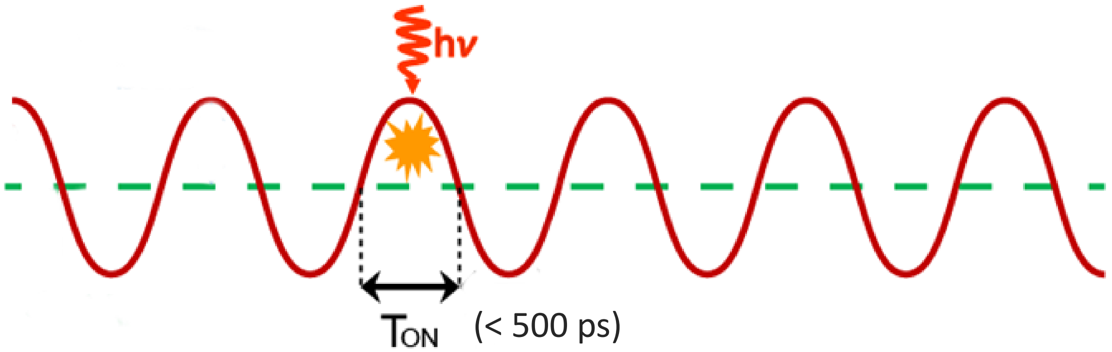
Gating of InGaAs/InP SPADs

Square-wave gate



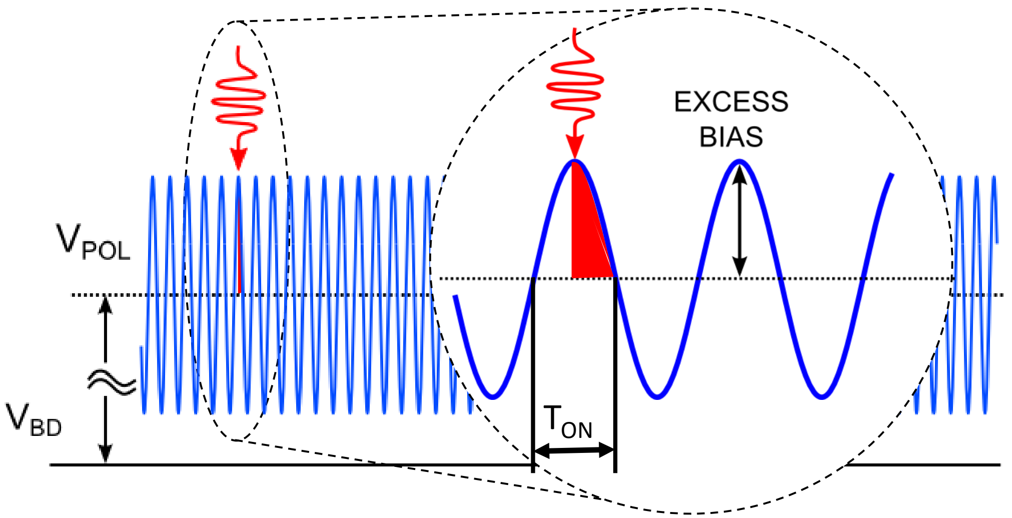
- ✓ Flat sensitivity (few %)
- ✓ Low time jitter (< 100 ps)
- ✗ High avalanche charge
- ✗ Low count rate

GHz sine-wave gate



- ✓ Short quenching time
- ✓ Very high count rate
- ✗ Complex systems
- ✗ Non-flat sensitivity

Gigahertz sinusoidal gating - requirements



Gate signal at f_G > 1 GHz for fast avalanche quenching

f_G tunable in a wide range (900-1400 MHz) for:

- Synchronization with different external laser systems
- Best trade-off between afterpulsing and detection efficiency

Adjustable excess bias:

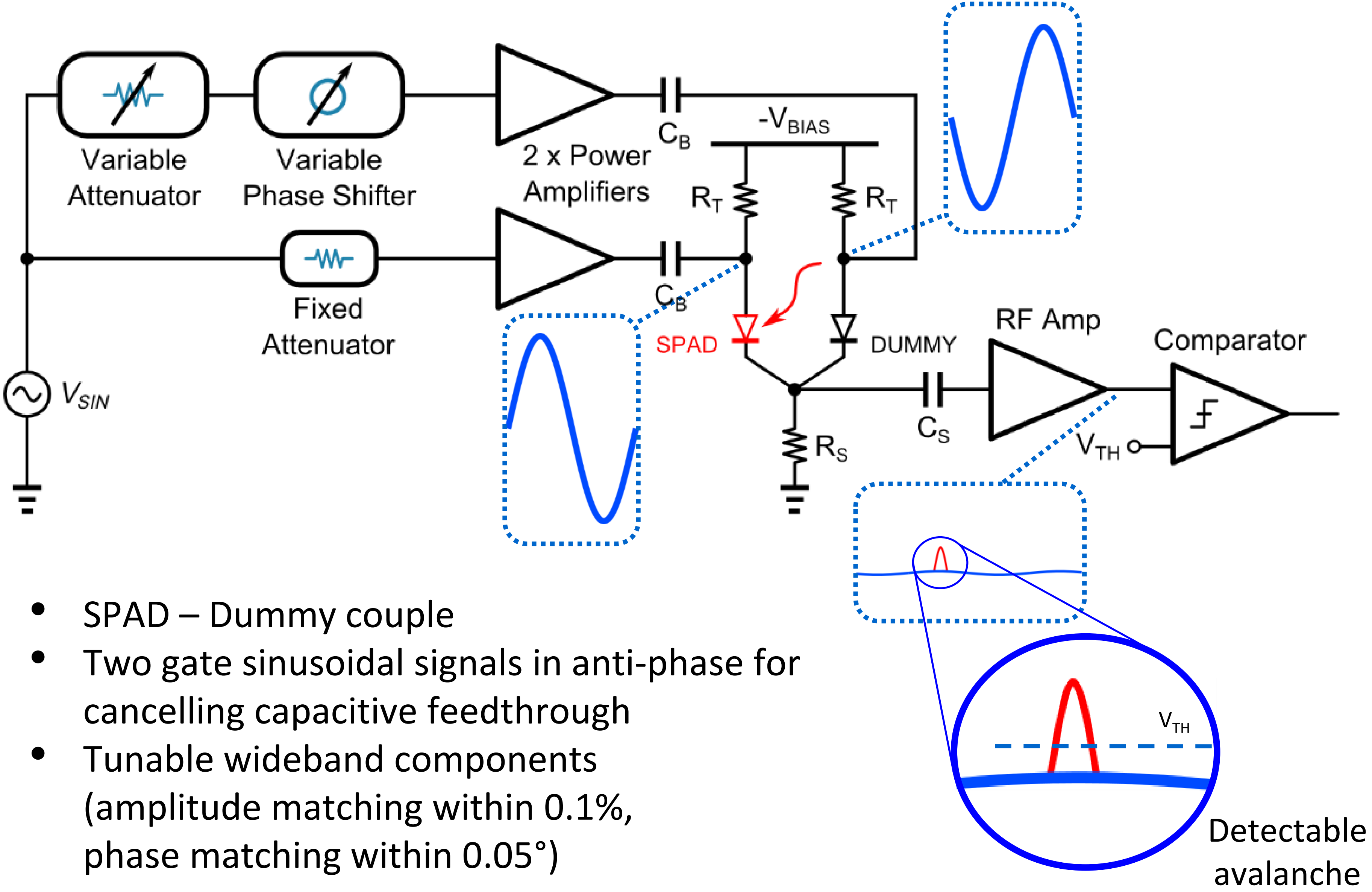
- for optimizing PDE, DCR, afterpulsing, timing jitter
- Up to 7 V (27 dBm!)

Long-term stability

- Feedback for gate feed-through rejection

Suitable for rack mounting

PoliMi “SPAD-dummy” balanced configuration



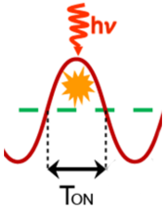
Detectable avalanche

- SPAD – Dummy couple
- Two gate sinusoidal signals in anti-phase for cancelling capacitive feedthrough
- Tunable wideband components (amplitude matching within 0.1%, phase matching within 0.05°)

Gigahertz sinusoidal gating of InGaAs/InP SPAD

PoliMi sine-wave gate results:

(compared to square-gate system with similar SPAD)

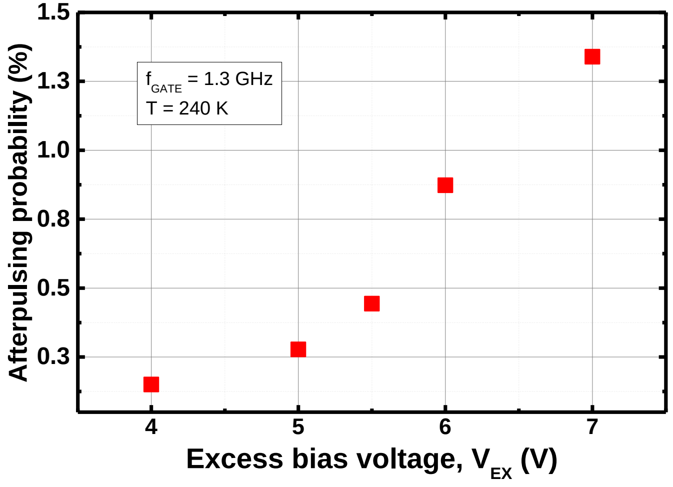


At the same low afterpulsing probability:		**1.5 %**	1.5 % (*)
✓	**Very high count rate**	**650 Mcps**	< 100 kcps
✓	**Good peak detection efficiency**	**~ 30 %**	~ 30 %
✓	**Narrow temporal response**	**< 70 ps**	< 70 ps

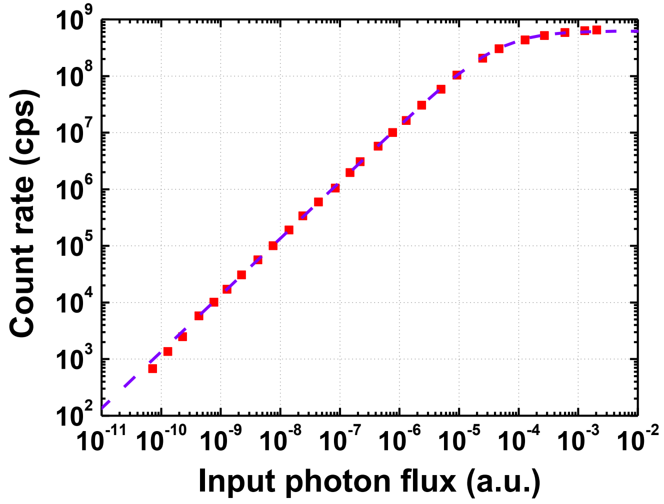
All results with 7 V excess bias unless specified – (*) T_{ON} = 5 ns, T_{HO} = 10 μs

Gigahertz sinusoidal gating of InGaAs/InP SPAD

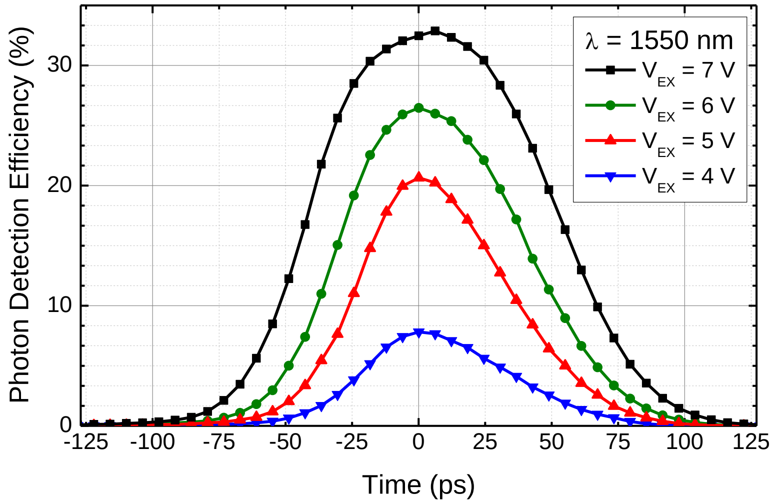
Afterpulsing probability



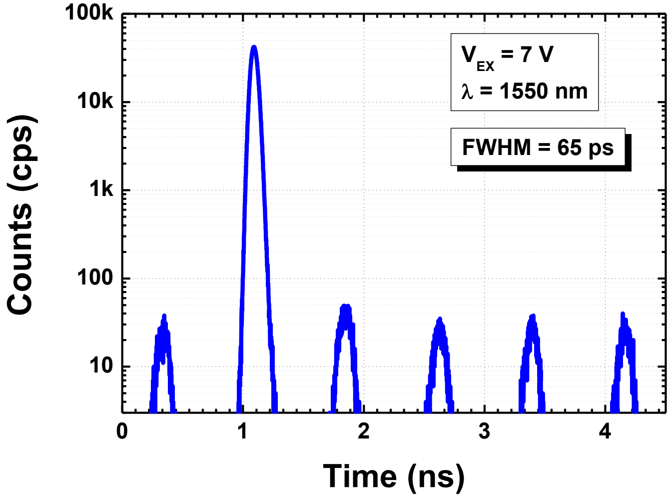
Linearity



Photon detection efficiency



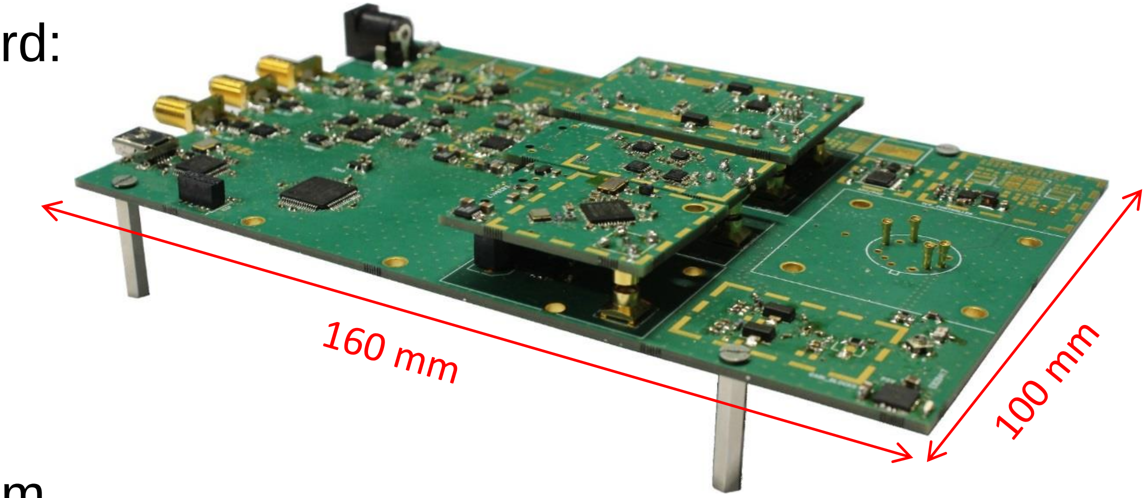
Temporal response



Towards compact gigahertz sinusoidal gating of SPADs

Main board of the new system:

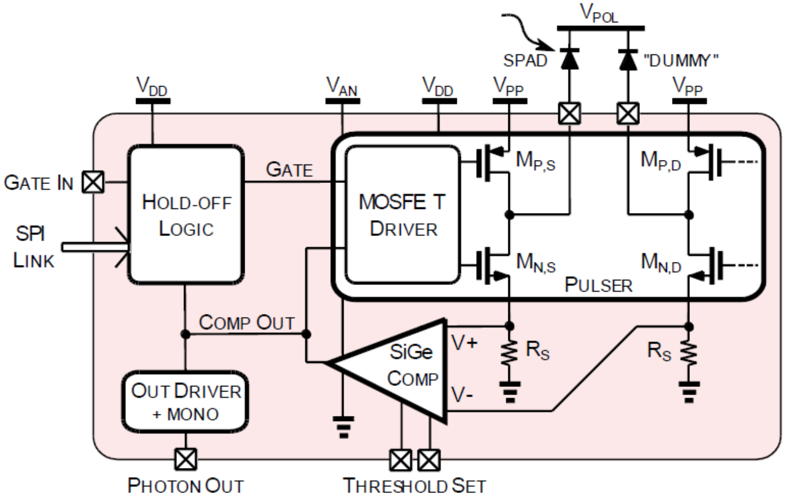
- All the basic blocks on board:
  - Gate generation
  - Gate amplification
  - Avalanche readout
  - Feedback control system

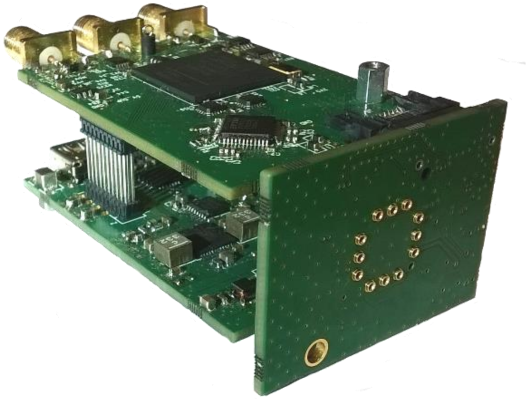


- PLL with multiple outputs generates both gate signals (800 – 1500 MHz)
- Programmable gain amplifier to set gate amplitude (up to V_{EX} = 7 V)
- Readout amplifiers with 3 GHz bandwidth and ultrafast comparator

SiGe integrated circuit for fast gating SPADs

Integrated fast-gated active quenching circuit (ASIC)





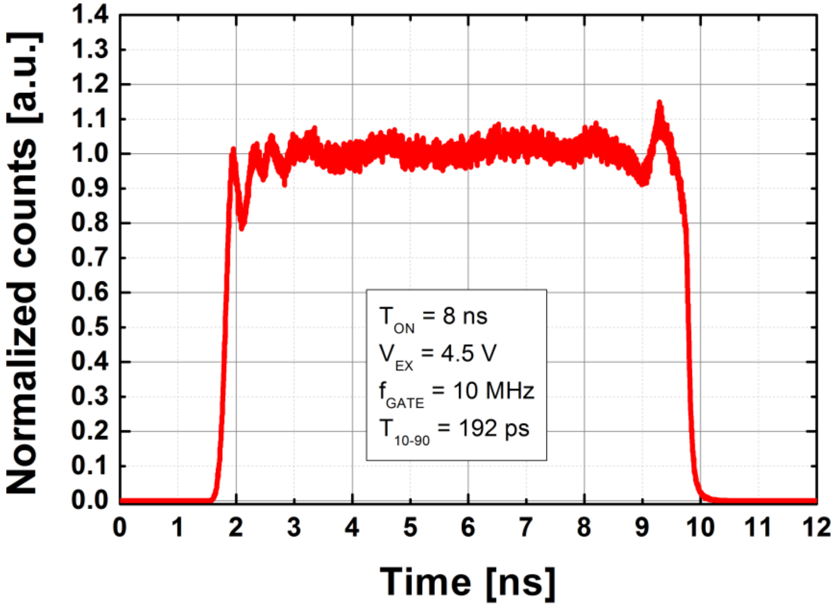
Integrated circuit (SiGe BiCMOS technology):

- SPAD front-end based on “SPAD-dummy” approach
- Quenching time < 1 ns
- Very fast transition times (< 200 ps @ V_{EX} = 5 V)
- High repetition rate (up to 250 MHz)
- Low timing jitter (FWHM < 90 ps with InGaAs/InP SPAD, intrinsic < 20 ps)
- Mounted in a 12 pin TO-8 package → compact module
- Ready for arrays!

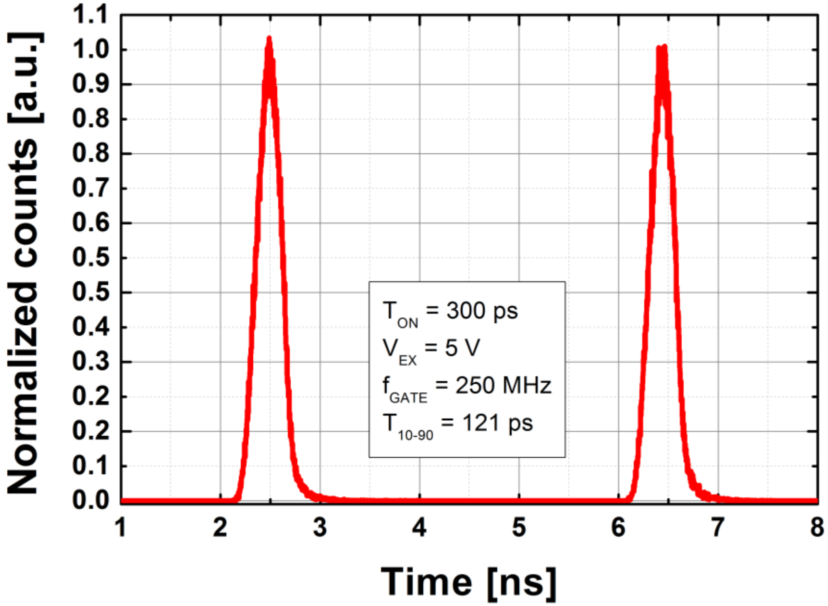
Integrated fast-gated active quenching circuit

- Very fast rise/fall edges (< 200 ps @ V_{EX} = 5 V) → **short gate (300 ps)**
- Flat sensitivity (±15%) inside long gate windows
- Free-running mode available

Long gate (8 ns)



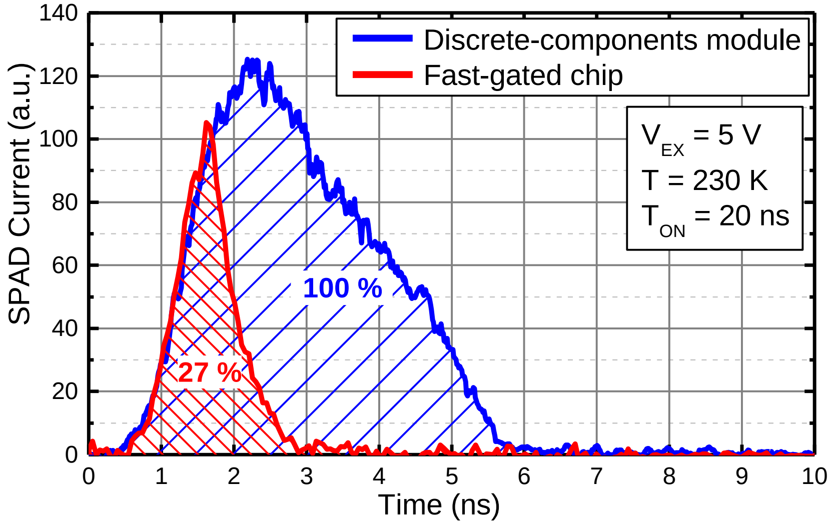
Short gate (**300 ps**)

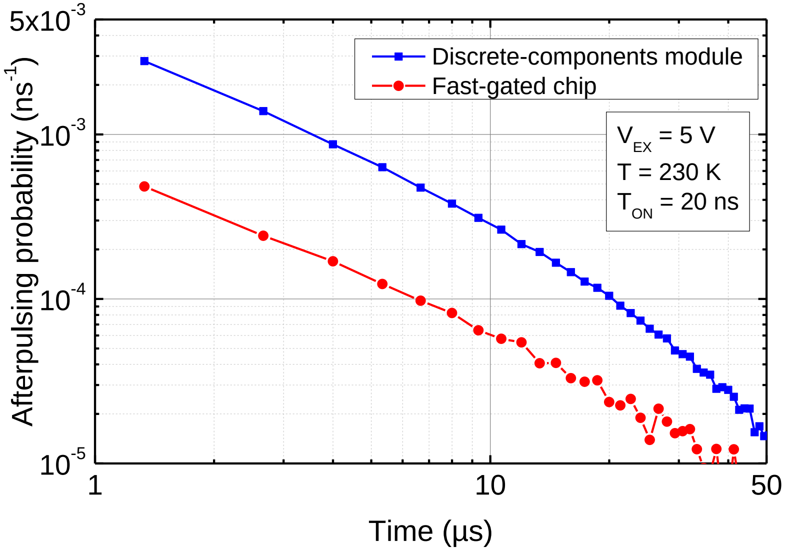


Integrated fast-gated active quenching circuit

Effective reduction of avalanche charge

→ **lower afterpulsing even with long gate**

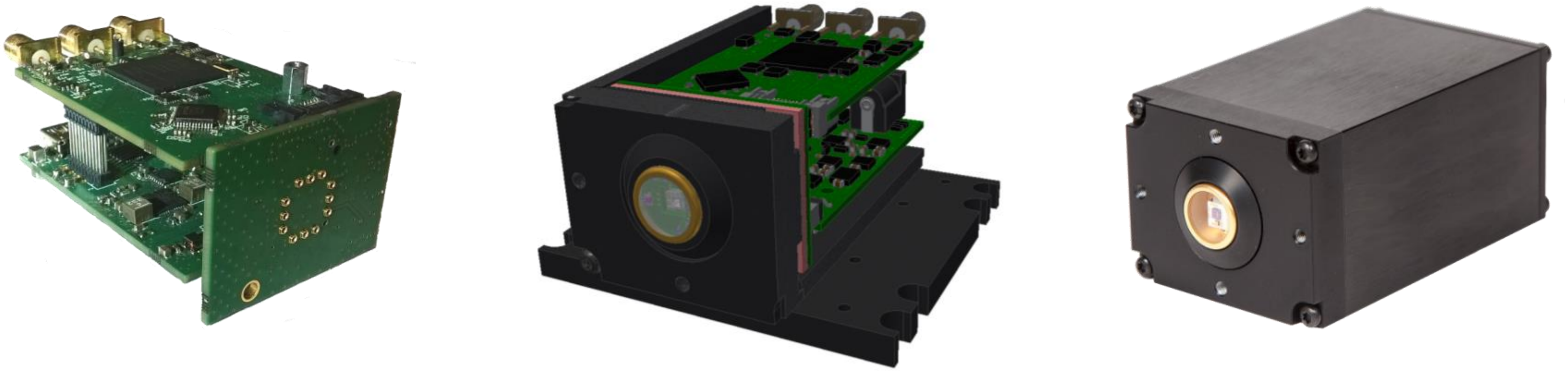




5X reduction of afterpulsing
with long gate

Compact module built around integrated fast-gated chip

Compact module based on integrated circuit & InGaAs/InP SPAD



Maximum gate repetition rate	250 MHz
Hold-off time	0.003 ÷ 1300 µs
Gate width	0.3 ÷ 1000 ns
SPAD temperature	205 ÷ 290 K
Size	40 x 50 x 70 mm^3

Conclusions

- **InGaAs/InP SPAD:**
  PoliMi experimental results (@ V_{EX} = 5 V):
  - Low DCR (~ 10^3 at 225 K)
  - Good detection efficiency (30 % @ 1550 nm)
  - Moderately low afterpulsing
  - Low timing jitter (FWHM < 90 ps)
- **Circuits for high-count-rate InGaAs/InP SPAD system:**
  - SPAD with integrated quenching resistor
  - GHz sinusoidal gate (SPAD-dummy balancing approach)
    - Very low afterpulsing (< 1.5%)
    - High count rate (> 600 Mcount/s)
  - Compact modules based on fast-gating ASIC
    - Trade-off between standard modules and GHz gating)

This work was funded by the projects **EMPIR 14IND05 MIQC2 (H2020)** and **DARPA REVEAL**:

Waiting for you at Single Photon Workshop 2019 in Milano!