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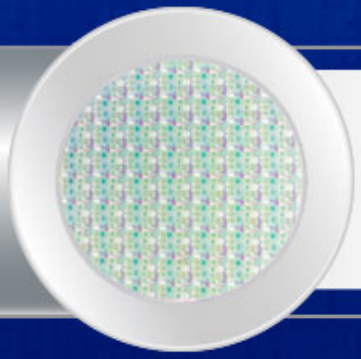
IC Manufacturing for a Smart World



CMOS 0.18μm SPAD

TowerJazz February, 2018
Dr. Amos Fenigstein

Outline

- CMOS SPAD – motivation
- Two ended vs. Single Ended SPAD (bulk isolated)
- **P+/N two ended SPAD and its optimization**
- **Application of P+/N two ended SPAD**
- **NIR enhanced N+/P SPAD scheme**
- **QE optimization device and optics**
- **SiPM and its density optimization**
- **Source Follower as an amplifier**

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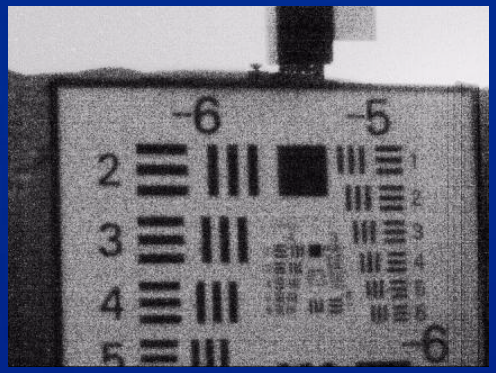
Single Photon Detection

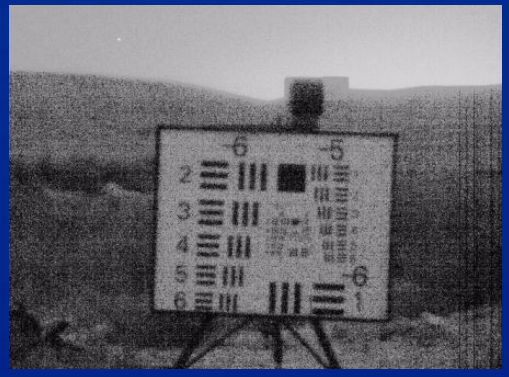
- OOPs – the wrong presentation, this is 4T pinned photo diode pixel – 1e noise, very high sensitivity
- So, why SPAD – People say, it's all about timing …

Images at starry night – 0.6 mili-Lux!!!!

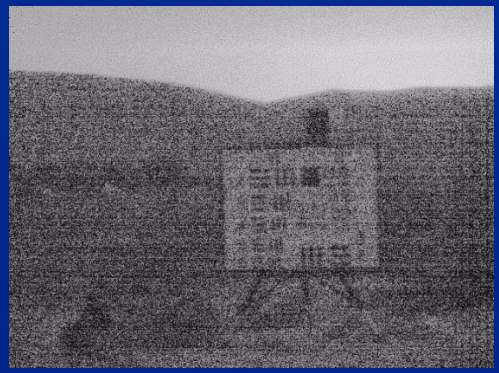
(10 micron pixels)



5 meters



10 meters



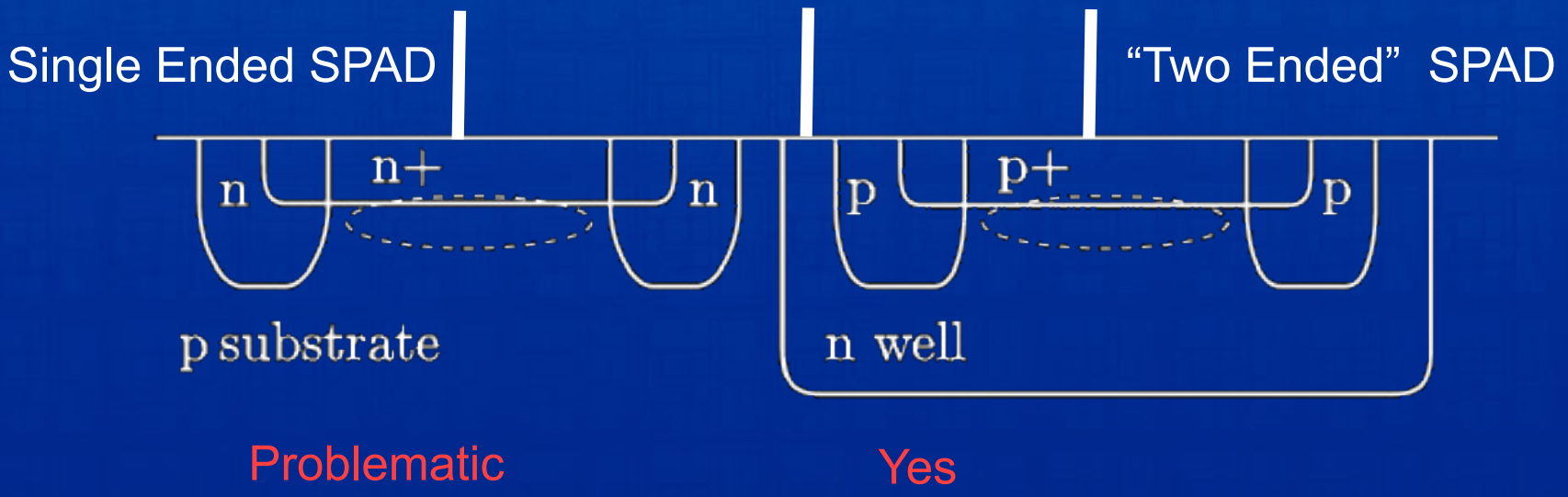
15 meters

CMOS – SPAD, SPAD in CMOS/CIS Process

- Stand alone SPAD can be well optimized
  - using minimal mask count
  - any desirable operating voltage
  - High performance
- SPAD embedded in CMOS/CIS process
  - Somewhat inferior for the features above, However:
  - Allows monolithic on chip quenching, readout, and other circuitry
  - Enable CIS optimized pixel on same chip with SPADs

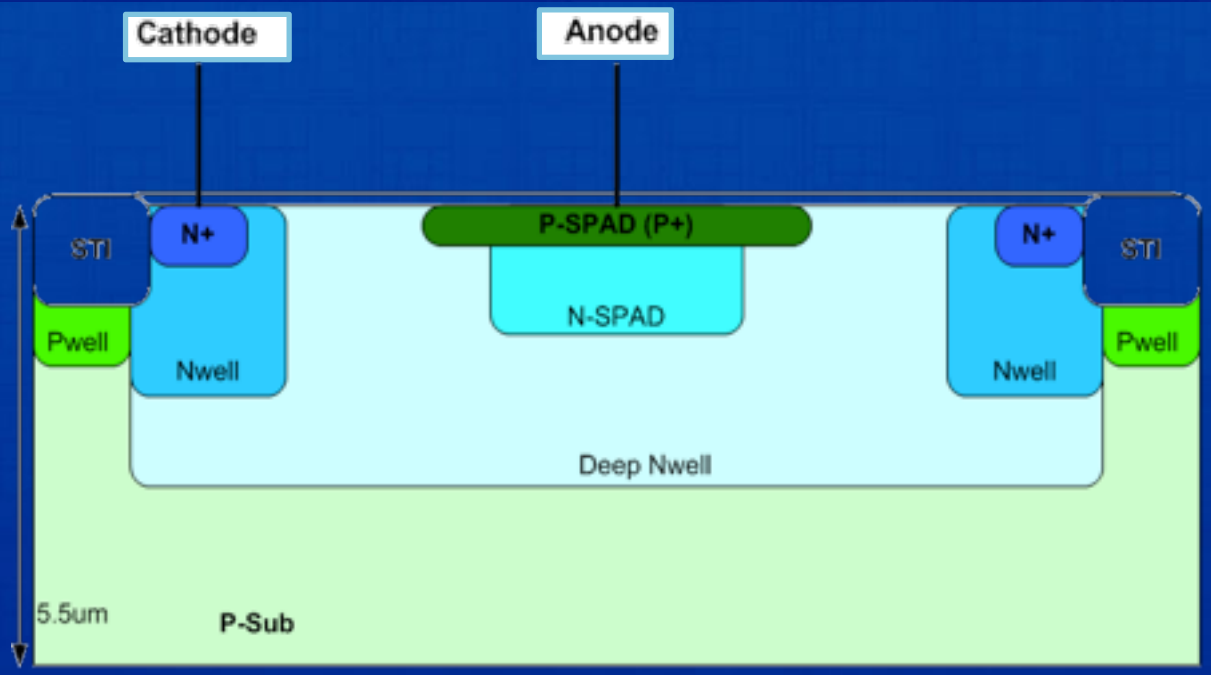
Single Ended SPAD (bulk Isolation) vs. Two Ended

- Can one add low voltage circuitry in series to the SPAD?

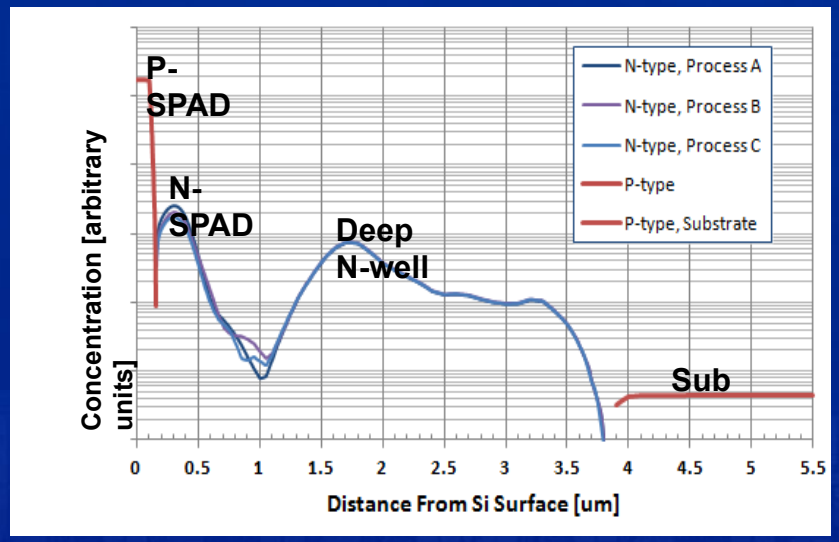


- Single Ended SPAD can have better NIR response but it's harder to use fancy quenching

P+/N “Two Ended” SPAD optimization

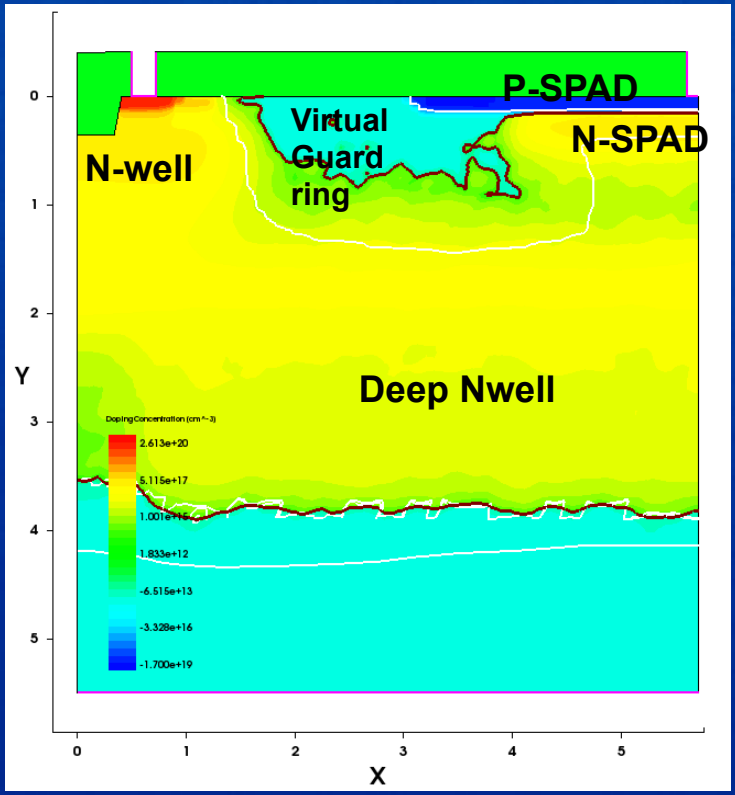


Schematic cross section of the SPAD

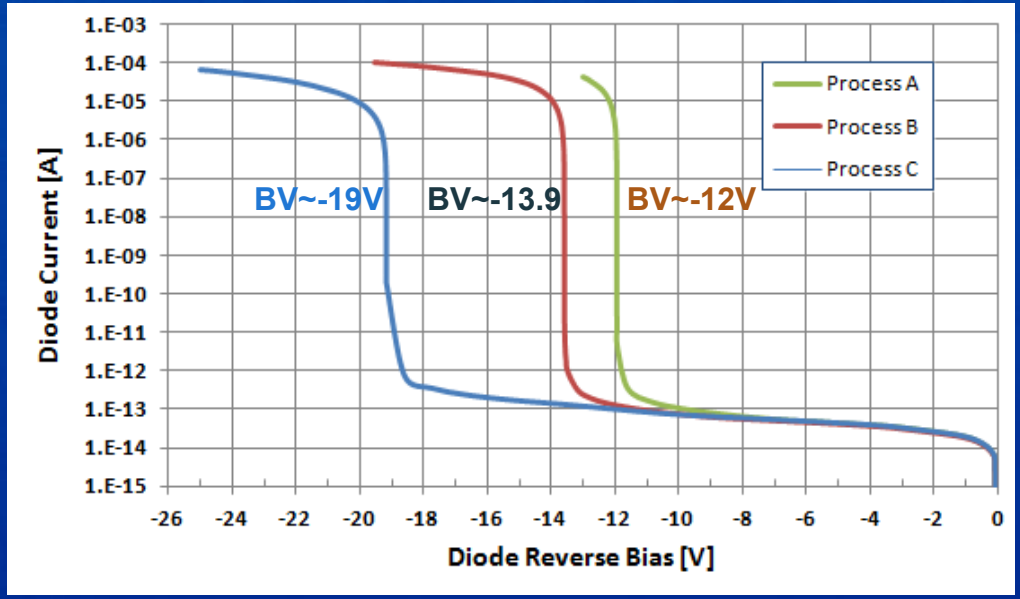


Simulated Doping Concentration on a vertical cut line

TCAD Process Simulation Results-



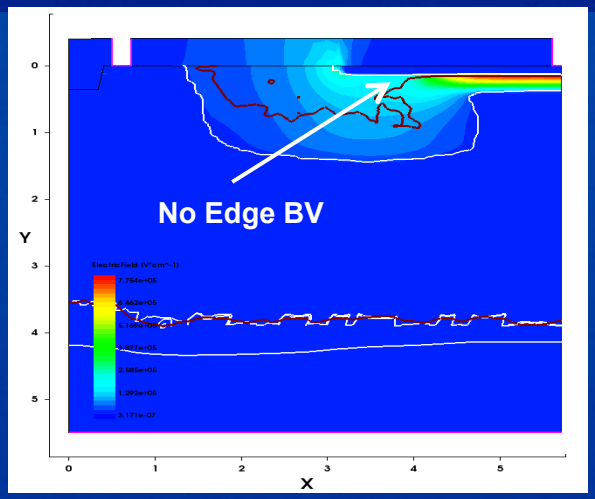
Simulated half SPAD structure (Doping Concentration)



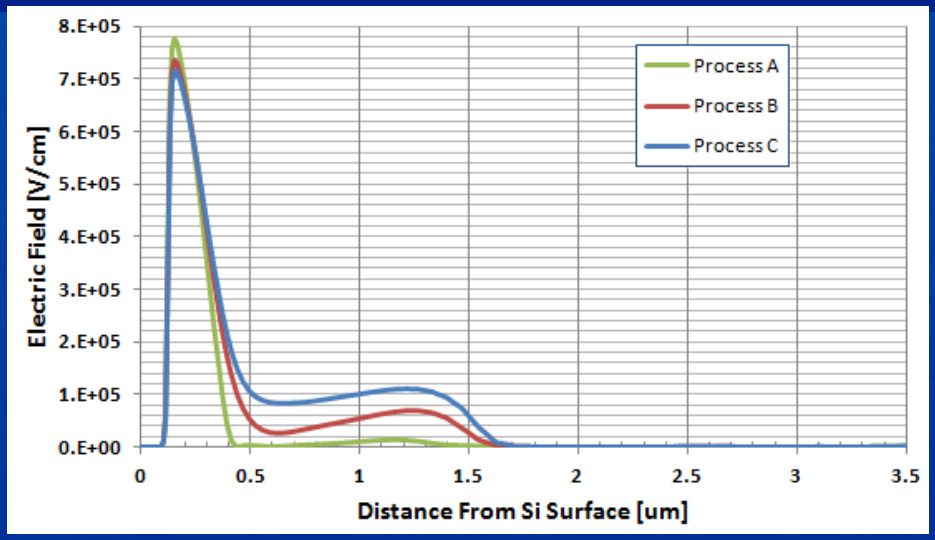
Simulated SPAD IV curve

- Avoiding Early Edge Breakdown by Virtual Guard ring

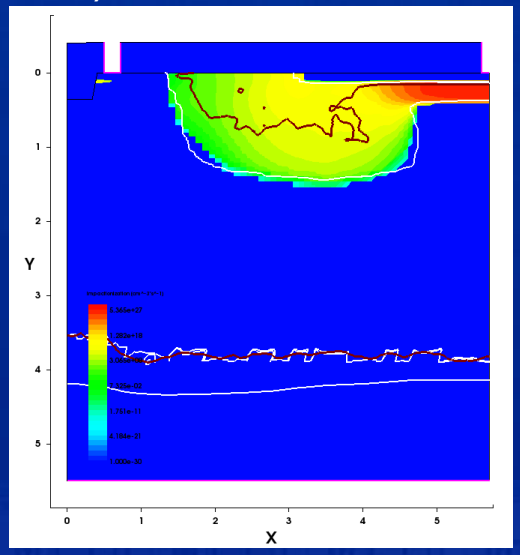
Electrical Fields and Impact Ionization Rate



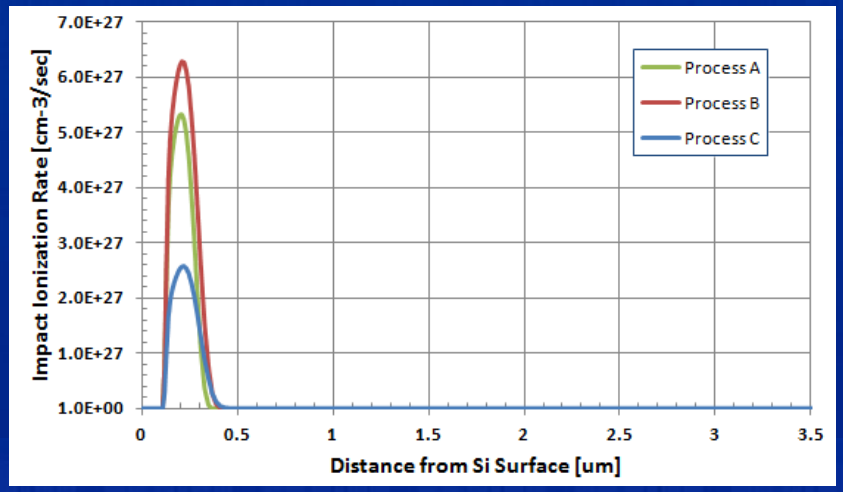
Simulated electrical fields at -14V on the Anode (process A)



Simulated electrical fields on the vertical cut line (A, -24V, B, -18V, C, -14V on the Anode)



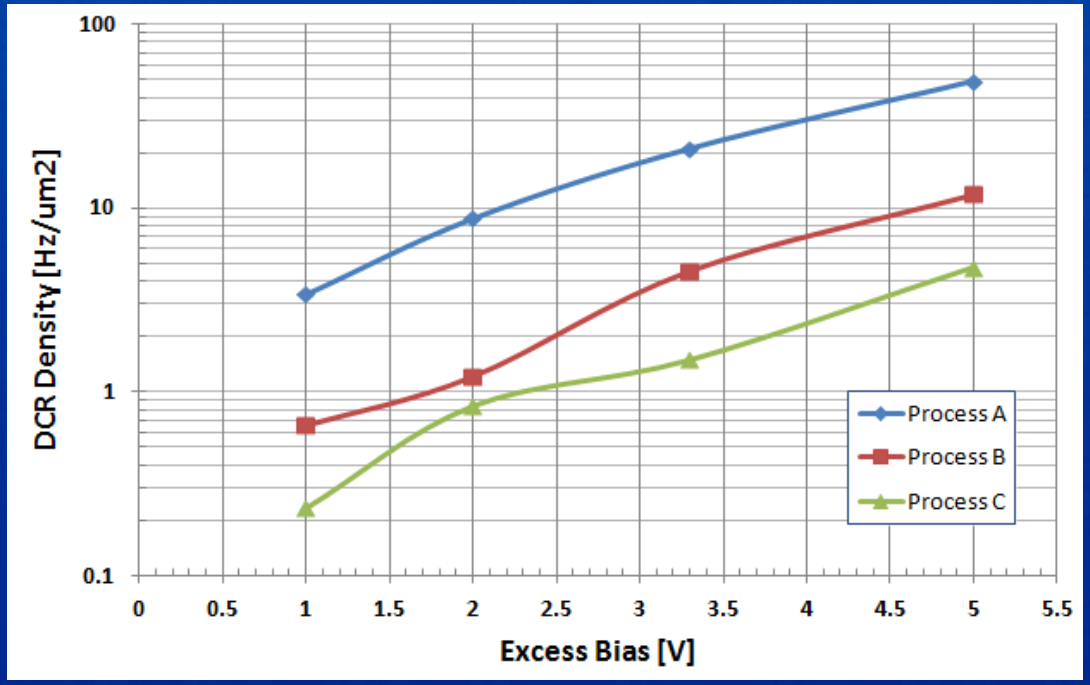
Simulated Impact Ionization rate at -14V on the Anode (process A)



Simulated Impact Ionization rate on the vertical cut line (A, -24V, B, -18V, C, -14V on the Anode)

DCR vs. Excess Bias (room temperature)

- *DCR is exponential in excess voltage*
- *Inversely depends on breakdown voltage*



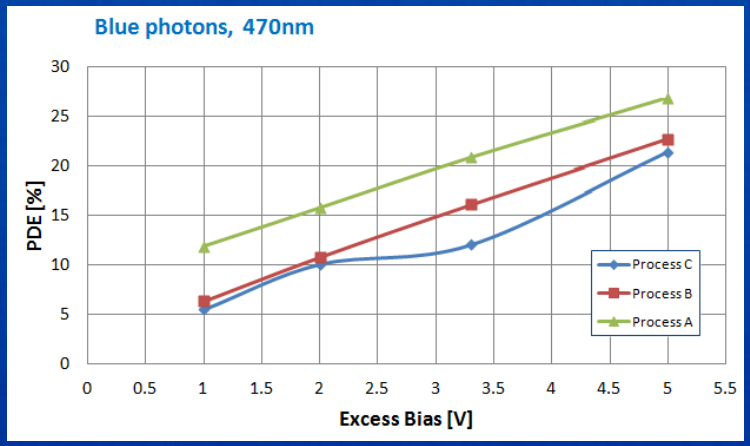
Measured DCR density vs. Excess bias at room temperature

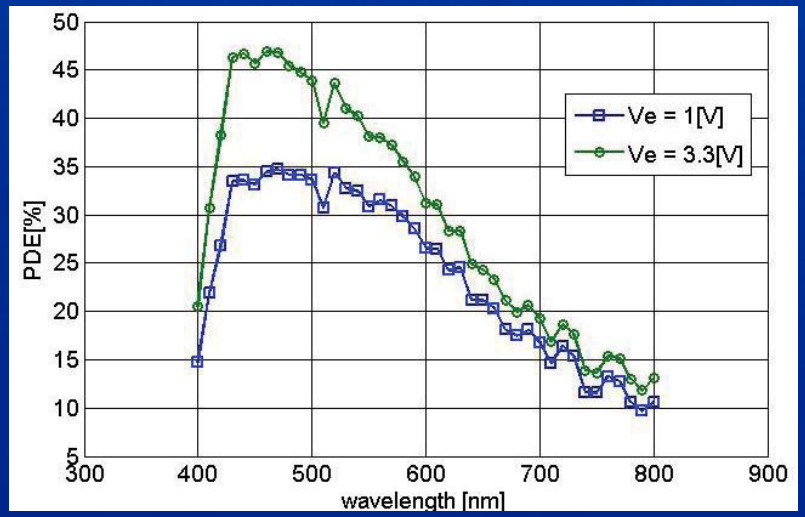
Process split	BV [V]	DCR Density [Hz/ um^2], RT
A	-12.41	21
B	-14.54	4.6
C	-20.13	1.5

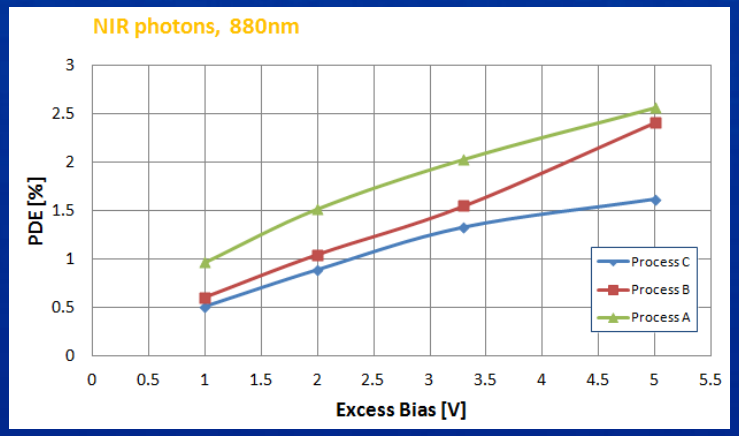
At 3.3V excess bias:

Photon Detection Efficiency Spectrum and Excess Bias dependency

- PDE linearly dependant on excess voltage
- Low PDE for NIR



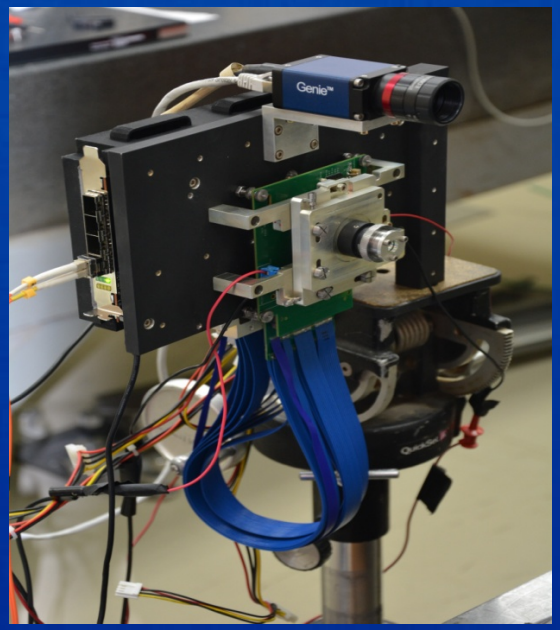




Measured PDE vs. Excess bias (passive quenching circuit)

Process split	BV [V]	PDE [%] Blue 470nm	PDE [%] Green 530nm	PDE [%] Red 660nm	PDE [%] NIR 880nm
A	-12.41	20.93	15.93	7.3	2.03
B	-14.54	16.13	12.69	6.63	1.55
C	-20.13	12.07	9.09	6.91	1.33

P+/N SPAD Application – Gunshot Detection



Muzzle flash emits photons at λ=766[nm]

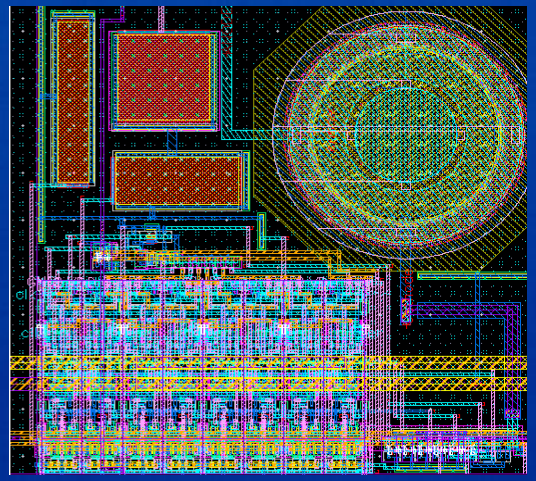
System Description

1) Commercial high resolution CMOS Imager for the spatial SPAD synchronization
2) FPGA commercial carrier board used for operating the SPAD image sensor and signal processing of its output data
3) A CMOS SPAD image sensor placed on a mezzanine board
4) Specially-designed opto-mechanical system for the SPAD image sensor.
5) Narrow-band optical filter

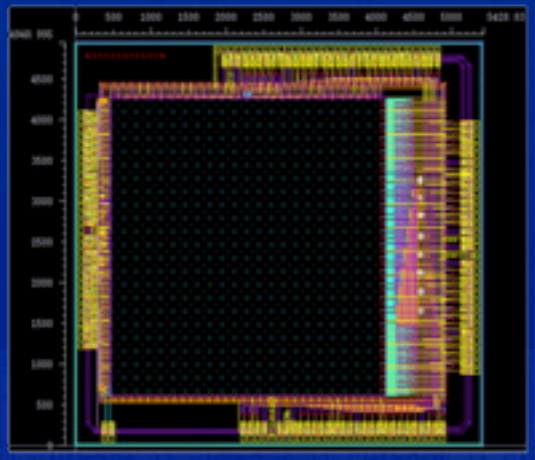
- Application works in visible light
- 2nd Generation can be monolithic since TowerJazz can join CIS pinned photodiode and SPAD within the same process

Device and Pixel Architecture

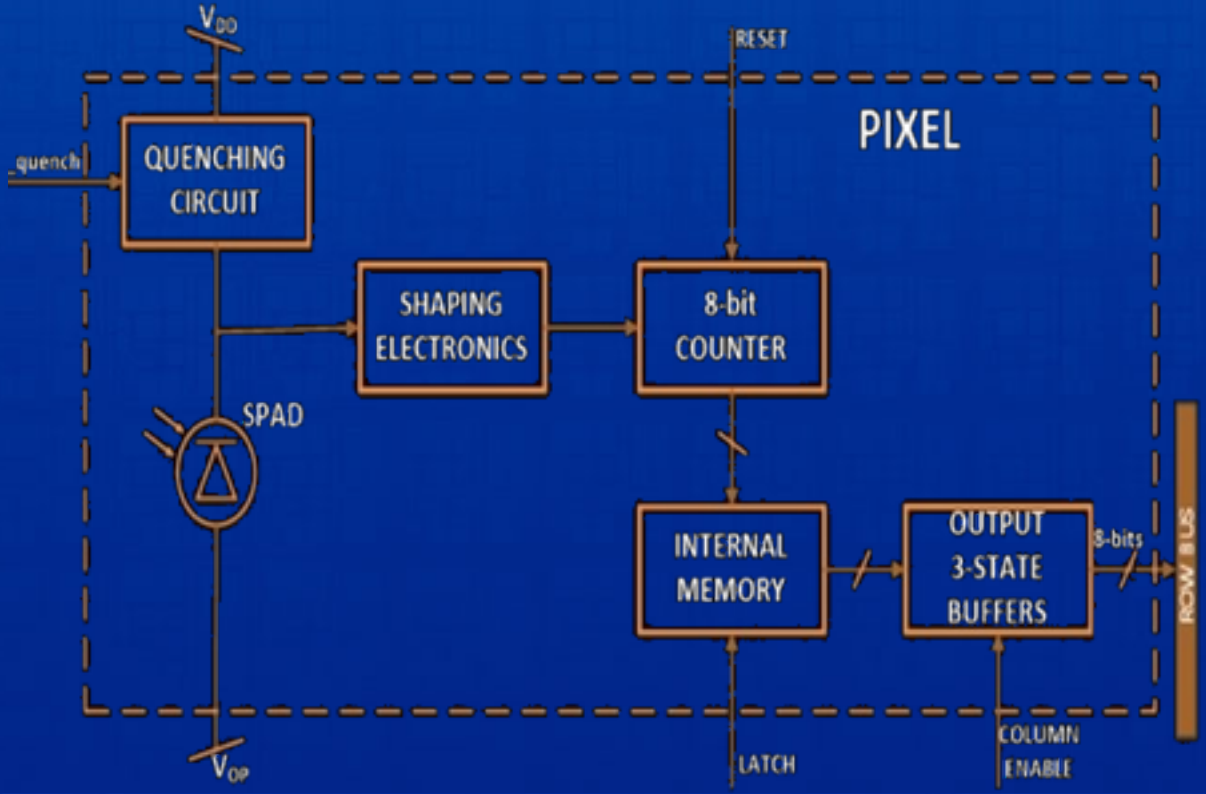
SPAD pixel Layout



64x64 SPAD Imager Layout

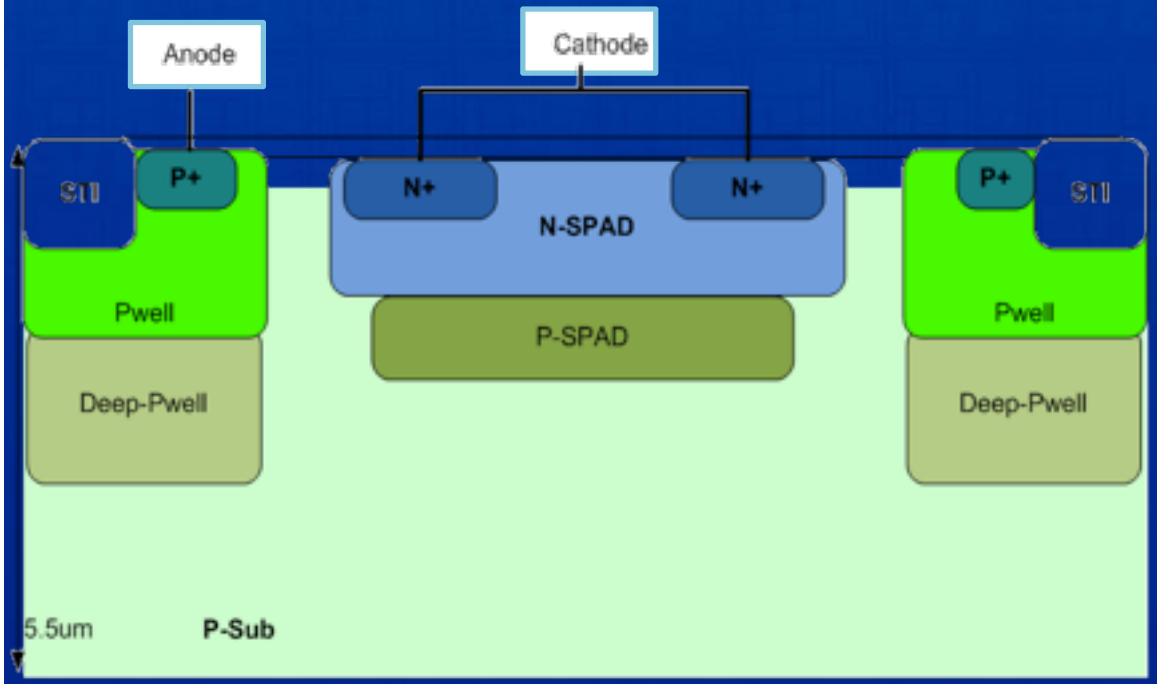


SPAD pixel Block Diagram

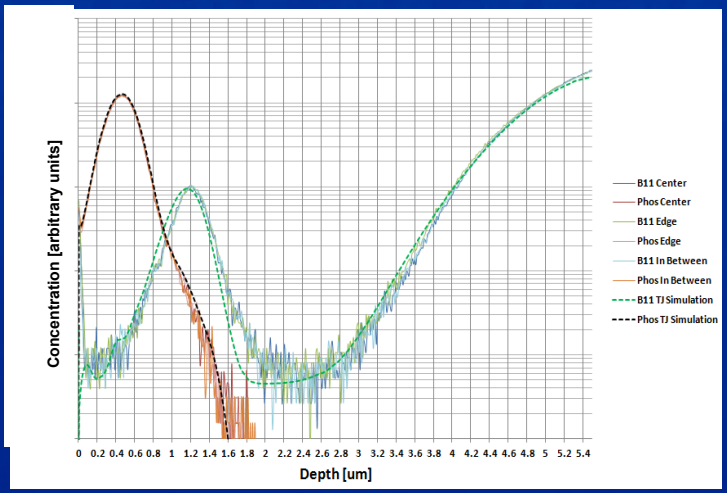


N+/P Single Ended SPAD

- Implemented on 5.5μm epi – 30Ωcm
- Note bulk to epi doping gradient



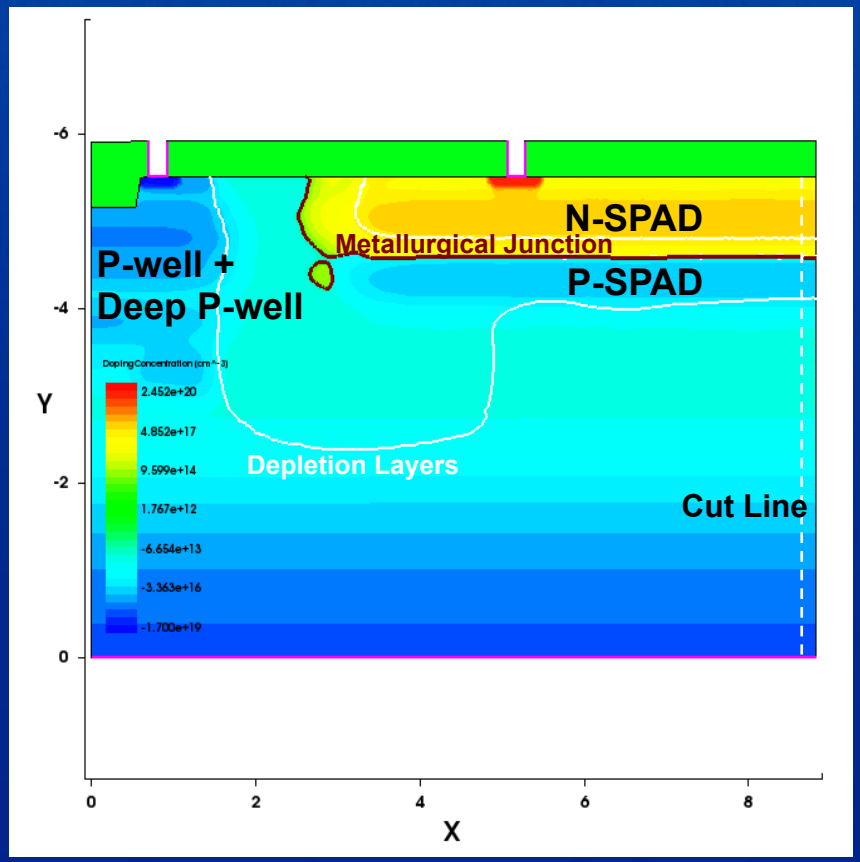
Schematic cross section of the SPAD and isolation P-wells



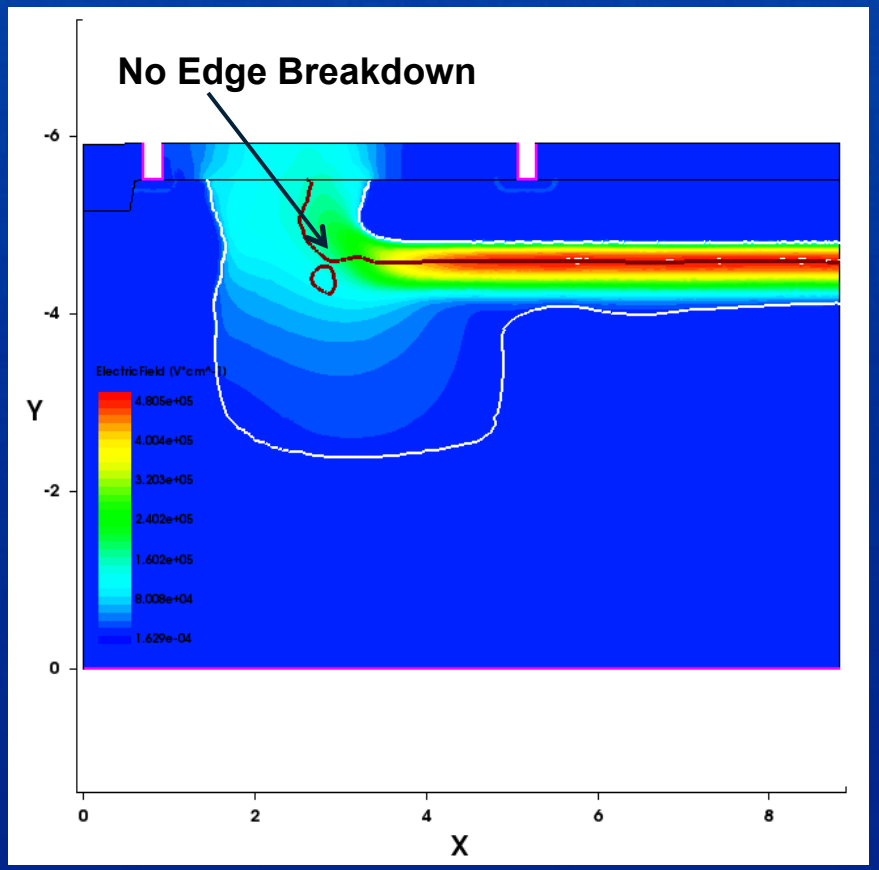
SPAD SIMS Vertical Profiles

TCAD Process Simulations Results-

- Low fields on diode edge – avoiding edge breakdown



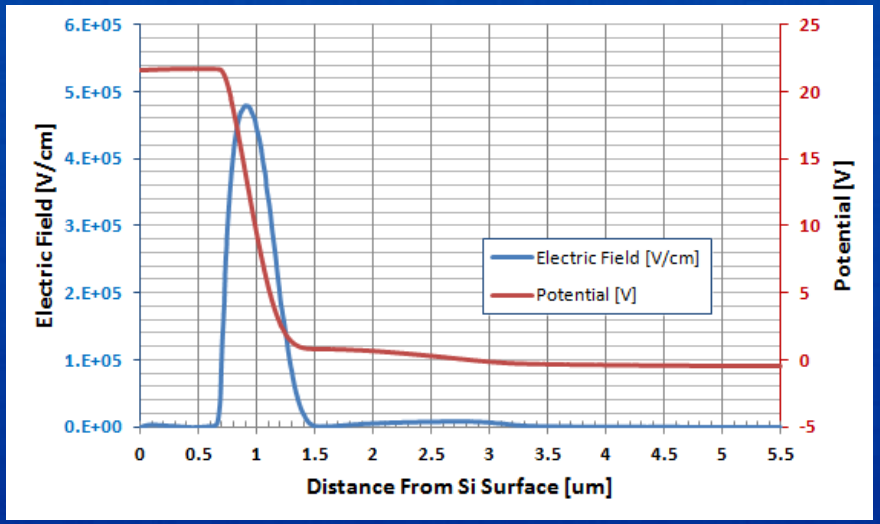
Simulated half SPAD structure (Doping Concentration)



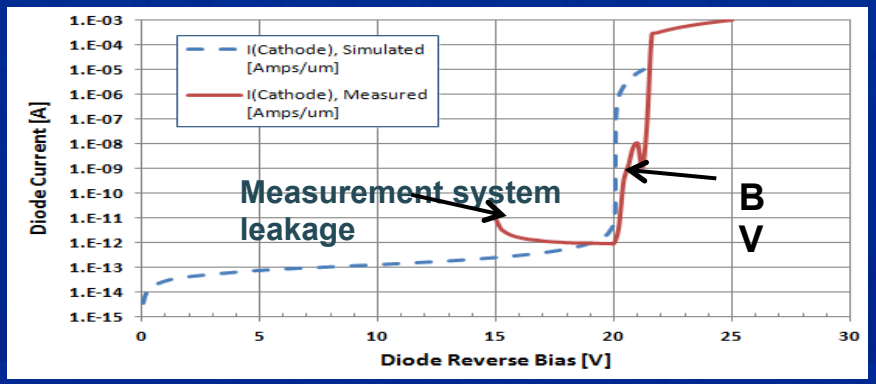
Simulated electrical fields at 21V on the Cathode

Electrical Fields (magnitude)- simulated-

- Electrical field is small out of multiplication region
- Good agreement of IV curve between simulations and measurements



Simulated electrical fields and potential on the vertical cut line (21V on the Cathode)

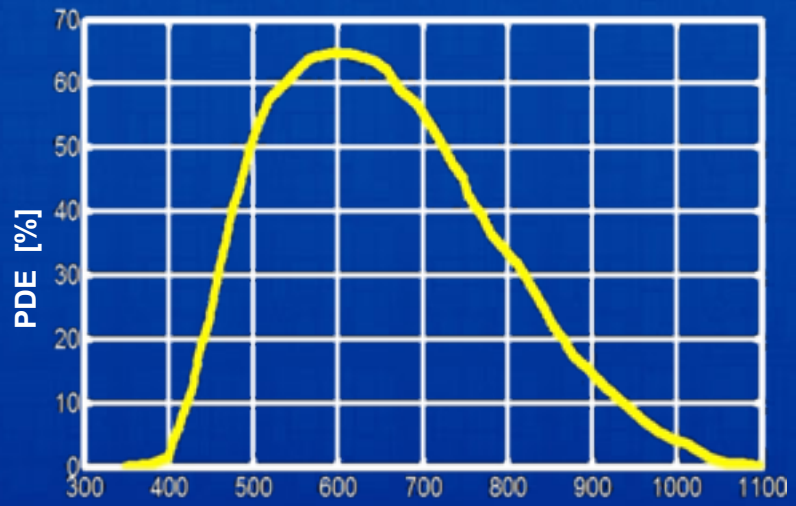


Simulated and Measured SPAD IV curve

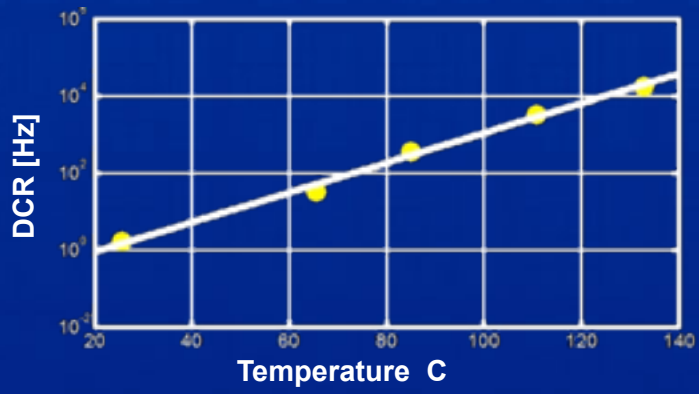
Measured Performance parameters

- PDE at 905nm 3.2% averaged on cell pitch
- Low DCR
- Acceptable DCR even for 100C!

Meas. by Niclass 2015



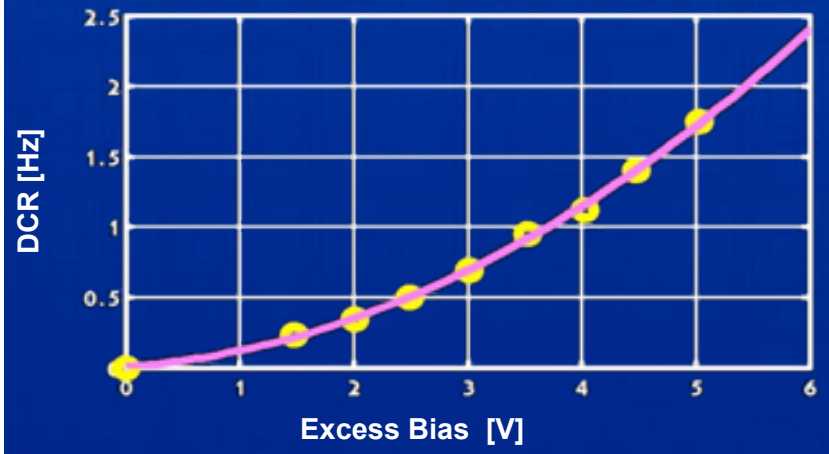
Normalized Photon Detection Efficiency at 5V Excess Bias



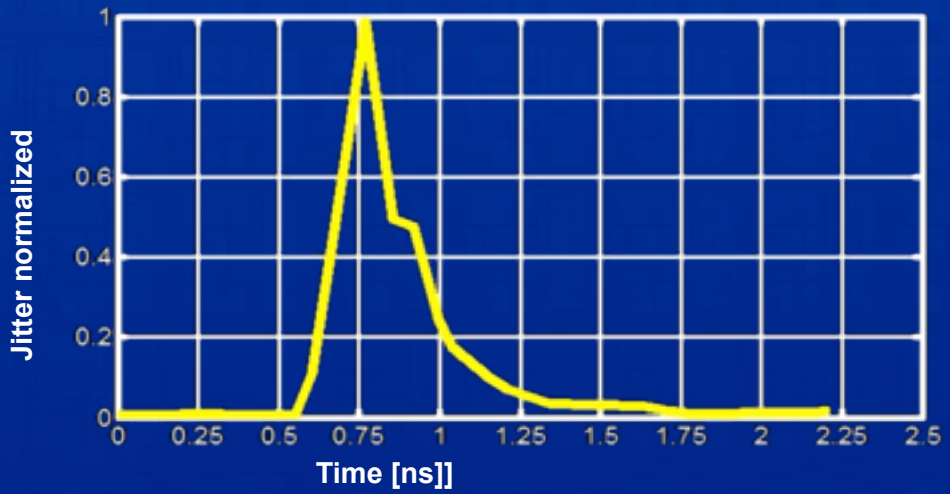
Measured mean DCR density vs. temperature at 5V Excess Bias

Measured Performance parameters (Cont.)

- DCR is weakly dependant on excess voltage
- Jitter is small and suitable to automotive demands



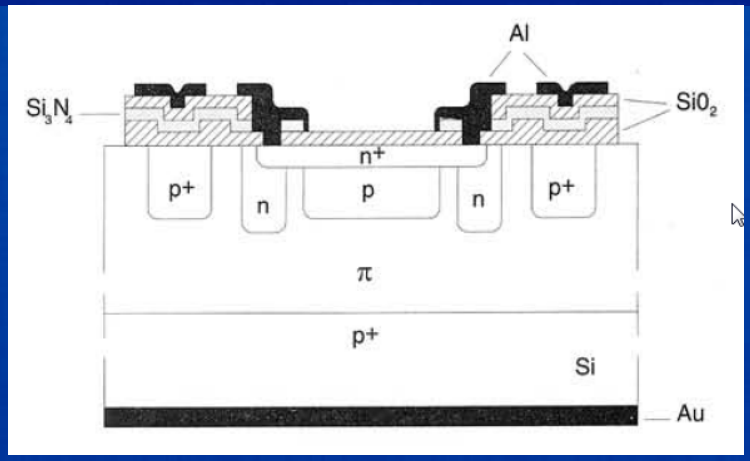
Measured mean DCR density vs. Excess Bias , room temperature



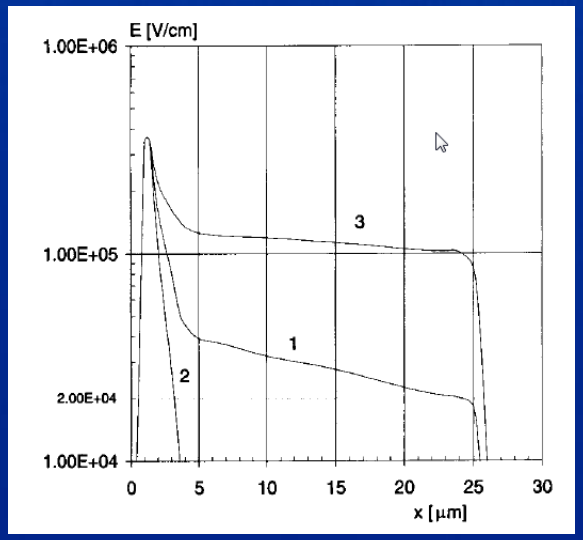
timing response @ 5V Excess Bias to a 635nm laser diode emitting 100 psec overall timing jitter of ~160 psec FWHM.

SPAD with depleted low doped region

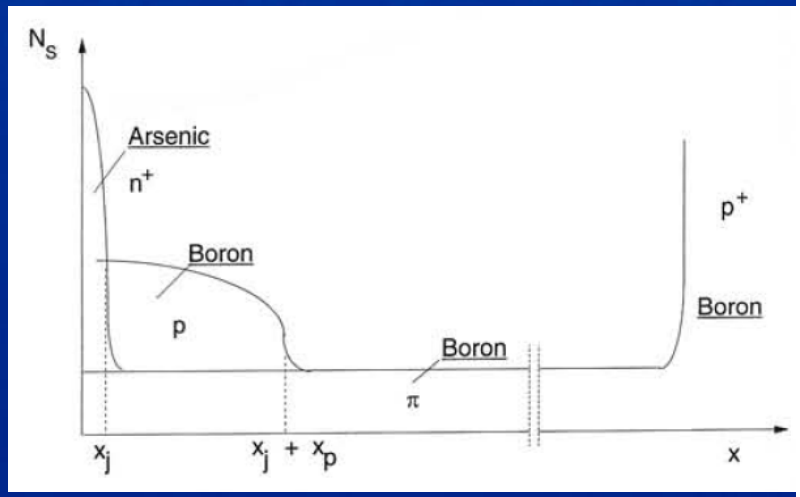
- Reach-Through SPAD
- Quit old concept
- From: Opto-Electr Rev. 5 no. 2 1997



Cross Section



Field Profile



Doping Profile

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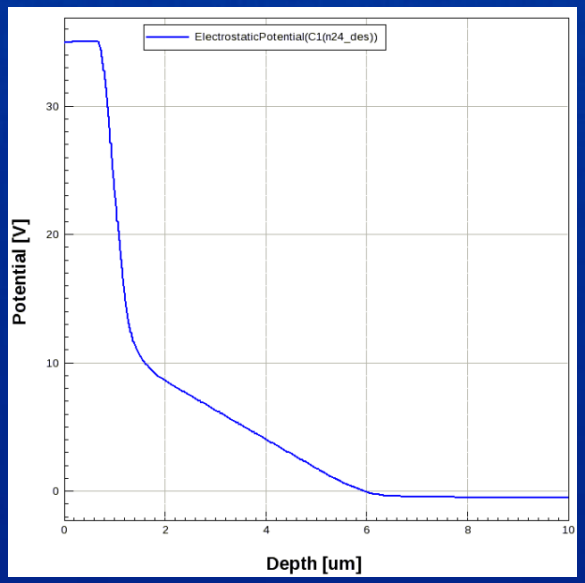
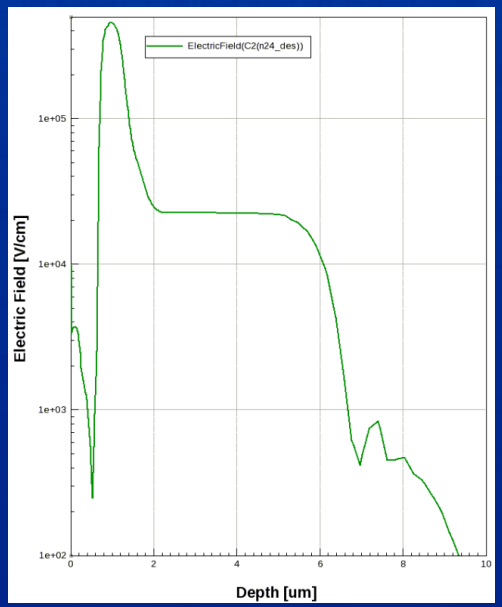
Fully depleted 9μm High Res SPAD Simulations

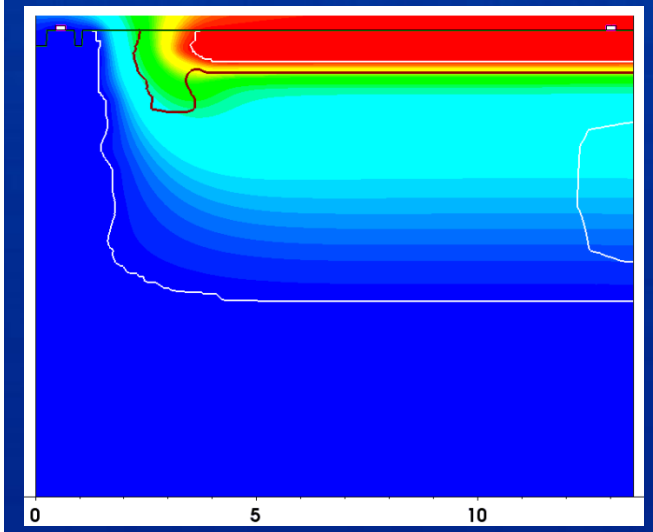
- Similar SPAD structure – starting material and implants change
- Breakdown - simulated 36V measured 38V
- Significant field deep in the epi -
- Average QE at 905nm enhanced from 3.2% to 4.6%



Simulated Potential vs. depth



Simulated Field vs. depth



Edge Optimization

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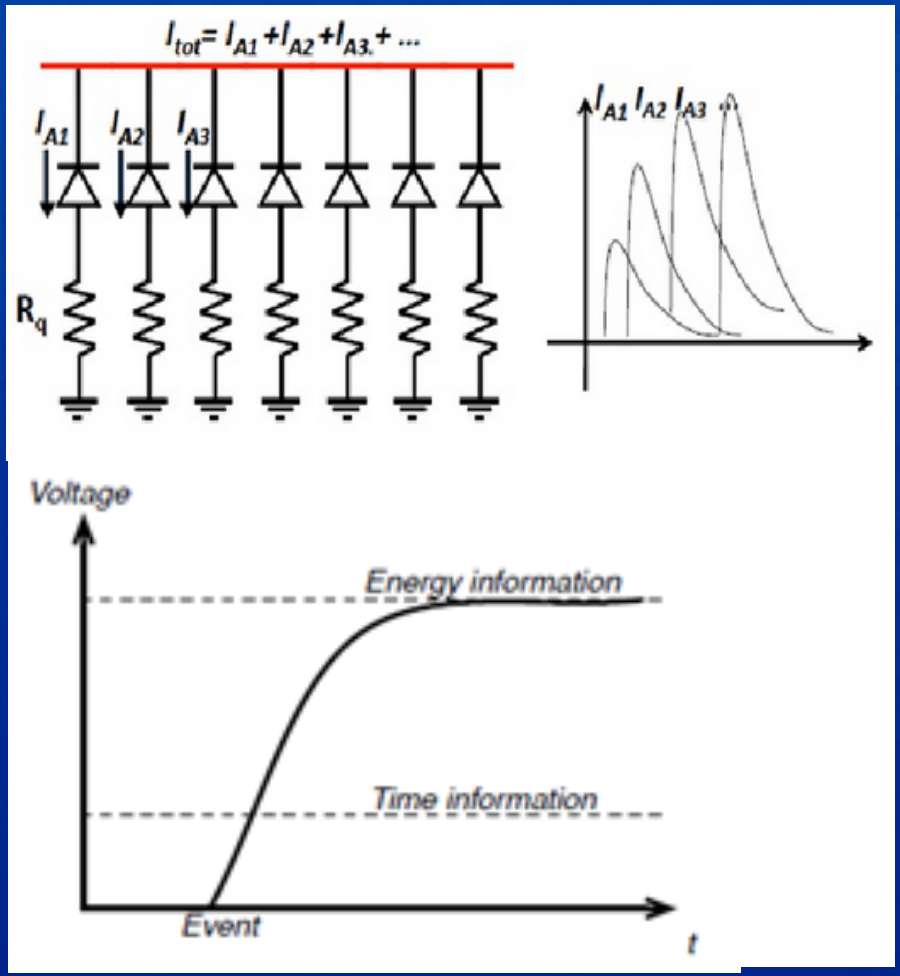
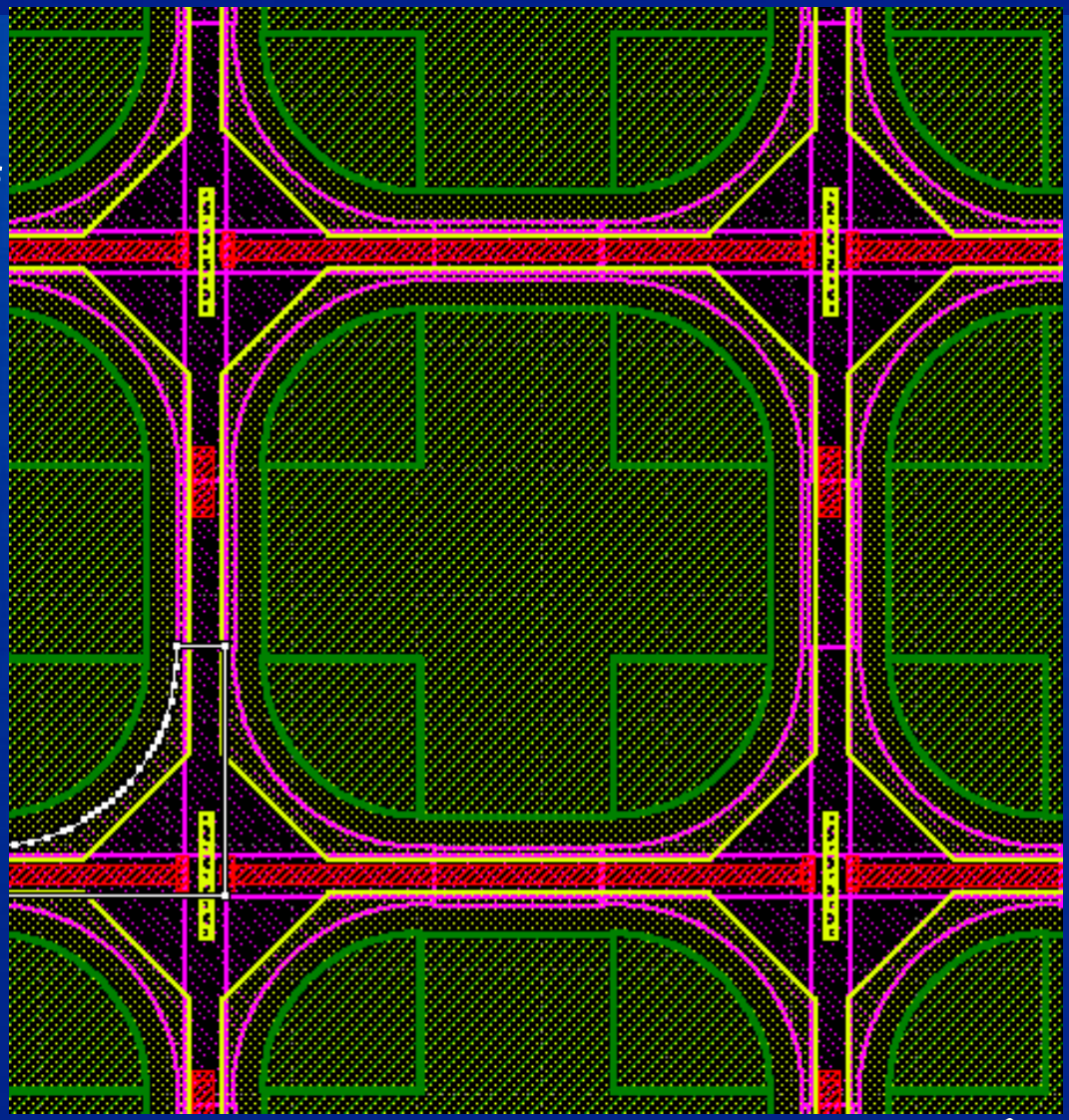
SiPM – Silicon Photo Multiplier

- Array of SPADs
- Hard wired or capacitively coupled SPADS
- Benefits:
  - Timing + number of photons
- Cons
  - Slower rise time
  - Sensitive to "screaming" SPADs
  - More prone to X-talk



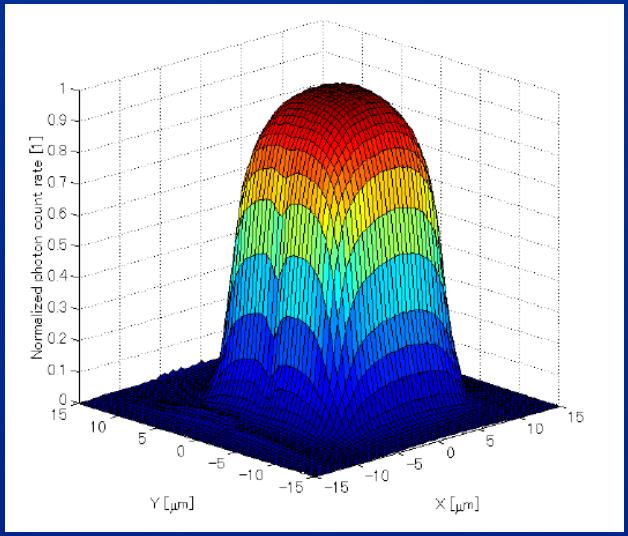
Optimization of Layout Of an SiPM

- Guard Ring is minimized
- Rounded corners instead of circles
- High Resistivity poly resistors 10kΩ/
- Fine optimization of cell size
  - Fill Factor
  - Microlenses
  - Capacitance
- No evidence for screaming SPADs nor for cross talk

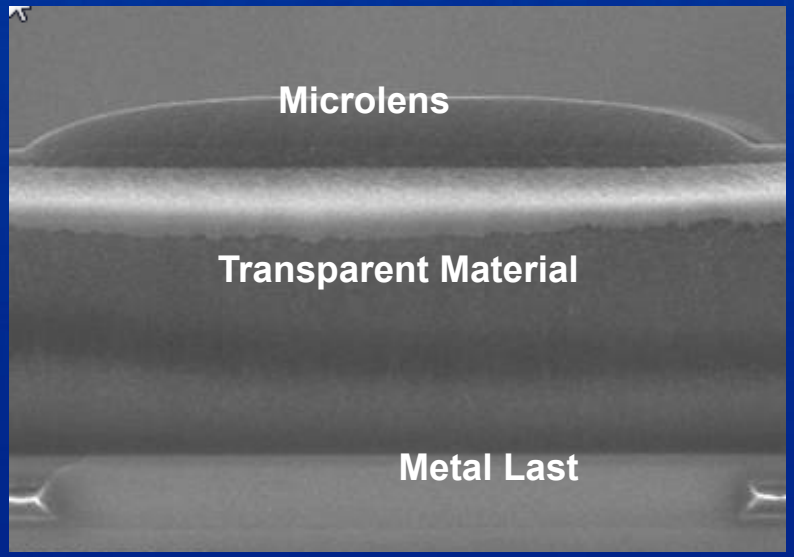


Elevated Microlenses Optics

- SPAD suffers from low fill factor
- SPAD diodes pitch is relatively large – hard to make effective microlenses
- For long focal length lenses should be put high above the B/E
- Tower developed large elevated microlenses
- With elevated microlenses we expect effective QE of about 7%
- Targeting effective QE of 10% at 905nm after further device optimization



Normalized PDE mapping of SPAD area, Niclass 2014



Elevated "Big" Microlenses

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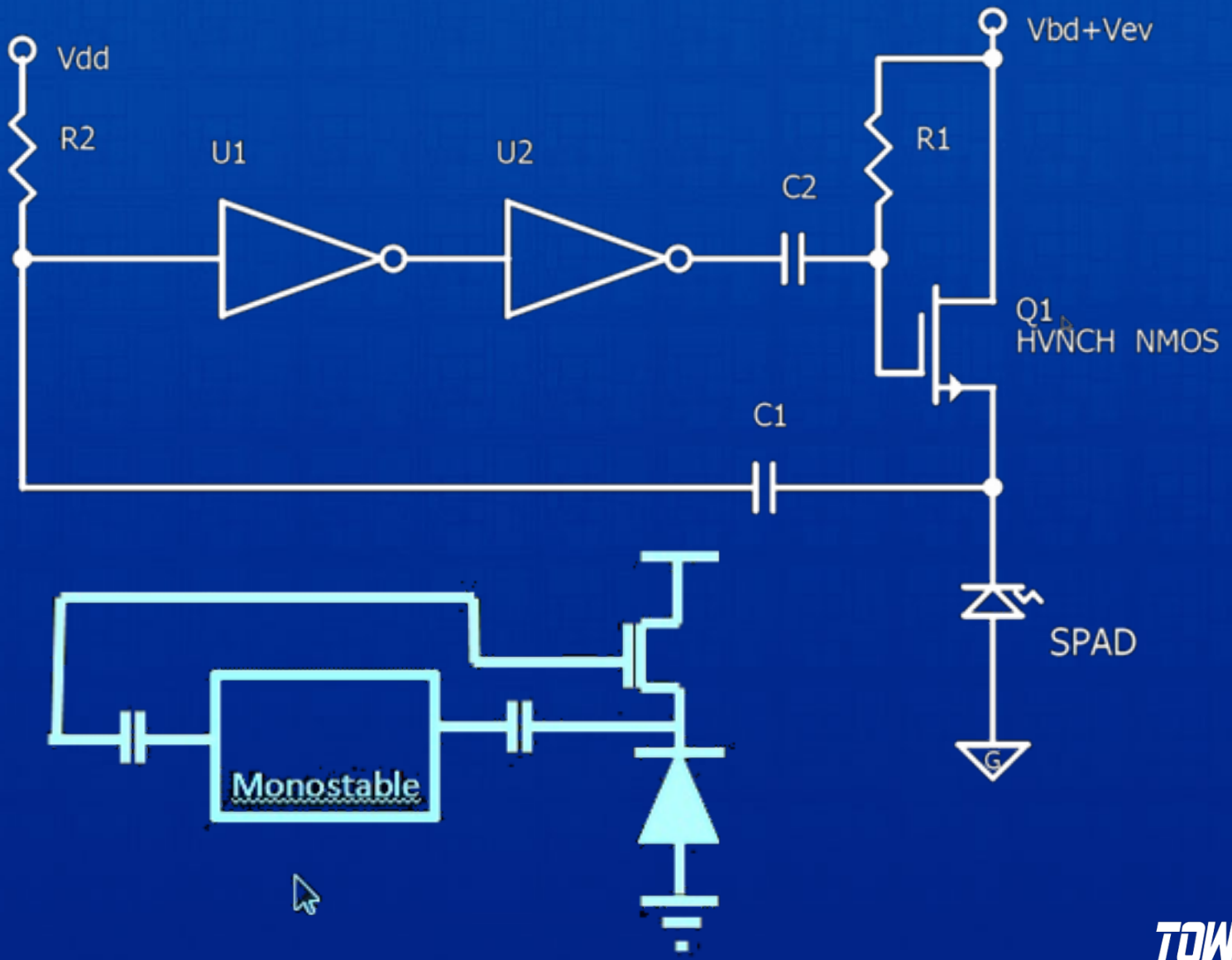
Dead time and Active Quenching

- SPAD capacitance is between 10fF-30fF depends on layout
- RC time with 250kΩ resistor is below 10ns, which is probably good enough for Automotive applications
- We are working on “tricky” quenching circuits that can improve by shortening and better defining the dead time

Capacitive Coupled Monostable Recovery Circuit



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Summary

- CMOS-SPAD was developed on platform supporting 0.18um CMOS (1.8V/3.3V or 1.8V/ 5.0V) and CIS state of the art pixels
- “Single Ended” and “Two Ended” version were developed
- Optimization was mostly focused on effective PDE in the NIR – Layout, Starting Material , Implant Scheme, and pixel optics
- Some special process modules were developed i.e. super high resistor, large microlenses and microlense elevation

References

- T. Leitner, A. Fenigstein, R. Turchetta, R. Coath, S. Chick, G. Visokolov, V. Savuskan, M. Javitt, L. G., I. Brouk, S. Bar-Lev, and Y. Nemirovsky “Measurements and Simulations of Low Dark Count Rate Single Photon Avalanche Diode Device in a Low Voltage 180-nm CMOS Image Sensor Technology” IEEE TRANSACTIONS ON E. DEVICES, Vol. 60, NO. 6, June 2013
- C. Niclass, H. Matsubara, M. Soga, M. Ohta, M. Ogawa, and T. YamashitaA , “NIR-Sensitivity-Enhanced Single-Photon Avalanche Diode in 0.18μm CMOS” *Sensors* **2016**, *16*(4),
- I Wegrzecka, M. Wegrzecki “Silicon Photodectors – the State of the Art. Opt-Electr. Rev., 5, no 2, 1197
- Y. Nemirovsky, V. Suvuskan, S. Bar-Lev, I. Brouk, G. Visokolov, A. Fenigstein, and T. Leitner, “Device Having an Avalanche Photo Diode and a Method for Sensing Photons” US Patent US 8,779,543 B2 July 15, 2014