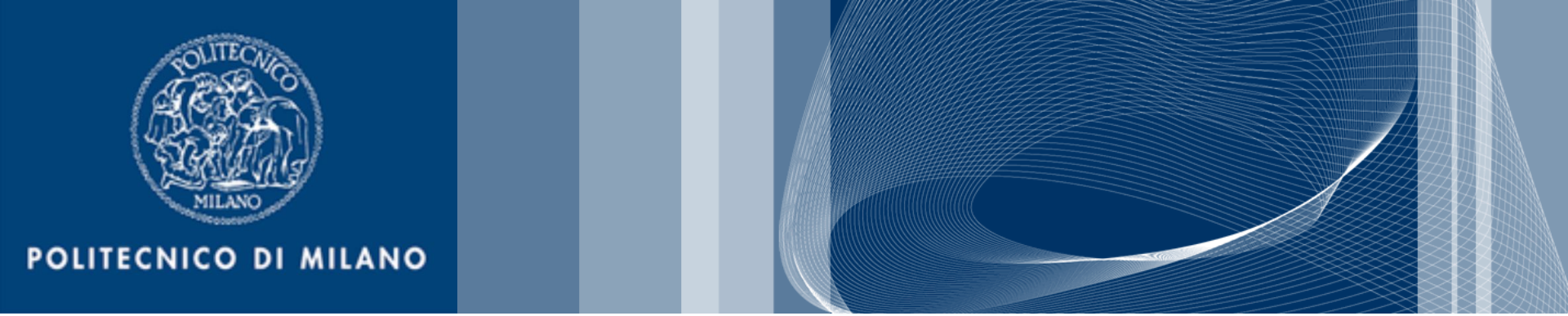

BCD SPAD imager with reconfigurable macropixels for photon counting, timing and coincidence detection

F. Villa, D. Portaluppi, M. Sanzaro, E. Conca, F. Zappa

Outline

- **Motivations and design goals**
- **SPAD imager architecture**
  - "Macropixel" design
  - TDC structure
  - 32x32 array
- **Chip characterizations**
  - TDC preliminary tests
  - SPAD characterization
- **Conclusions**

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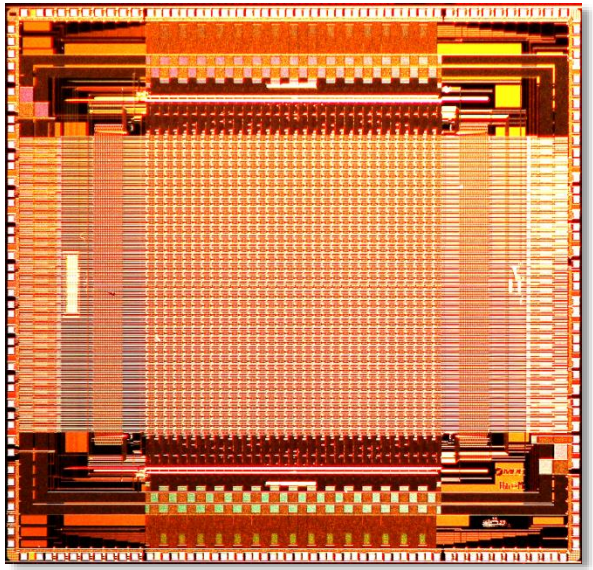
PoliMi 32×32 SPAD+TDC array chip

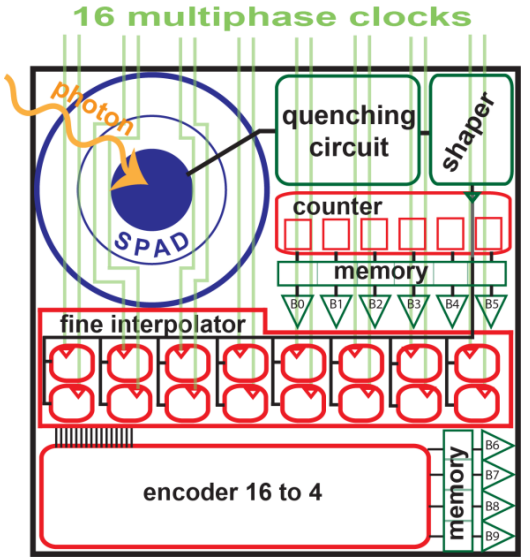
- 1024 smart pixels
- 30-µm diameter SPADs

  (3.14% fill-factor)
- 10-bit in-pixel TDCs

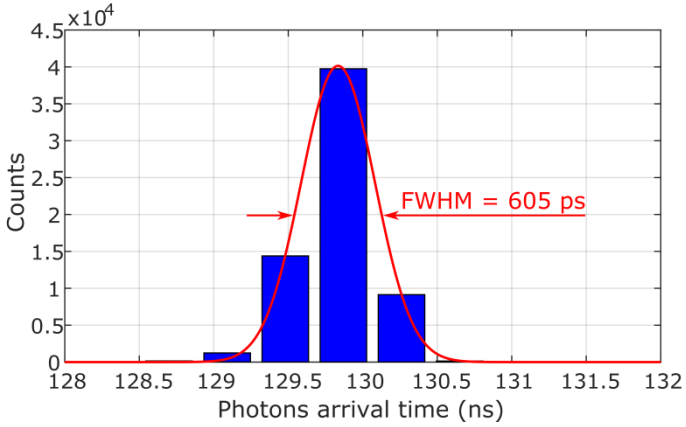
  for "photon-timing" (TOF 3D ranging, FLIM)
  312 ps LSB, 320 ns FSR
- 6-bit in-pixel counters

  for "photon-counting" (2D imaging)
- 100,000 frames/s

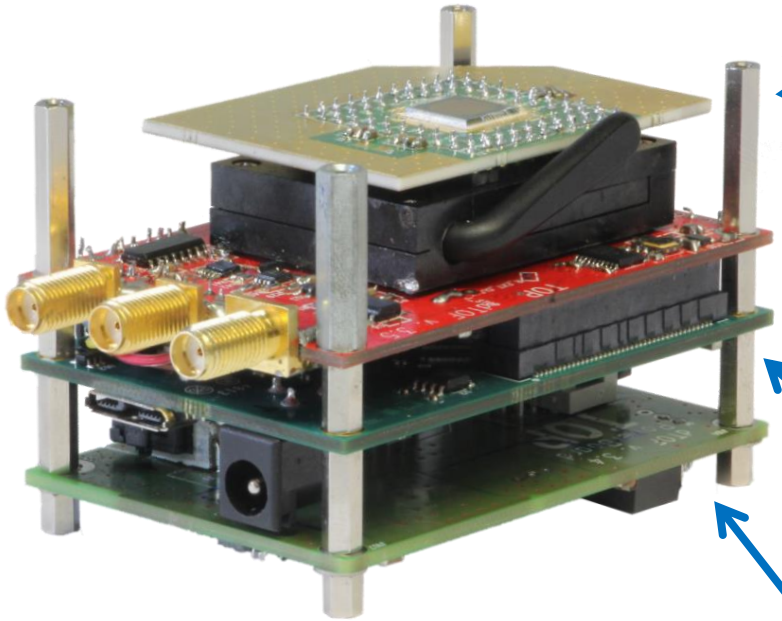




F. Villa et al., JSTQE, 2014



Single-photon camera



SPAD+TDC array chip carrier board

Analog interface board

(for interfacing the chip and handling triggering and synchronization input/output signals)

Digital processing board

(FPGA for data processing, storage, and USB3 communication link)

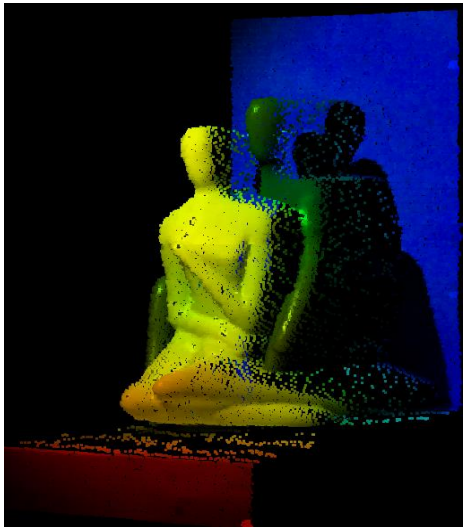
Power supply board

(power supplies generation, including user-selectable SPAD bias)

R. Lussana et al., OE, 2015

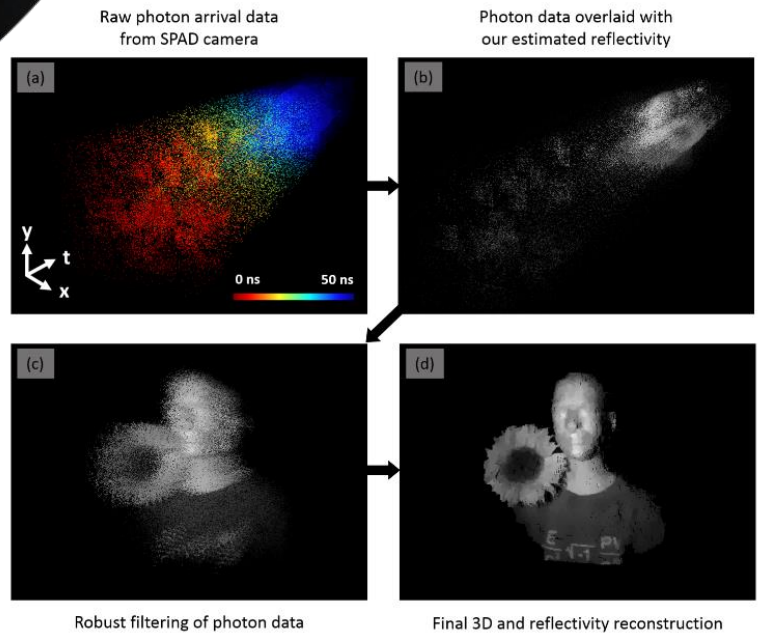
Many applications

- 3D ranging at short-distance



- Satellite 3D ranging

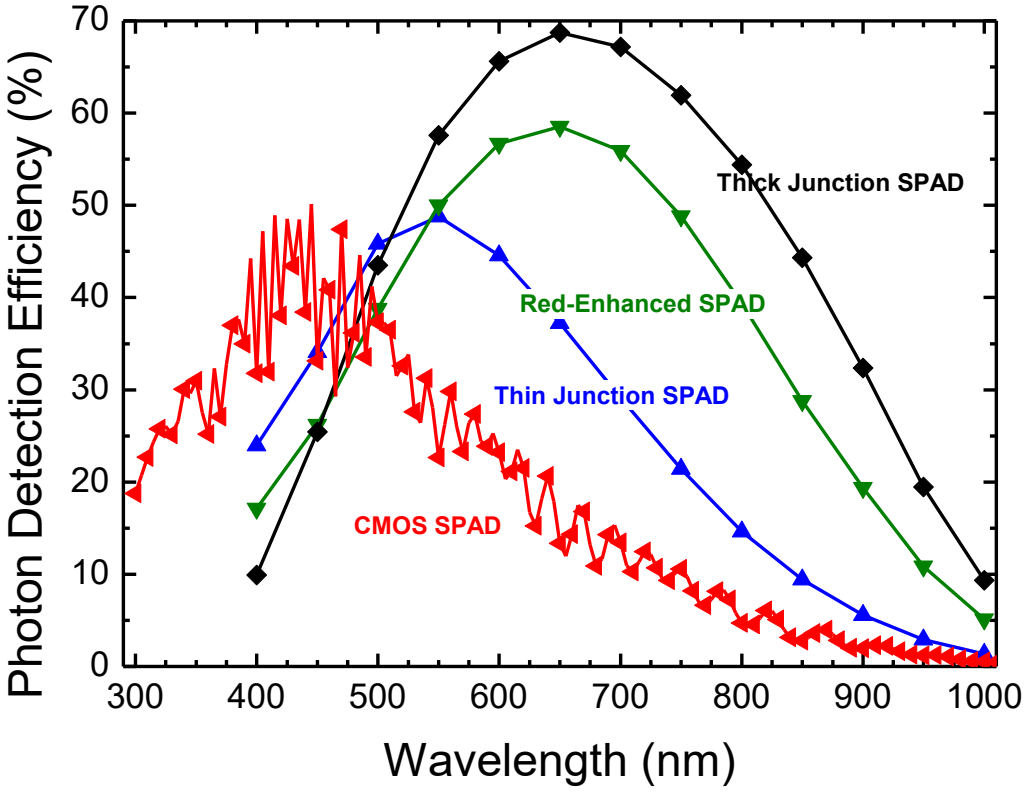
- First-photon 3D ranging

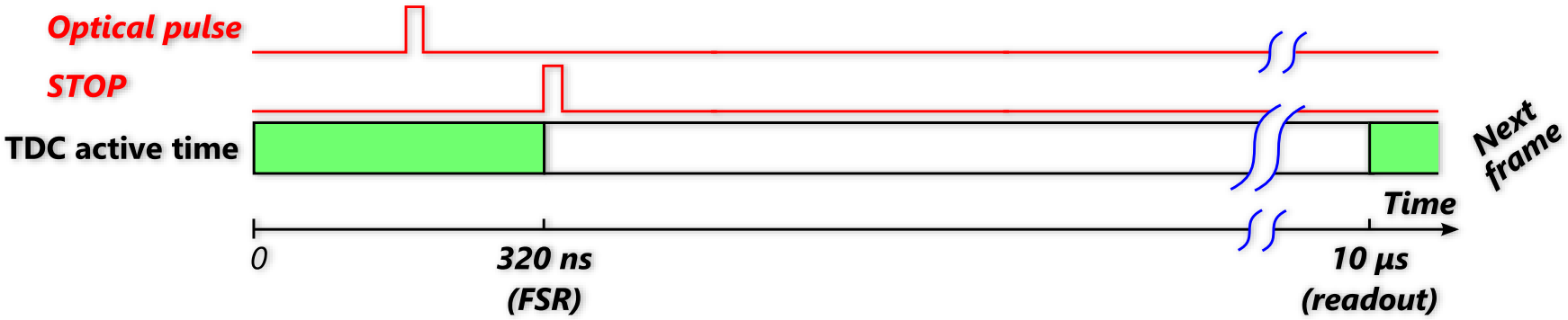


- Quantum physics (Weak measurements)

Main limitation of previous camera

- low PDE in the NIR
- low fill-factor
- low timing resolution
- no simultaneous counting/timing
- no hardware gating
- low TDC duty-cycle





New design specifications

Imager features:

- Hardware-gating and free-running modes
- In-pixel counters and TDC
- Multiple gates within 1 frame
- High flexibility: 2D imaging, 3D LIDAR, FLIM…

Best-in-class performance:

- SPADs with high PDE
- Fill Factor (> 5%)
- Timing resolution (< 100 ps)
- Scalability

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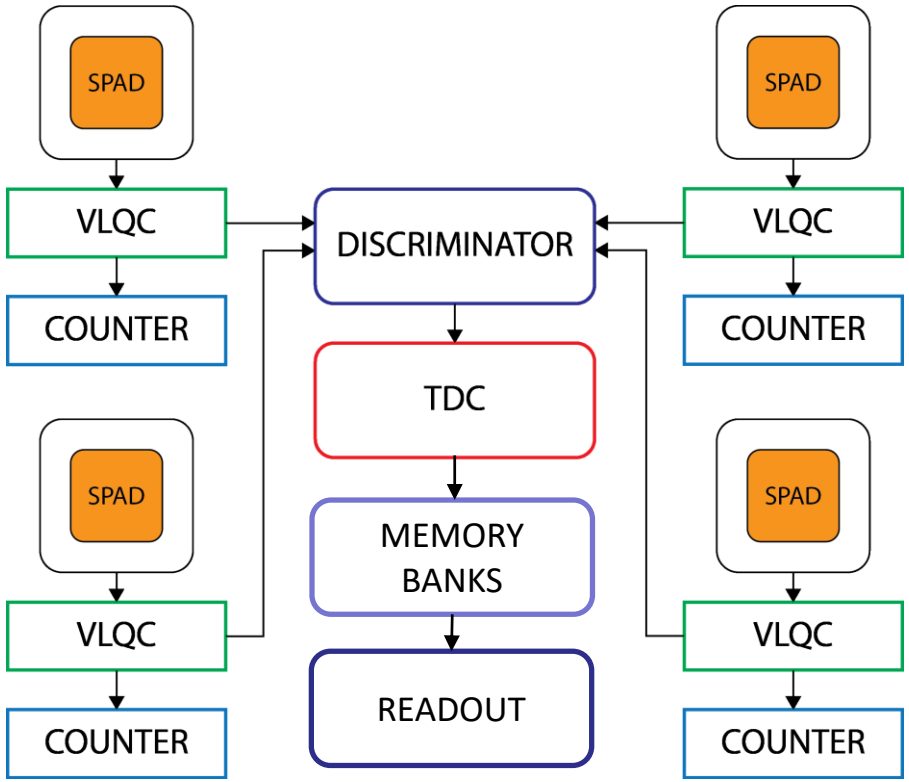
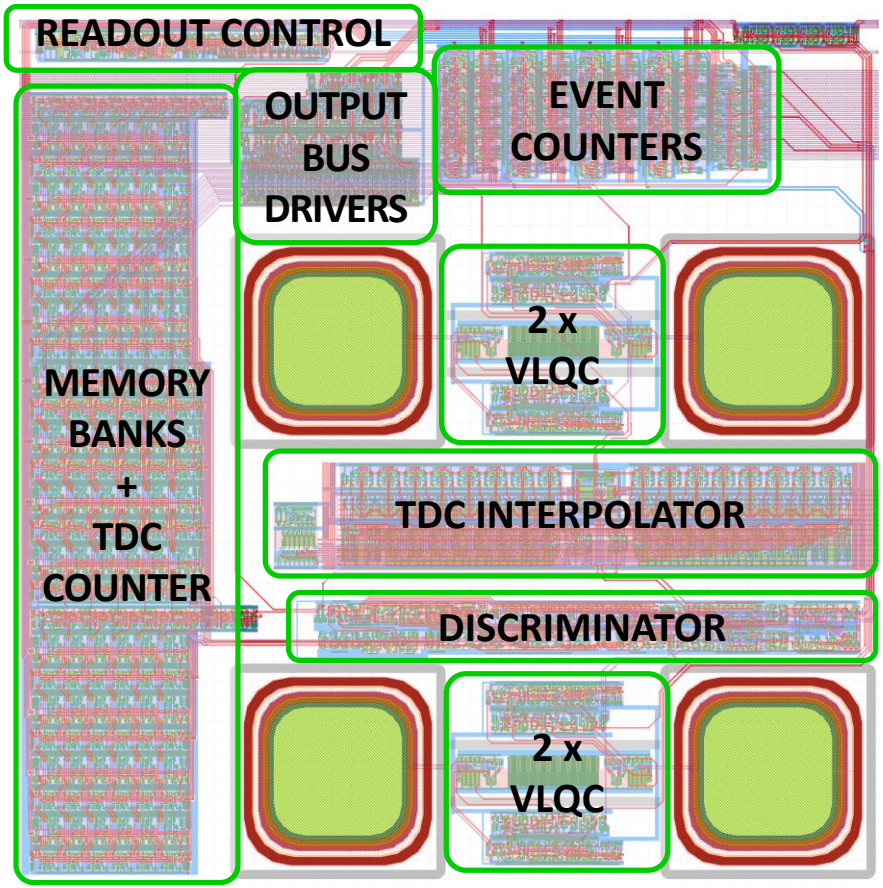
Macropixel architecture

- 32 μm square SPAD, 100 μm pitch, 9.6% fill factor
- 160 nm BCD technology





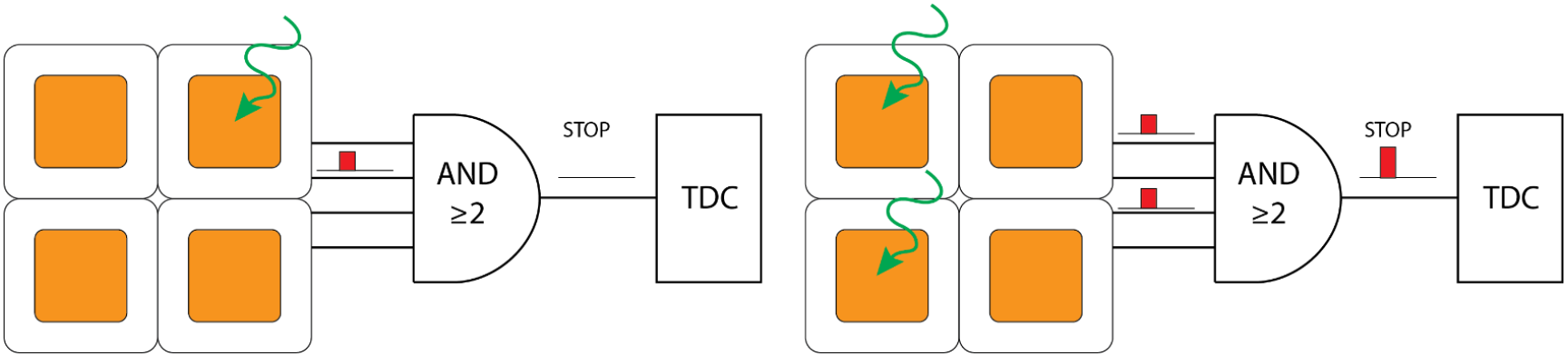
Macropixel operating modes

➢ Single-photon mode (preserve spatial information)

- TDC is shared with no loss of X-Y resolution
- Each SPAD has its own storage register

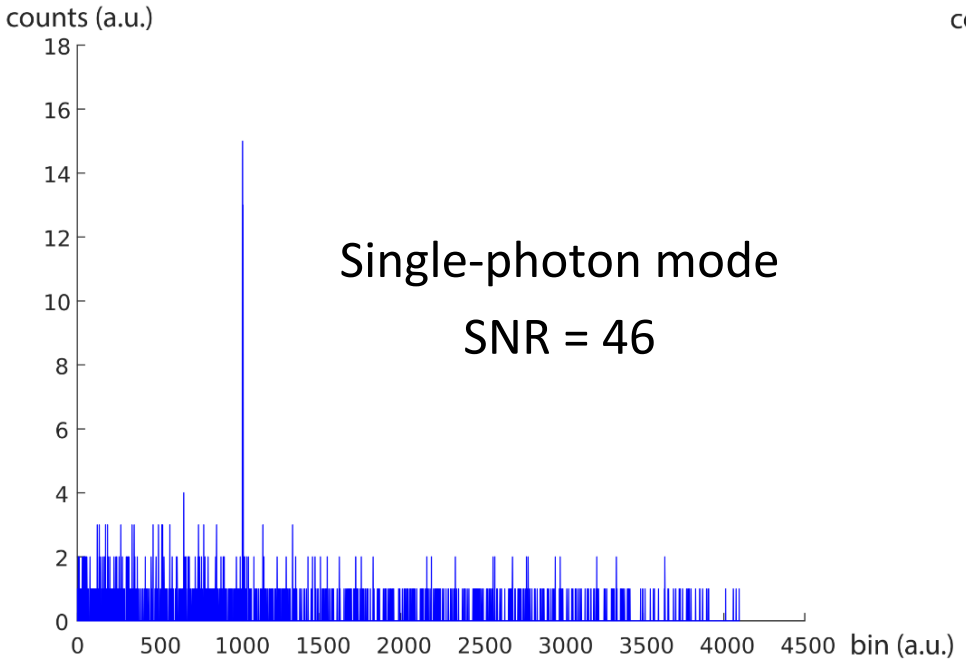
➢ Two-photon mode (ambient light suppression)

- Discrimination among multiple detectors, allowing 2×2 mini-SiPM operation



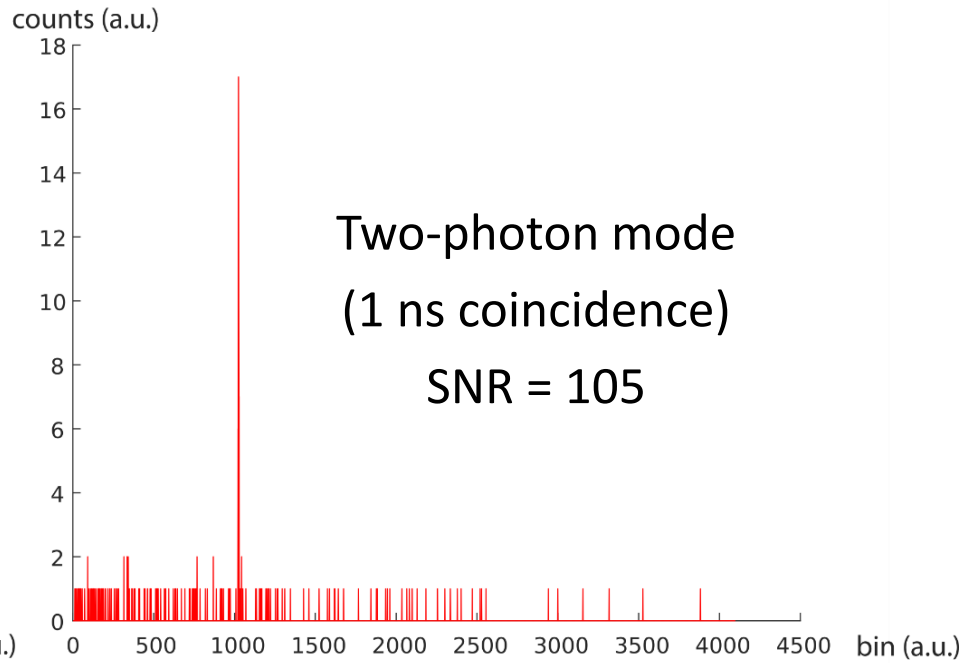
Two synchronous detections → one TDC conversion

Two-photon mode



Single-photon mode

SNR = 46



Two-photon mode

(1 ns coincidence)

SNR = 105

10 Mcps background, 10% PDP

Pro:

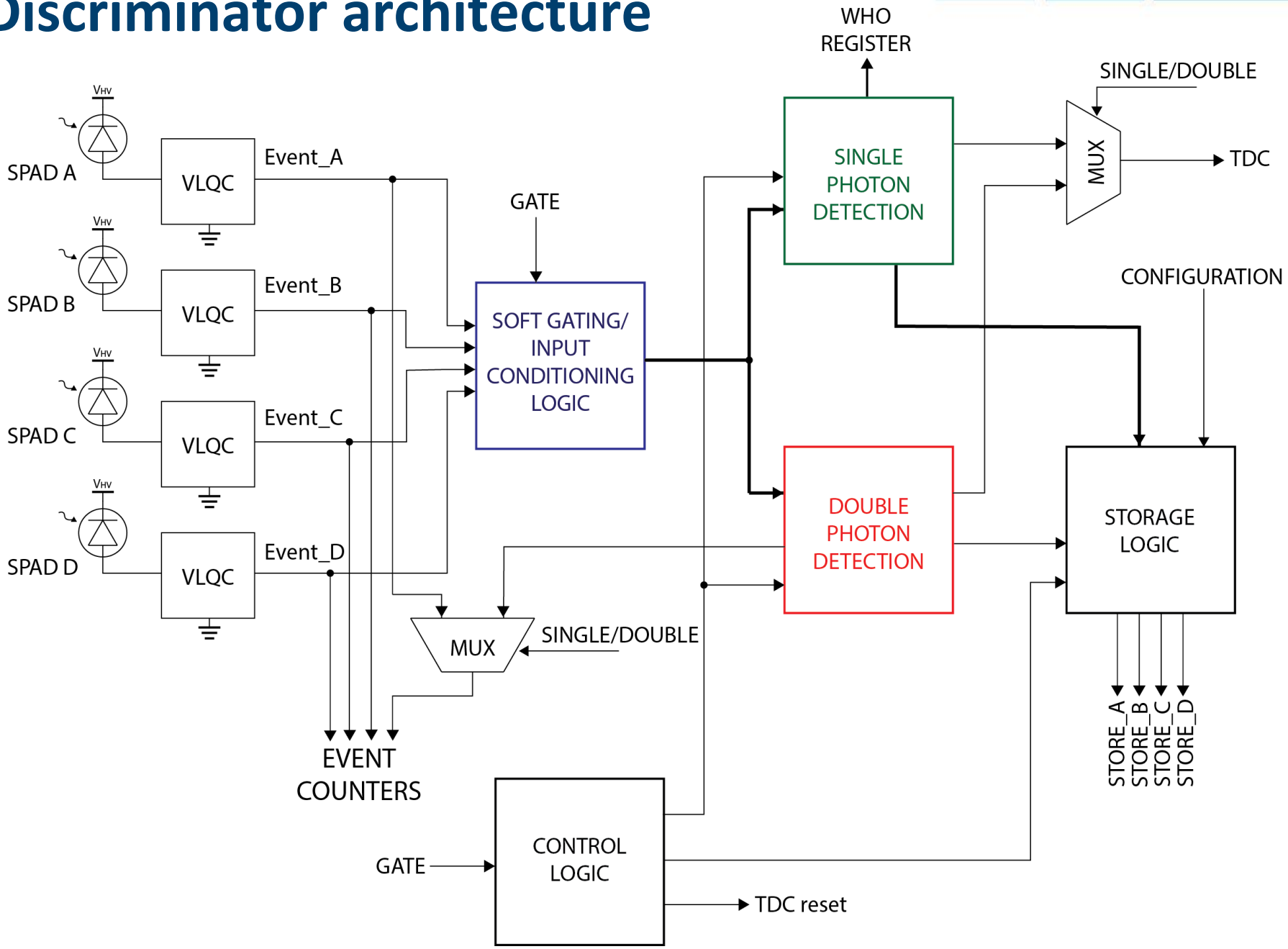
Uncorrelated noise suppression

Con:

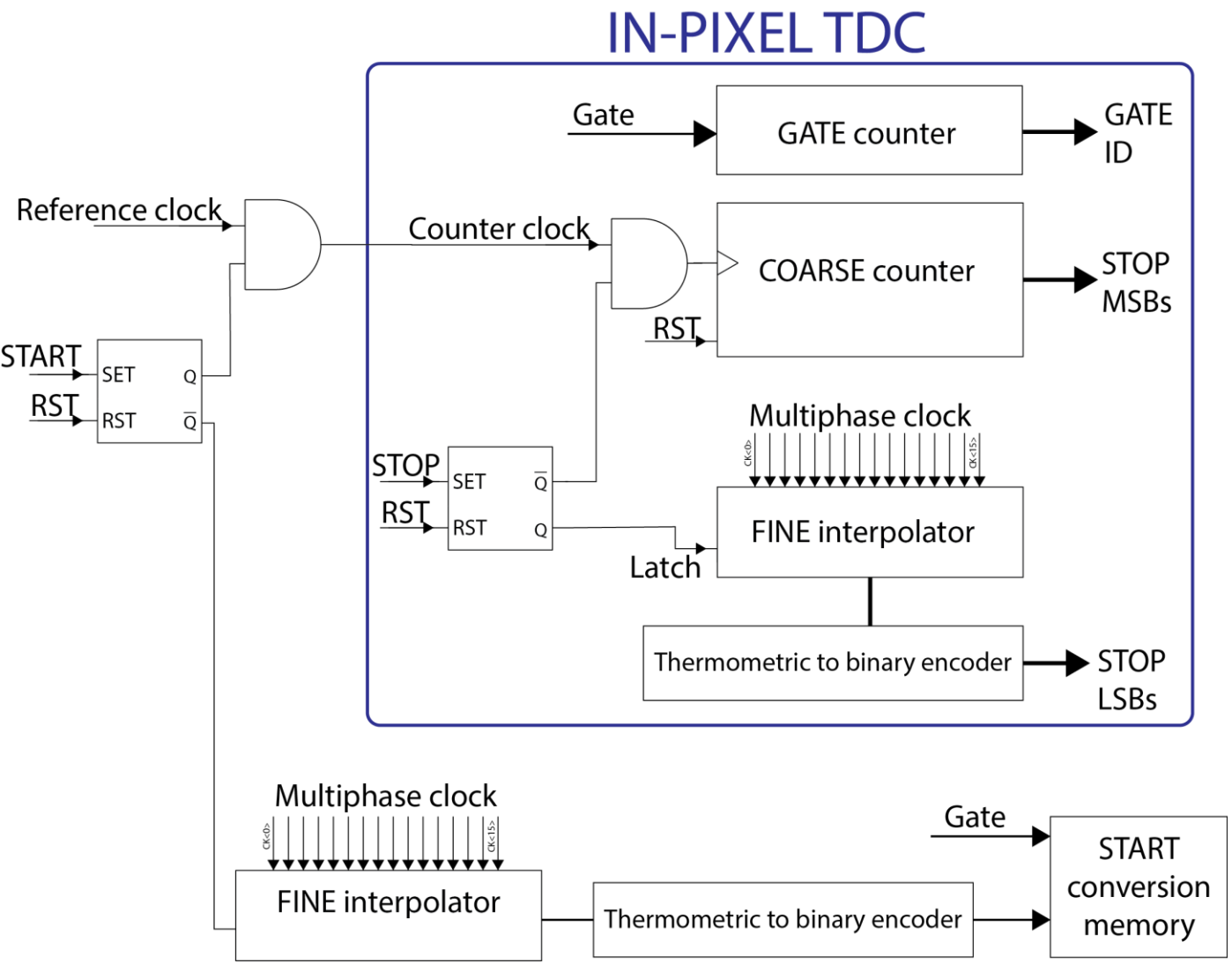
Halved spatial resolution

(like a mini-SiPM)

Discriminator architecture



TDC architecture



- 75 ps LSB, 12 bit (300 ns FSR)
- 415 MHz ref clock
- 7 bit coarse counter + 5 bit interpolator (STOP)
- Global electronics: START interpolator, DLL clock gen.
- Sliding scale
- Single-hit within gate, but multi-gate frame

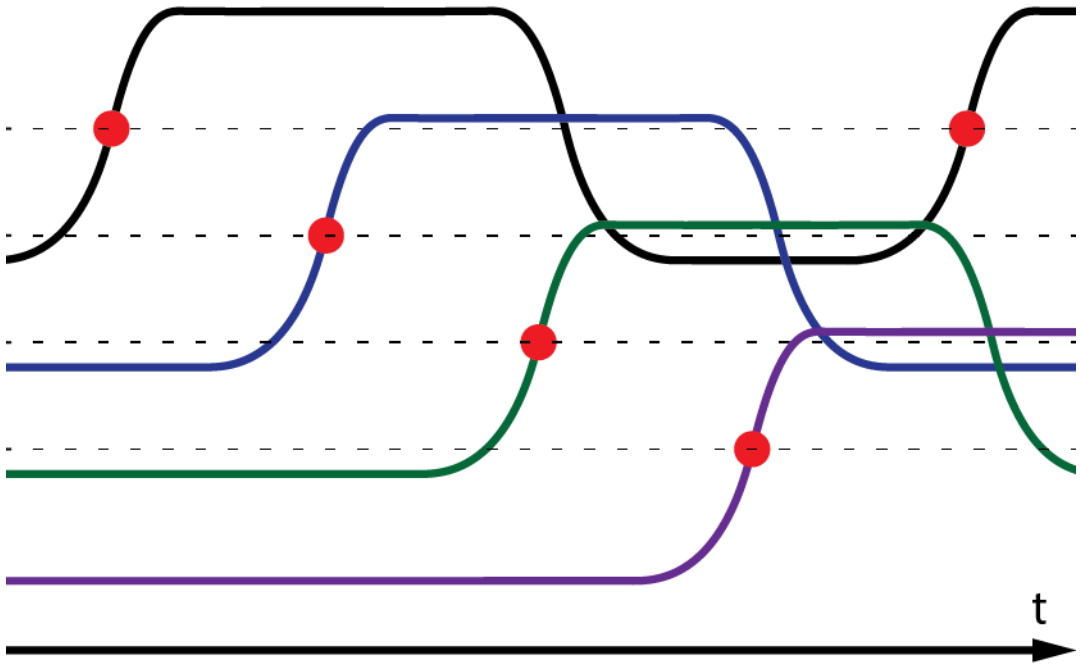
Innovative TDC features

- In-pixel gate counter → up to 64 gate windows per frame
- Rising- and falling-edge sensitive interpolator:

  ½ clock lines (reduced area occupation and power consumption)

  50% duty-cycle needed

STANDARD INTERPOLATOR



Innovative TDC features

- In-pixel gate counter → up to 64 gate windows per frame
- Rising- and falling-edge sensitive interpolator:

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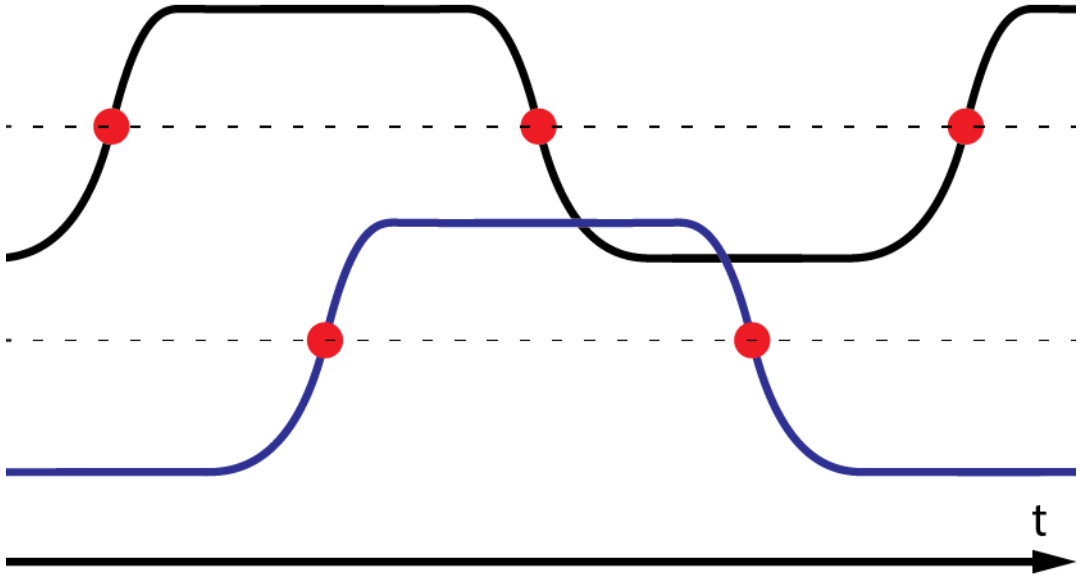
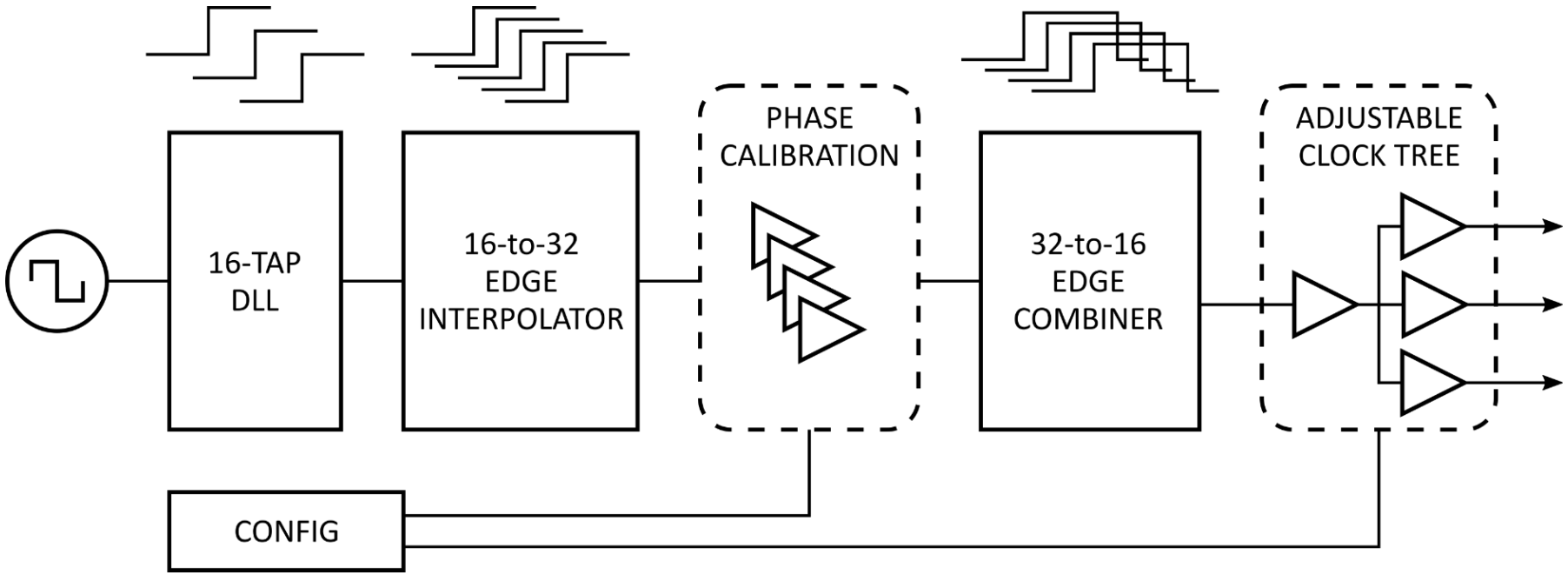
DUAL-EDGE SENSITIVE INTERPOLATOR



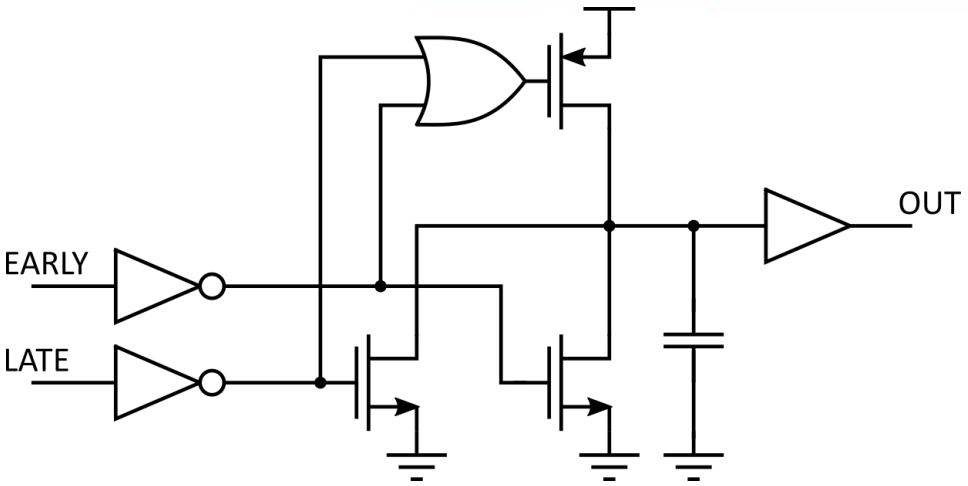
Multiphase clock generator

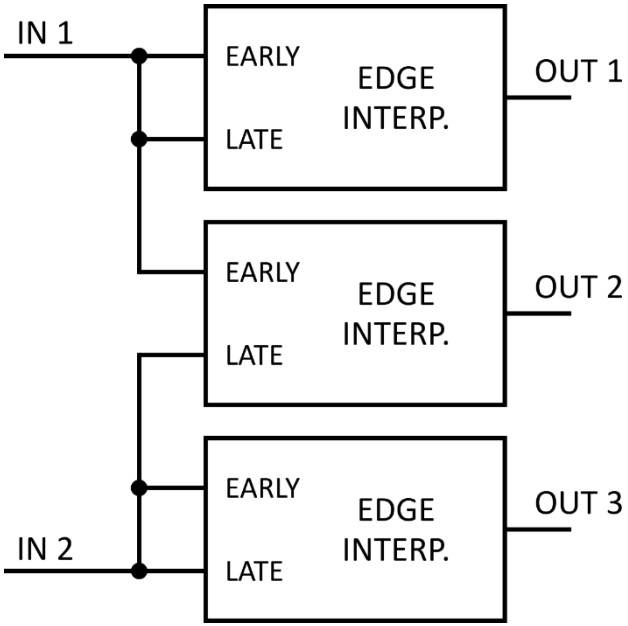
- 150 ps phase delay from DLL
- Clock edge interpolators to achieve 75 ps resolution
- Adjustable buffers for calibration

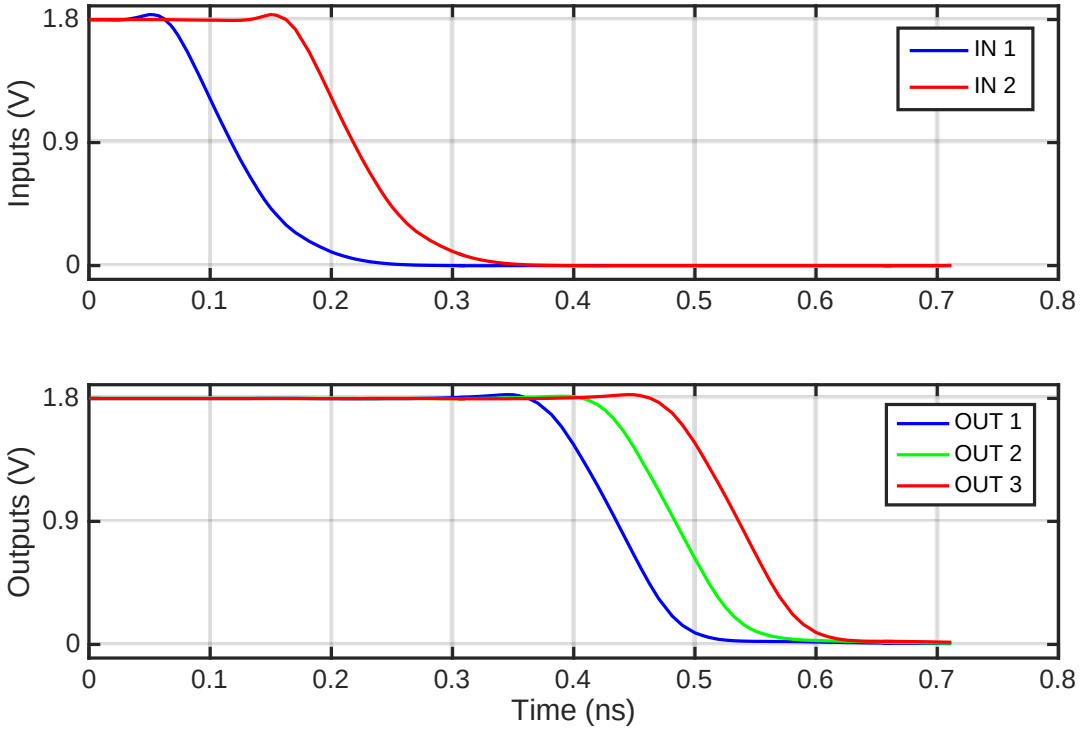


Edge interpolator

- Constant current C discharge
- Robust vs. process variations



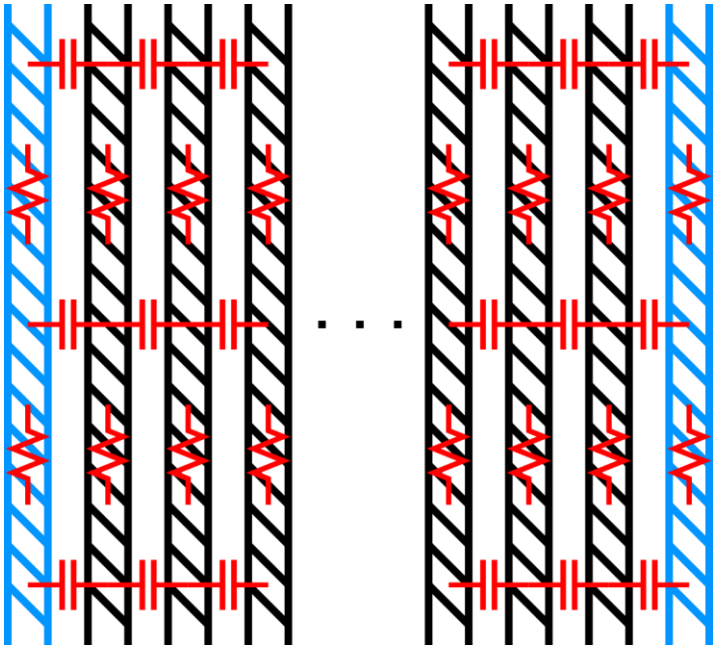


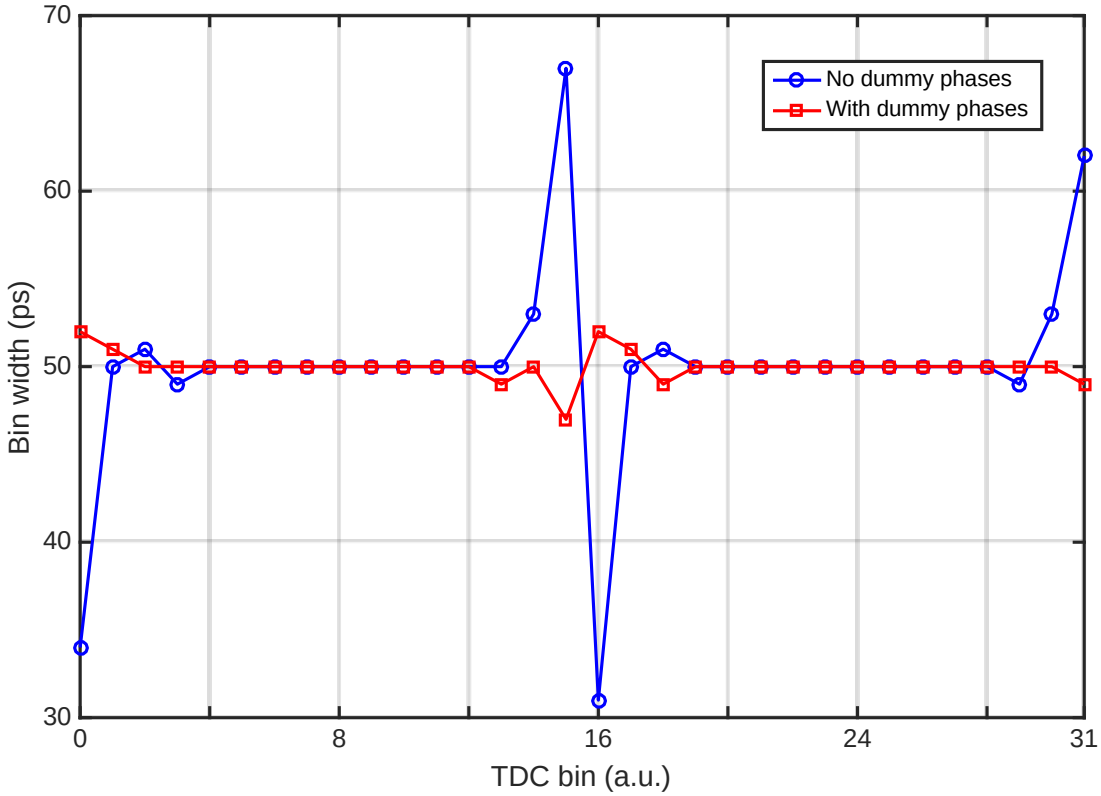


T. Saeki et al., JSSC, 2000

Dummy guard traces

- Crosstalk between clock phases results in non-linearity
- Routing within clock generator is critical
- Dummy phases added to global clock routing





Clock driver performance (post layout)

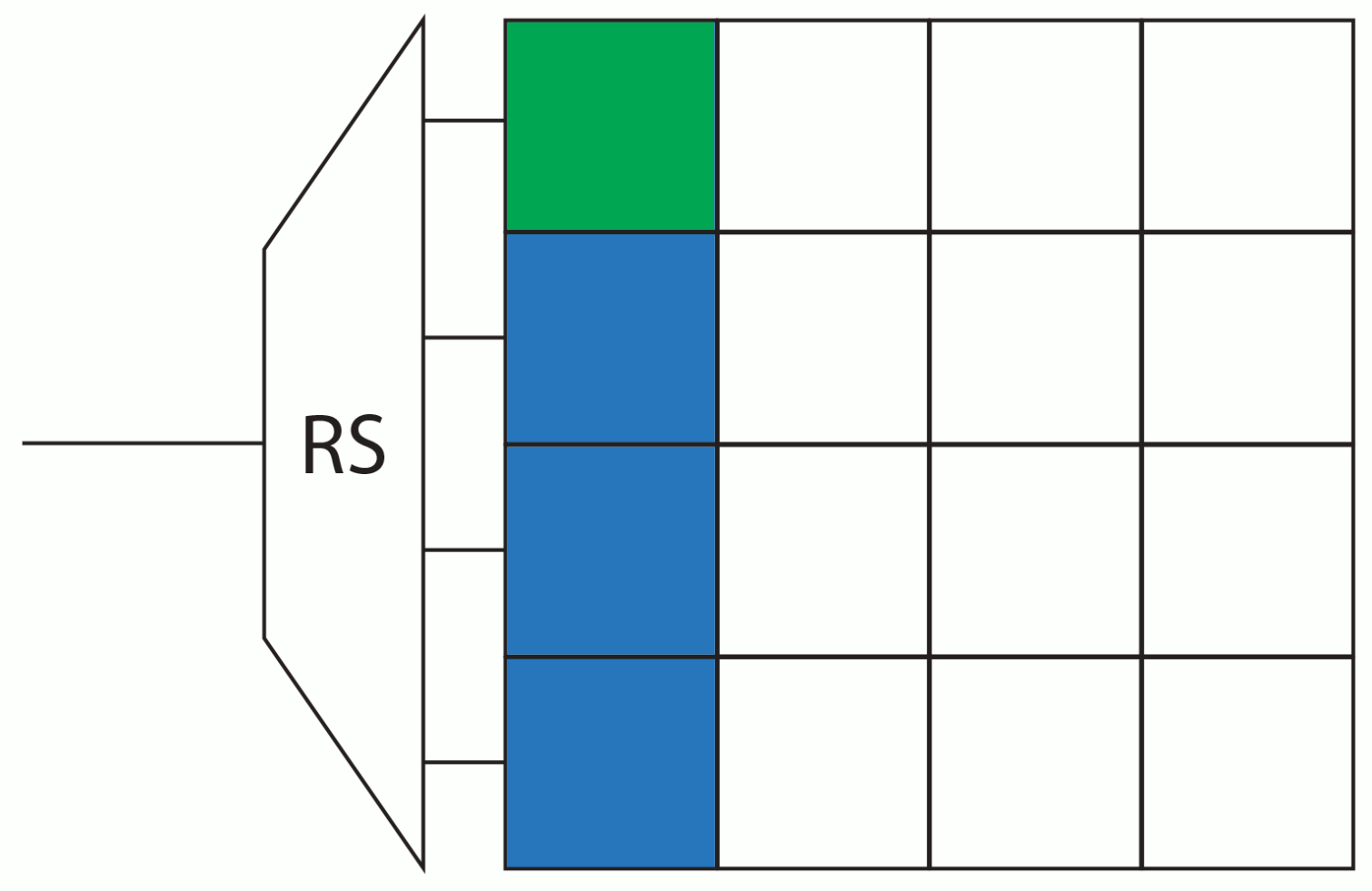
Vdd = 1.8 V	Near end	Far end
$T_{RISE_{20-80}}$	120 ps	202 ps
$T_{FALL_{20-80}}$	90 ps	170 ps

Vdd = 1.5 V	Near end	Far end
$T_{RISE_{20-80}}$	146 ps	221 ps
$T_{FALL_{20-80}}$	108 ps	182 ps

power consumption / performance trade-off
favorable for lower supply voltage

Power consumption	1.8V driver	1.5V driver
Overall clock-related power	4.93 W	**3.92 W (- 20%)**

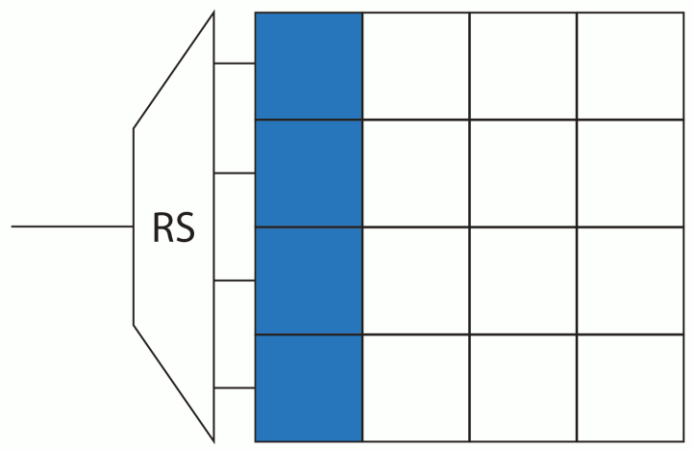
Single column select readout

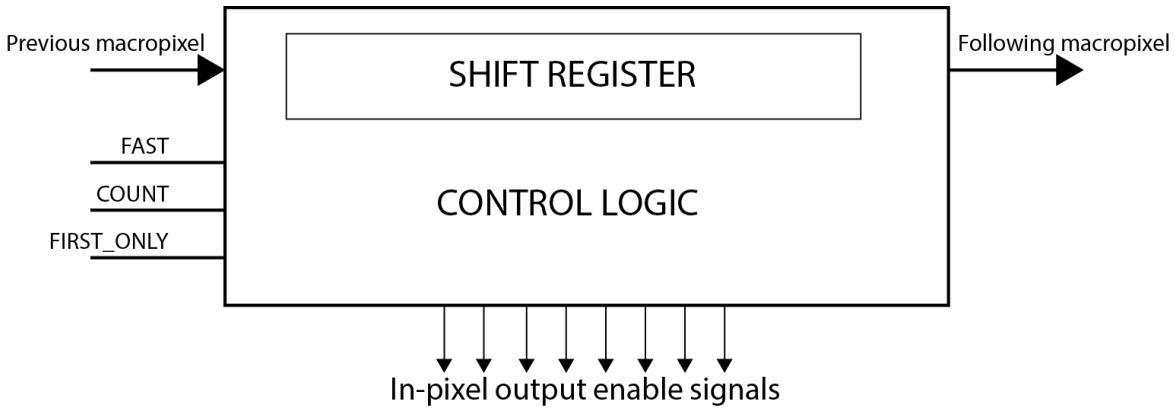


- PIXEL BEING READOUT
- PIXEL ENABLED, PRECHARGING THE BUS

In-pixel readout logic

- 3 static control signals: FAST, COUNT, FIRST_ONLY
- Distributed «one-hot» shift register plus combinatorial logic
- Maximizes bus precharge time, reduces number of global lines, offers great readout flexibility





PIXEL BEING READOUT

PIXEL ENABLED, PRECHARGING THE BUS

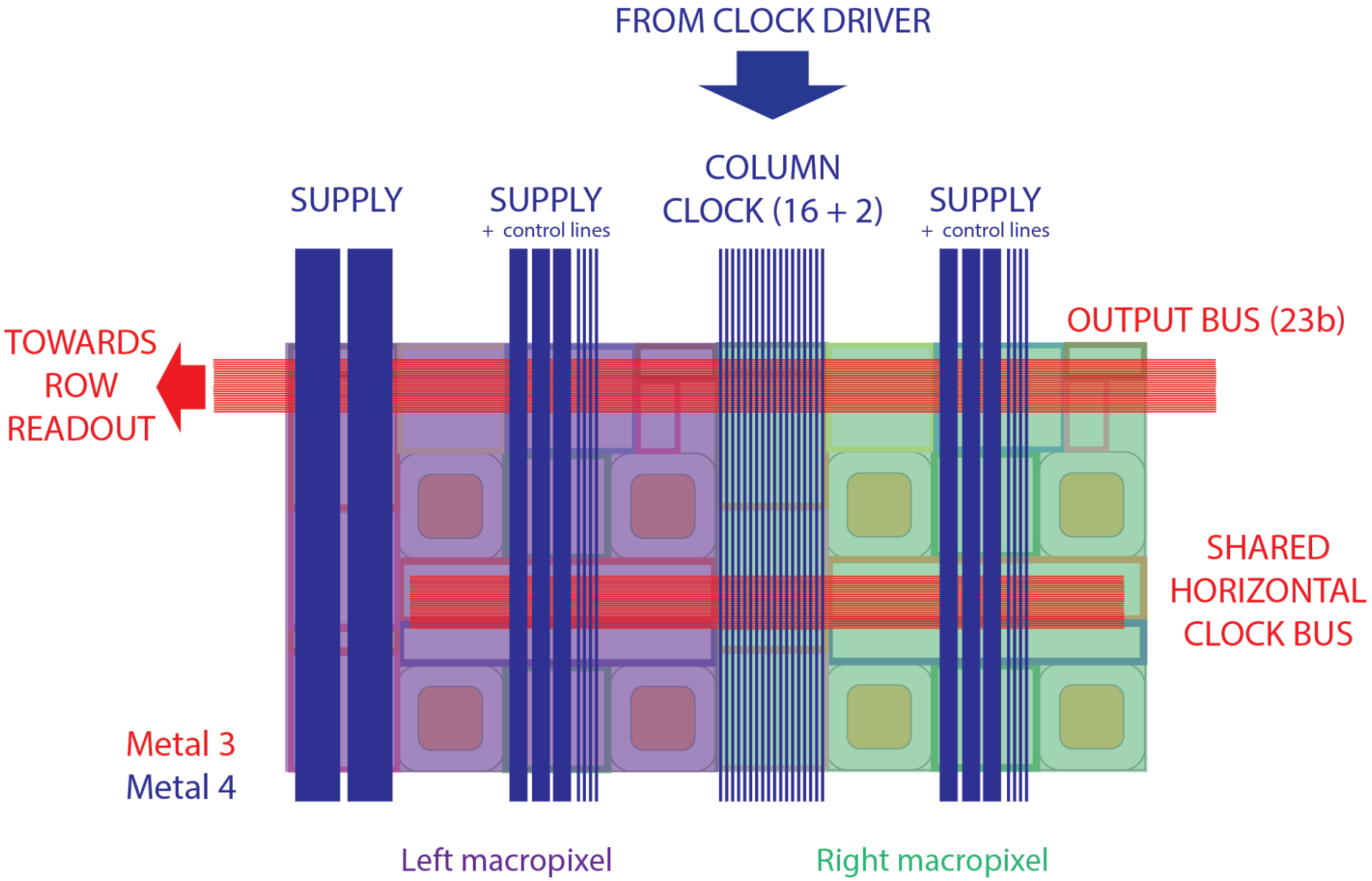
Available operation modes

Mode	Outputs	# cycles
Single-photon normal readout	4 timing (one per SPAD), 4 counters	4
Single-photon fast readout	First event timing, WHO, 4 counters	2
Single-photon first timing only	First event timing, WHO	1
Counting only	4 counters	1
Double-photon full readout	First 4 event timing, double event counter [3 SPAD single event counters]	4
Double-photon first only	First event timing, double event counter	1

Global routing constraints

- **Power supplies**
  - Thick top metal
- **TDC clocks**
  - 5 bit interpolator (32 phases @ 415 MHz)
  - Thick top metal
- **Row readout**
  - 23 bit bus
  - Metal 3 (thin)

Imager «building block»



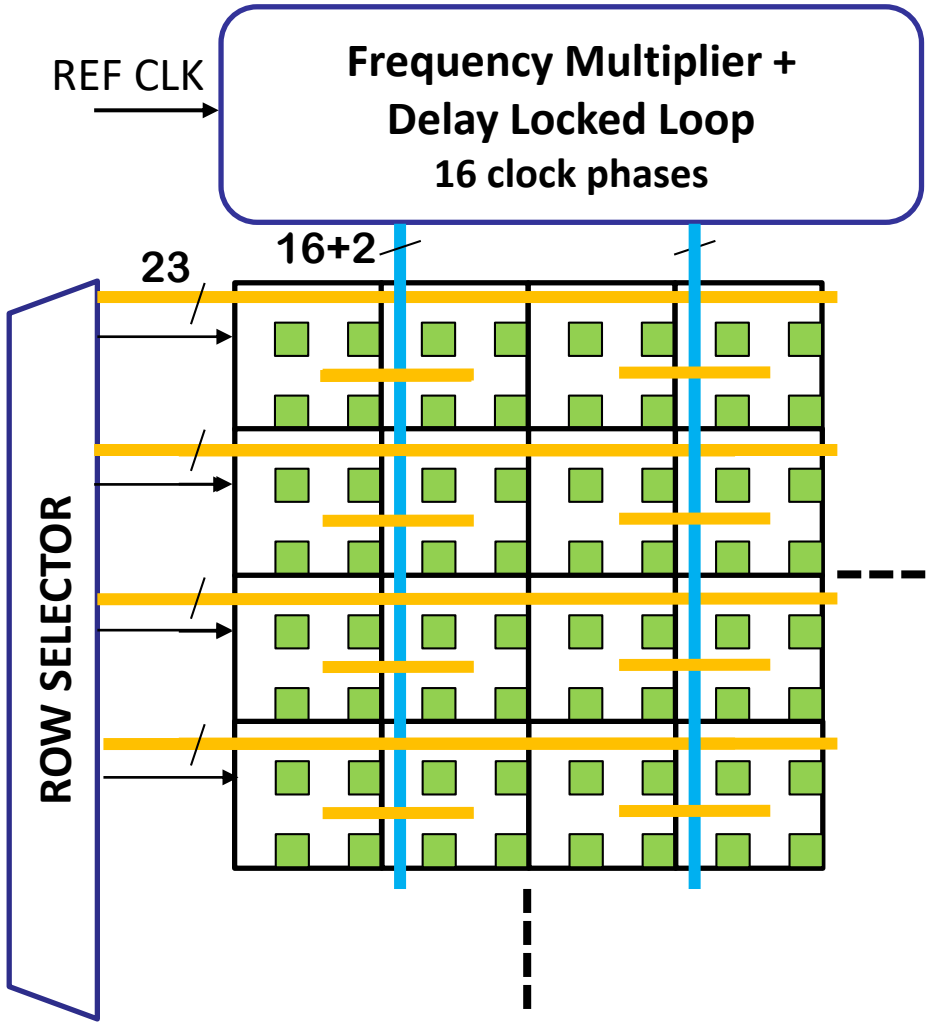
16x16 macropixel array

Macropixel

- 4 SPADs, VLQCs, gating
- TDC and event counters

Array

- 16x16 macropixels (32x32 SPADs)
- Clock generation
- Global readout electronics
- Power distribution

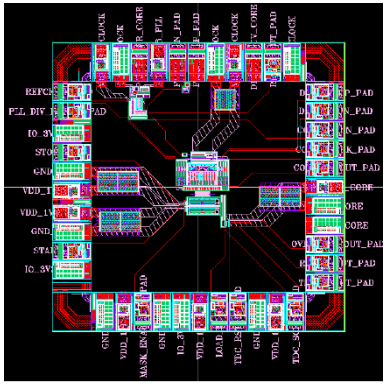


Fabricated chips

- **Stand-alone TDC**

  75 ps LSB, 300 ns FSR (extendable),

  1.6 x 1.6 mm^2

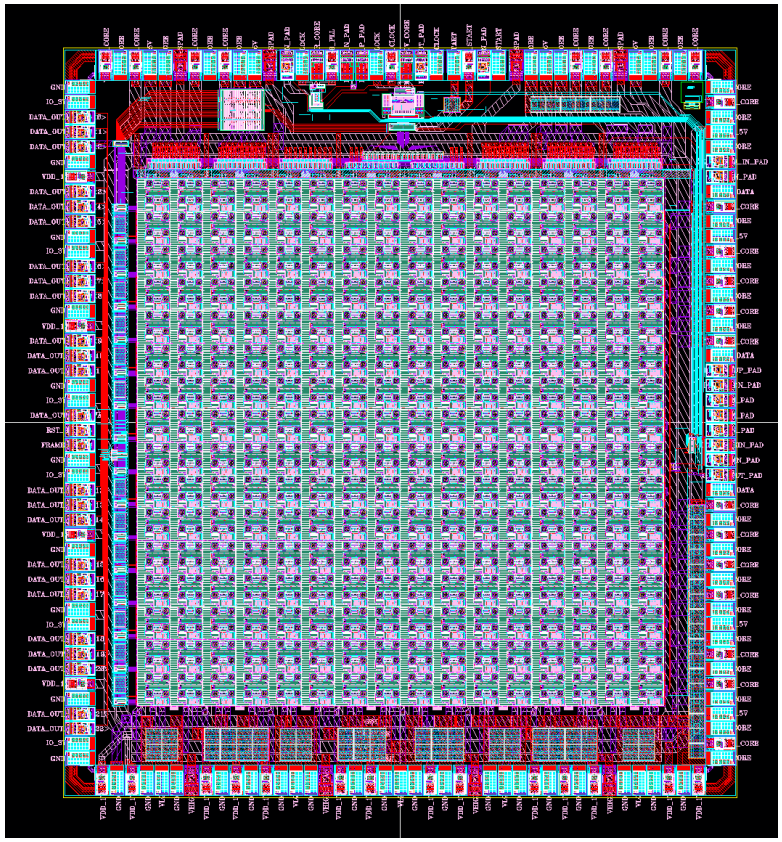


- **32 x 32 SPAD array**

  9.6% fill factor,

  1 mm^2 total active area,

  4.2 x 4.6 mm^2



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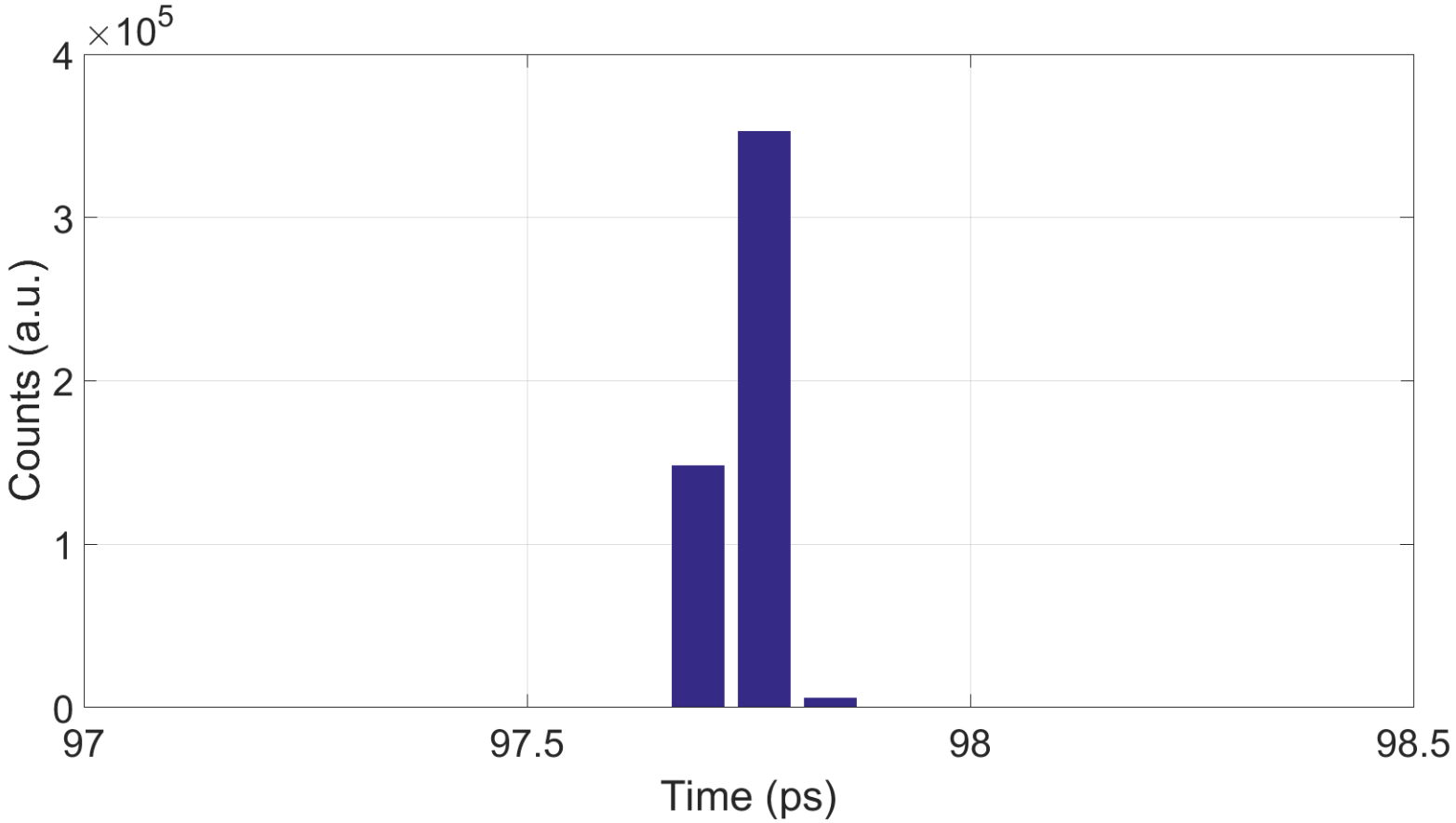
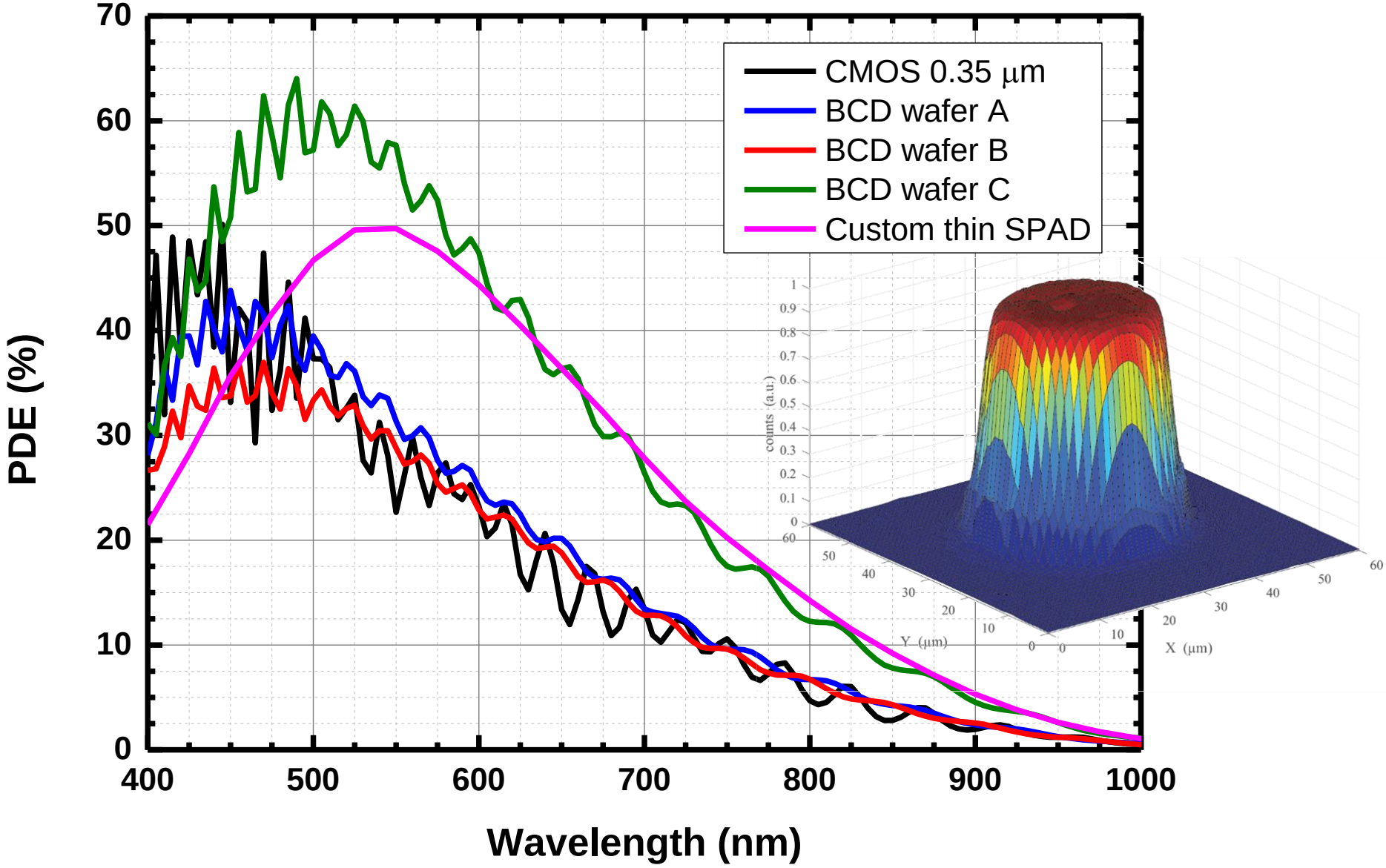
TDC preliminary characterization



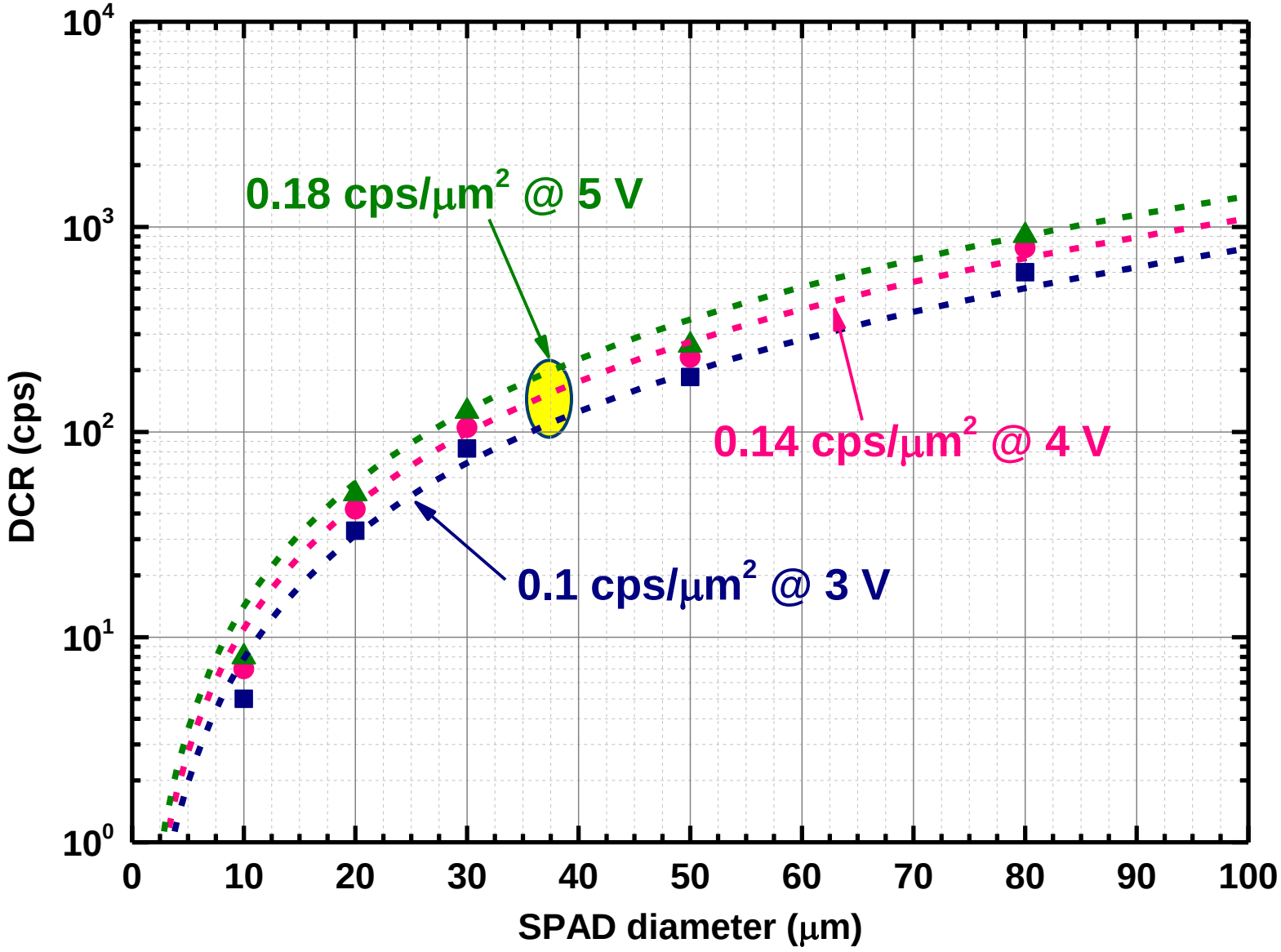
Single shot precision = 115 ps FWHM

SPAD PDE and uniformity



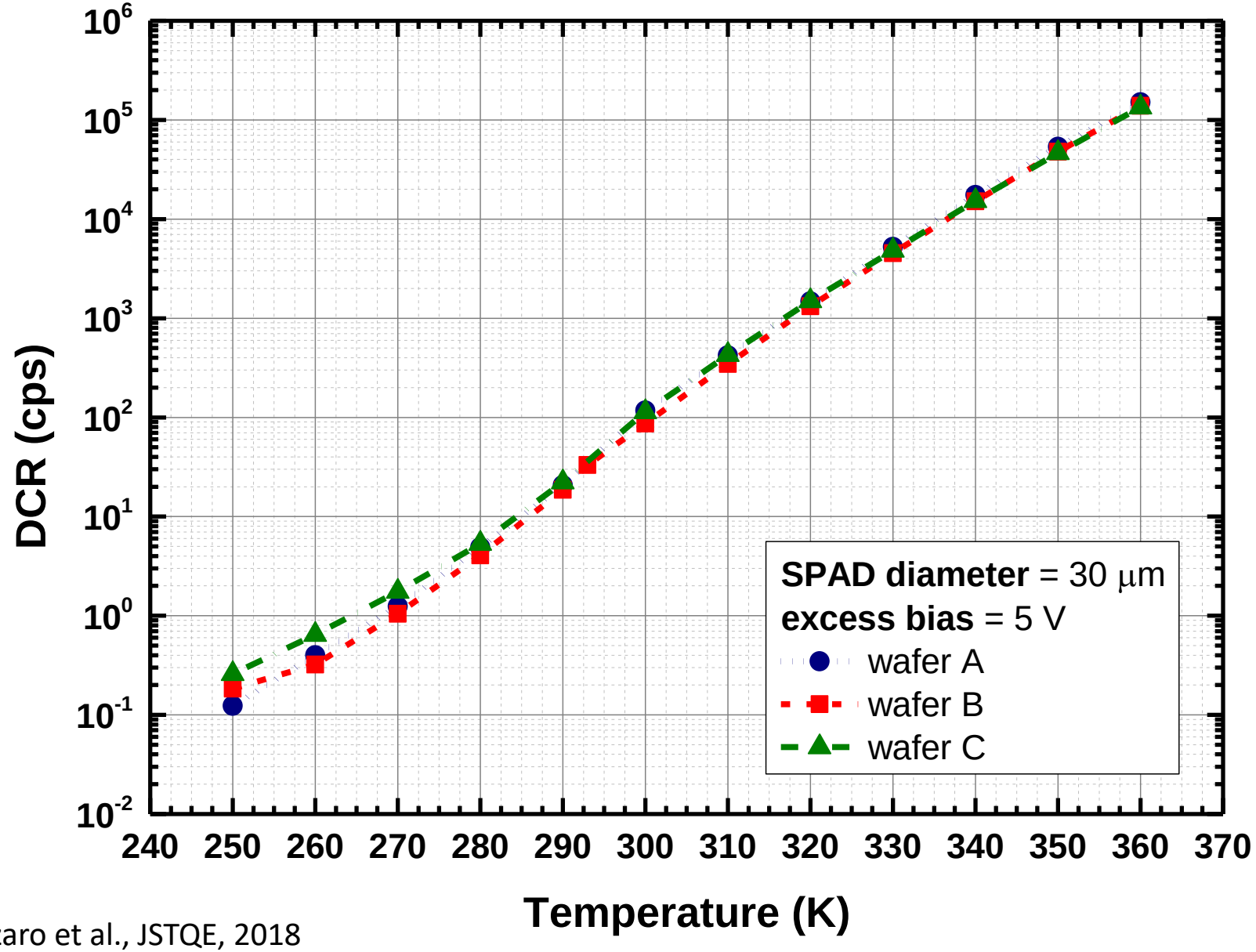
M. Sanzaro et al., JSTQE, 2018

SPAD DCR



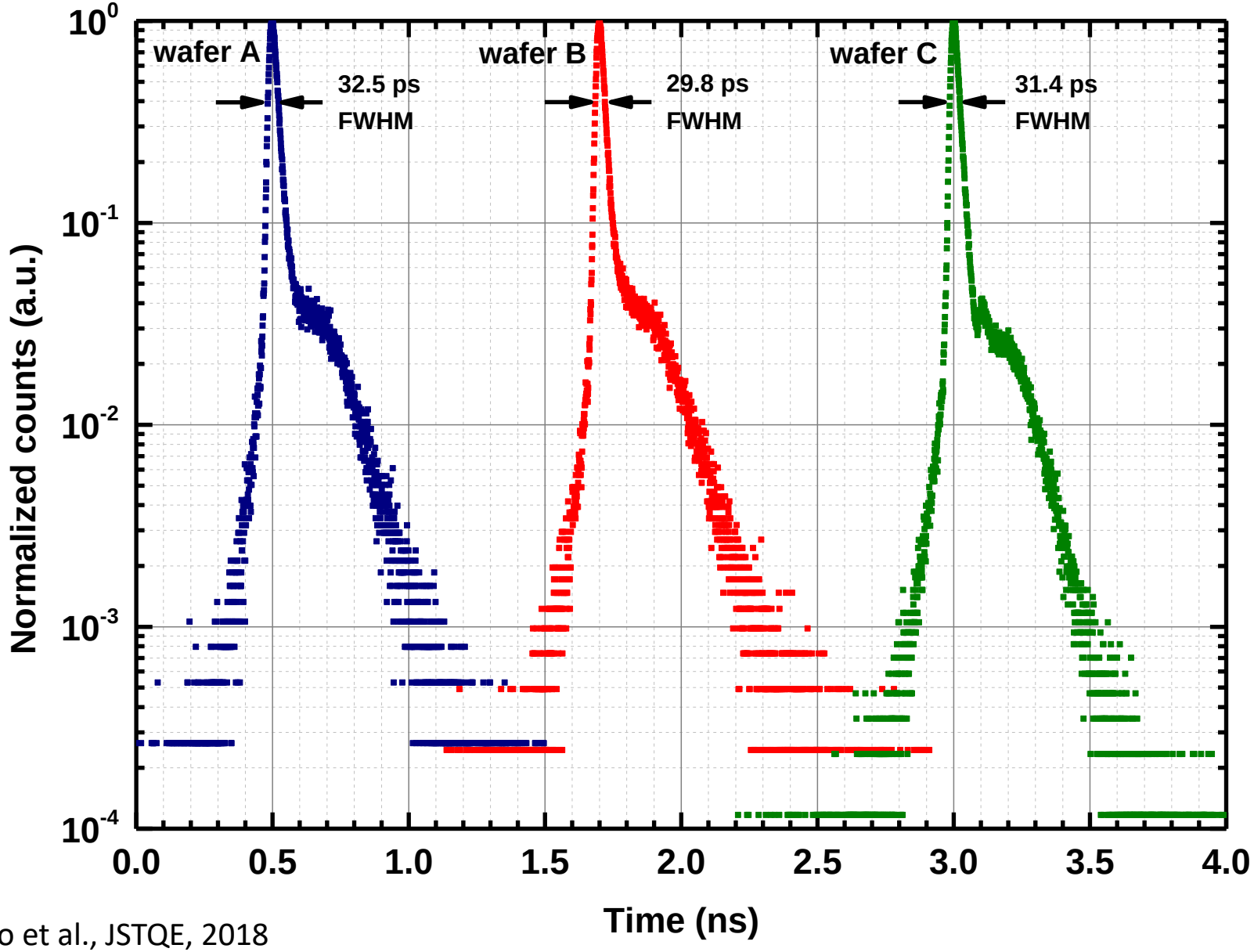
M. Sanzaro et al., JSTQE, 2018

SPAD DCR



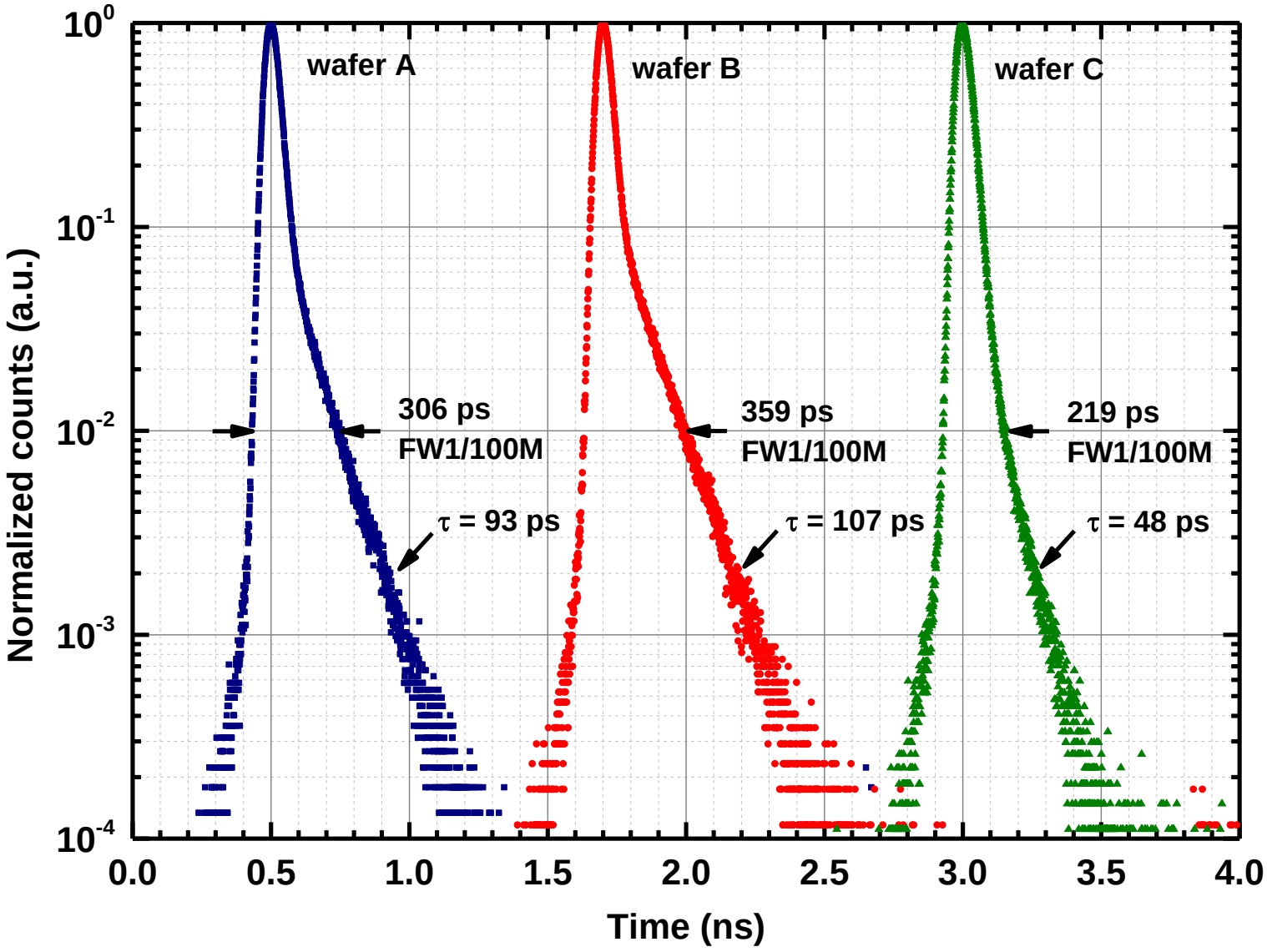
M. Sanzaro et al., JSTQE, 2018

SPAD timing (FWHM)



M. Sanzaro et al., JSTQE, 2018

SPAD timing (diffusion tail)



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Parameter	Value	Units
SPAD number	32 × 32	
TDC number	16 × 16	
SPAD pitch	100	µm
SPAD side	32	µm
Fill-factor	9.6%	
Operating mode	Only timing / Only counting Simultaneous timing and counting	
SPAD activation	HW gate Free running	
TDC resolution	75	ps
TDC FSR	300	ns
TDC number of bit	12	bit
TDC single-shot precision	115	ps (FWHM)
Counter number of bit	5	bit
SPAD PDE	60% (@500nm), 12% (@800nm)	
SPAD DCR	150	cps
SPAD time jitter	60	ps (FWHM)