BCD SPAD imager with reconfigurable macropixels for photon counting, timing and coincidence detection

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Outline

- Motivations and design goals
- SPAD imager architecture
  - “Macropixel” design
  - TDC structure
  - 32x32 array
- Chip characterizations
  - TDC preliminary tests
  - SPAD characterization
- Conclusions
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PoliMi $32\times32$ SPAD+TDC array chip

- 1024 smart pixels
- 30-µm diameter SPADs
  (3.14% fill-factor)
- 10-bit in-pixel TDCs
  for “photon-timing” (TOF 3D ranging, FLIM)
  312 ps LSB, 320 ns FSR
- 6-bit in-pixel counters
  for “photon-counting” (2D imaging)
- 100,000 frames/s

F. Villa et al., JSTQE, 2014
Single-photon camera

SPAD+TDC array chip carrier board

Analog interface board
(for interfacing the chip and handling triggering and synchronization input/output signals)

Digital processing board
(FPGA for data processing, storage, and USB3 communication link)

Power supply board
(power supplies generation, including user-selectable SPAD bias)

R. Lussana et al., OE, 2015
Many applications

- 3D ranging at short-distance
- Satellite 3D ranging
- First-photon 3D ranging
- Quantum physics (Weak measurements)
Main limitation of previous camera

- low PDE in the NIR
- low fill-factor
- low timing resolution
- no simultaneous counting/timing
- no hardware gating
- low TDC duty-cycle
New design specifications

Imager features:

• Hardware-gating and free-running modes
• In-pixel counters and TDC
• Multiple gates within 1 frame
• High flexibility: 2D imaging, 3D LIDAR, FLIM...

Best-in-class performance:

• SPADs with high PDE
• Fill Factor (> 5%)
• Timing resolution (< 100 ps)
• Scalability
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Macropixel architecture

- 32 µm square SPAD, 100 µm pitch, 9.6% fill factor
- 160 nm BCD technology
Macropixel operating modes

- **Single-photon mode (preserve spatial information)**
  
  - TDC is shared with no loss of X-Y resolution
  - Each SPAD has its own storage register

- **Two-photon mode (ambient light suppression)**
  
  - Discrimination among multiple detectors, allowing 2×2 mini-SiPM operation

  ![Diagram](image)

  Two synchronous detections $\rightarrow$ one TDC conversion
Two-photon mode

Single-photon mode
SNR = 46

Two-photon mode (1 ns coincidence)
SNR = 105

10 Mcps background, 10% PDP

Pro:
Uncorrelated noise suppression

Con:
Halved spatial resolution (like a mini-SiPM)
Discriminator architecture
TDC architecture

IN-PIXEL TDC

- 75 ps LSB, 12 bit (300 ns FSR)
- 415 MHz ref clock
- 7 bit coarse counter + 5 bit interpolator (STOP)
- Global electronics: START interpolator, DLL clock gen.
- Sliding scale
- Single-hit within gate, but multi-gate frame
Innovative TDC features

• In-pixel gate counter $\rightarrow$ up to 64 gate windows per frame

• Rising- and falling-edge sensitive interpolator:
  $\frac{1}{2}$ clock lines (reduced area occupation and power consumption)
  50% duty-cycle needed
Innovative TDC features

- In-pixel gate counter → up to 64 gate windows per frame
- Rising- and falling-edge sensitive interpolator:
  ½ clock lines (reduced area occupation and power consumption)
  50% duty-cycle needed
Multiphase clock generator

- 150 ps phase delay from DLL
- Clock edge interpolators to achieve 75 ps resolution
- Adjustable buffers for calibration
**Edge interpolator**

- Constant current $C$ discharge
- Robust vs. process variations

![Edge Interpolator Diagram]

T. Saeki et al., JSSC, 2000
Dummy guard traces

- Crosstalk between clock phases results in non-linearity
- Routing within clock generator is critical
- Dummy phases added to global clock routing

![Diagram showing comparison between traces with and without dummy phases](image)
Clock driver performance (post layout)

<table>
<thead>
<tr>
<th>Voltage (Vdd)</th>
<th>Near end $T_{RISE_{20-80}}$</th>
<th>Near end $T_{FALL_{20-80}}$</th>
<th>Far end $T_{RISE_{20-80}}$</th>
<th>Far end $T_{FALL_{20-80}}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.8 V</td>
<td>120 ps</td>
<td>170 ps</td>
<td>202 ps</td>
<td>182 ps</td>
</tr>
<tr>
<td>1.5 V</td>
<td>146 ps</td>
<td>182 ps</td>
<td>221 ps</td>
<td>208 ps</td>
</tr>
</tbody>
</table>

Power consumption / performance trade-off favorable for lower supply voltage

<table>
<thead>
<tr>
<th>Power consumption</th>
<th>1.8V driver</th>
<th>1.5V driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overall clock-related power</td>
<td>4.93 W</td>
<td>3.92 W</td>
</tr>
<tr>
<td></td>
<td>( - 20% )</td>
<td></td>
</tr>
</tbody>
</table>
Single column select readout

- PIXEL BEING READOUT
- PIXEL ENABLED, PRECHARGING THE BUS
In-pixel readout logic

- 3 static control signals: FAST, COUNT, FIRST_ONLY
- Distributed «one-hot» shift register plus combinatorial logic
- Maximizes bus precharge time, reduces number of global lines, offers great readout flexibility

![Diagram of in-pixel readout logic]

- PIXEL BEING READOUT
- PIXEL ENABLED, PRECHARGING THE BUS

ISSW, February 27th, 2018
federica.villa@polimi.it
### Available operation modes

<table>
<thead>
<tr>
<th>Mode</th>
<th>Outputs</th>
<th># cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single-photon normal readout</td>
<td>4 timing (one per SPAD), 4 counters</td>
<td>4</td>
</tr>
<tr>
<td>Single-photon fast readout</td>
<td>First event timing, WHO, 4 counters</td>
<td>2</td>
</tr>
<tr>
<td>Single-photon first timing only</td>
<td>First event timing, WHO</td>
<td>1</td>
</tr>
<tr>
<td>Counting only</td>
<td>4 counters</td>
<td>1</td>
</tr>
<tr>
<td>Double-photon full readout</td>
<td>First 4 event timing, double event counter [3 SPAD single event counters]</td>
<td>4</td>
</tr>
<tr>
<td>Double-photon first only</td>
<td>First event timing, double event counter</td>
<td>1</td>
</tr>
</tbody>
</table>
Global routing constraints

- **Power supplies**
  - Thick top metal

- **TDC clocks**
  - 5 bit interpolator (32 phases @ 415 MHz)
  - Thick top metal

- **Row readout**
  - 23 bit bus
  - Metal 3 (thin)
Imager «building block»

FROM CLOCK DRIVER

SUPPLY

SUPPLY + control lines

COLUMN CLOCK (16 + 2)

SUPPLY + control lines

OUTPUT BUS (23b)

TOWARDS ROW READOUT

Metal 3 Metal 4

Left macro-pixel

Right macro-pixel

SHARED HORIZONTAL CLOCK BUS
16x16 macropixel array

- **Macropixel**
  - 4 SPADs, VLQC gates, gating
  - TDC and event counters

- **Array**
  - 16x16 macropixels (32x32 SPADs)
  - Clock generation
  - Global readout electronics
  - Power distribution

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Frequency Multiplier +
Delay Locked Loop
16 clock phases
Fabricated chips

- **Stand-alone TDC**
  
  75 ps LSB, 300 ns FSR (extendable),
  1.6 x 1.6 mm$^2$

- **32 x 32 SPAD array**
  
  9.6% fill factor,
  1 mm$^2$ total active area,
  4.2 x 4.6 mm$^2$
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TDC preliminary characterization

Single shot precision = 115 ps FWHM
SPAD PDE and uniformity

M. Sanzaro et al., JSTQE, 2018
SPAD DCR

M. Sanzaro et al., JSTQE, 2018
SPAD DCR

SPAD diameter = 30 \mu m
excess bias = 5 V

wafer A
wafer B
wafer C

M. Sanzaro et al., JSTQE, 2018
SPAD timing (FWHM)

M. Sanzaro et al., JSTQE, 2018
SPAD timing (diffusion tail)

![Graph showing SPAD timing with three wafers: A, B, and C. The graph displays normalized counts (a.u.) against time (ns) on a logarithmic scale.]

- **Wafer A**: τ = 93 ps, 306 ps FW1/100M
- **Wafer B**: τ = 107 ps, 359 ps FW1/100M
- **Wafer C**: τ = 48 ps, 219 ps FW1/100M
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<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPAD number</td>
<td>32 × 32</td>
<td></td>
</tr>
<tr>
<td>TDC number</td>
<td>16 × 16</td>
<td></td>
</tr>
<tr>
<td>SPAD pitch</td>
<td>100</td>
<td>µm</td>
</tr>
<tr>
<td>SPAD side</td>
<td>32</td>
<td>µm</td>
</tr>
<tr>
<td>Fill-factor</td>
<td>9.6%</td>
<td></td>
</tr>
<tr>
<td>Operating mode</td>
<td>Only timing / Only counting</td>
<td></td>
</tr>
<tr>
<td>Simultaneous timing and counting</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SPAD activation</td>
<td>HW gate</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Free running</td>
<td></td>
</tr>
<tr>
<td>TDC resolution</td>
<td>75</td>
<td>ps</td>
</tr>
<tr>
<td>TDC FSR</td>
<td>300</td>
<td>ns</td>
</tr>
<tr>
<td>TDC number of bit</td>
<td>12</td>
<td>bit</td>
</tr>
<tr>
<td>TDC single-shot precision</td>
<td>115</td>
<td>ps (FWHM)</td>
</tr>
<tr>
<td>Counter number of bit</td>
<td>5</td>
<td>bit</td>
</tr>
<tr>
<td>SPAD PDE</td>
<td>60% (@500nm), 12% (@800nm)</td>
<td></td>
</tr>
<tr>
<td>SPAD DCR</td>
<td>150</td>
<td>cps</td>
</tr>
<tr>
<td>SPAD time jitter</td>
<td>60</td>
<td>ps (FWHM)</td>
</tr>
</tbody>
</table>