Multizone, Multiobject D-TOF System in 55nm

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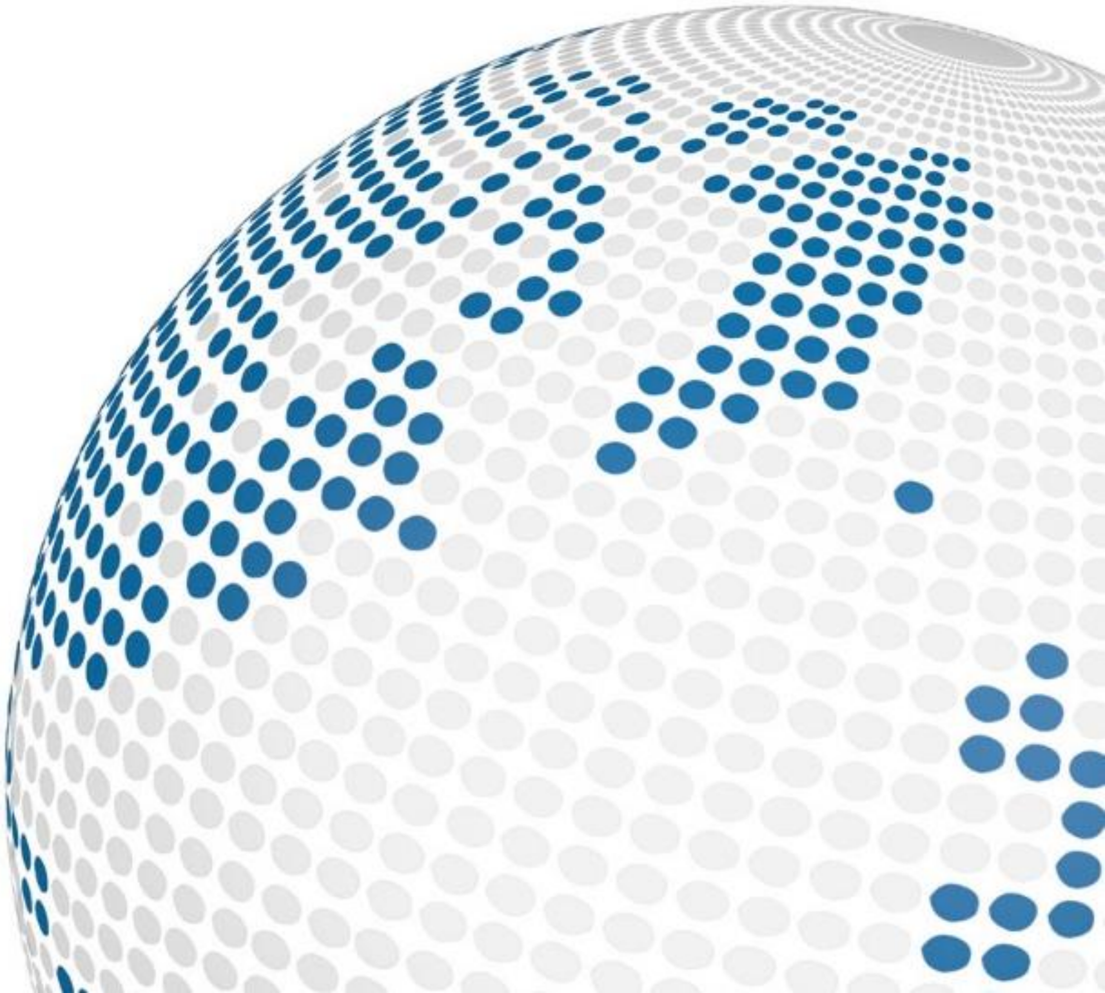


Robert Kappel

1st International SPAD Sensor Workshop
Les Diablerets, Feb 27th, 2018

Content

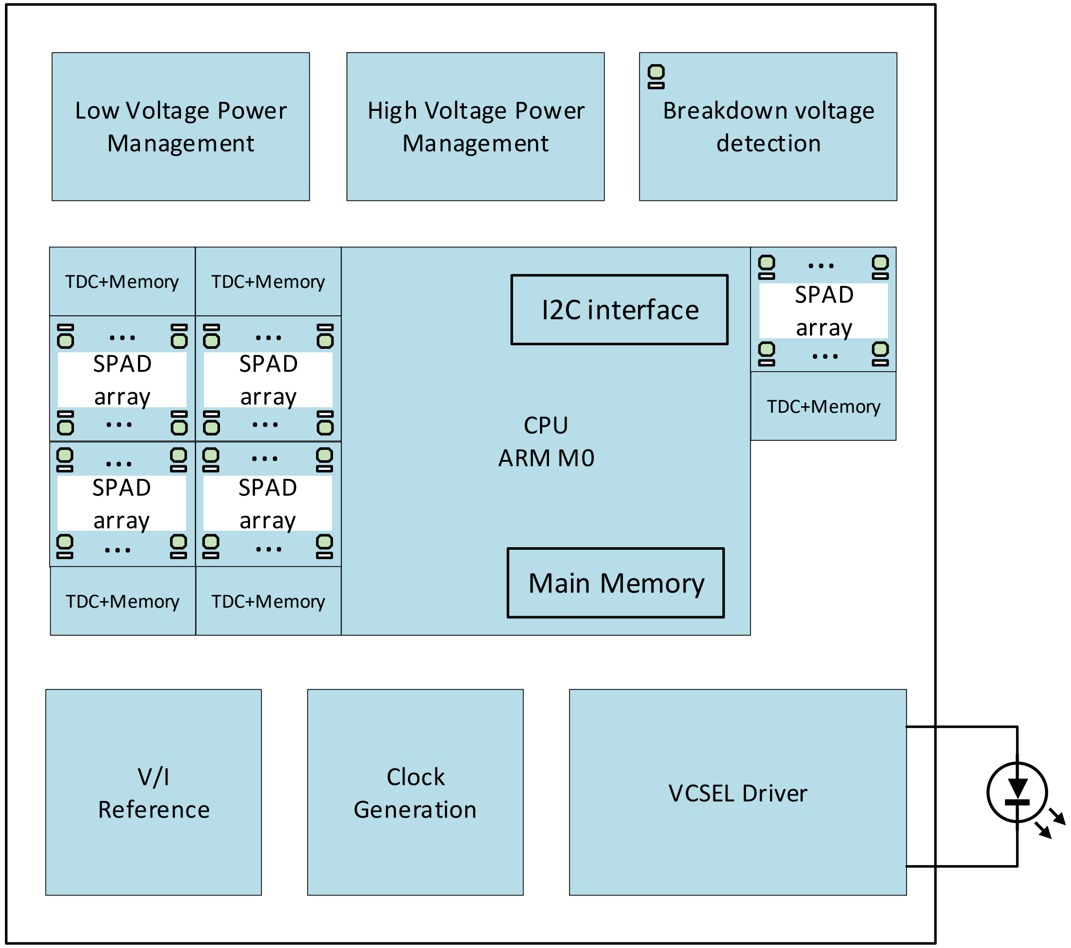
- Time of flight module
  - Silicon
    - Sensor
      - SPAD
      - Readout
      - Time to Digital Converter
      - Data storage
    - Illumination
      - VCSEL driver
- Measurement Results
  - VCSEL beam
  - Distance measurement
    - Module only, cover glass, smudge
- Demonstration video
    - Distance measurement
    - Multi object
    - Multi zone

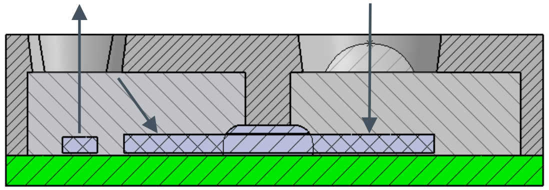
D-TOF Silicon

SPAD sensor and light emitter

- Architecture
- Characterization data

Block Diagram

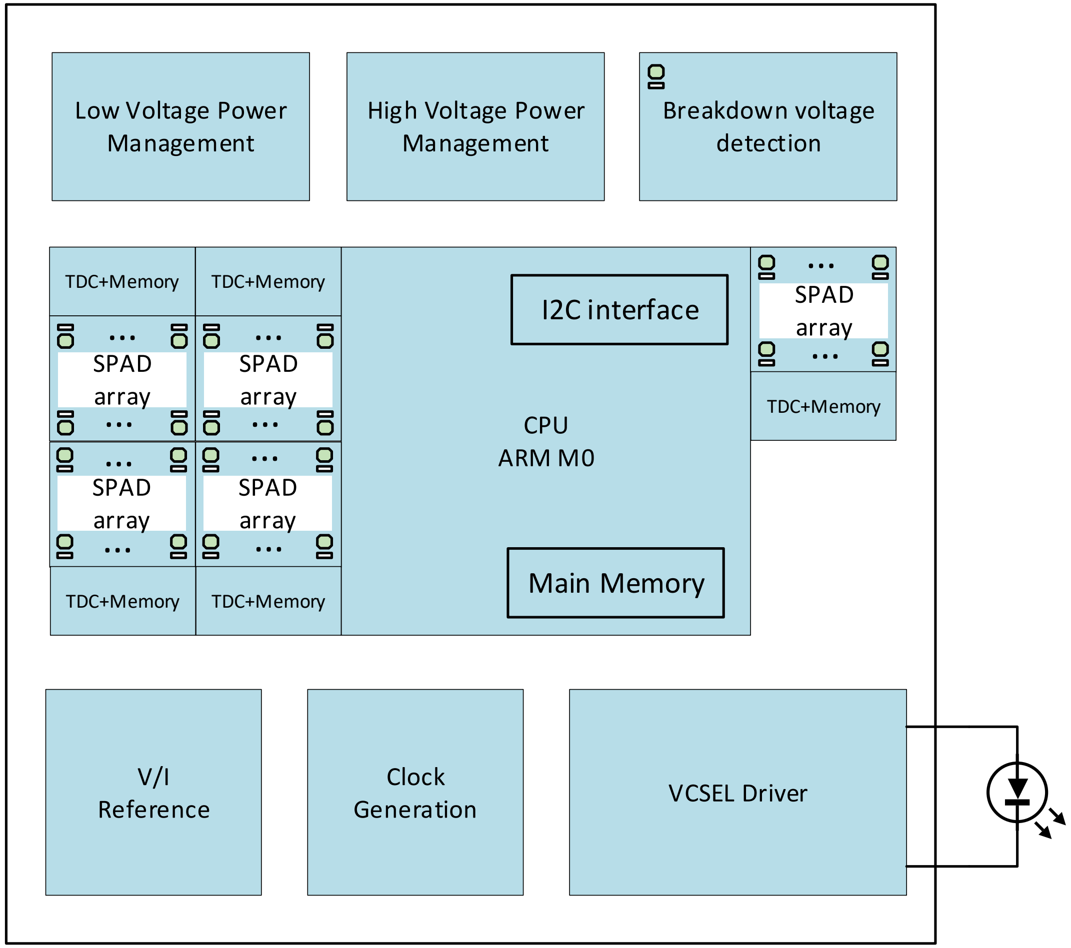


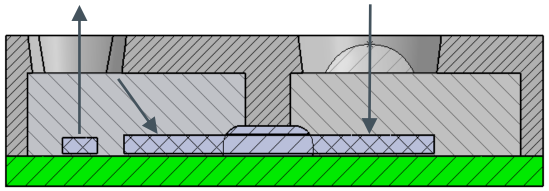


Features:

- 55nm HV process node
- Custom developed SPAD sensor
- 4 zones on main sensor array
- TDC and histogram based distance detection
- Fully integrated power management
- Cortex M0 CPU
- Sub-ns pulse generating laser driver
- Multi-mesa VCSEL diode

Block Diagram





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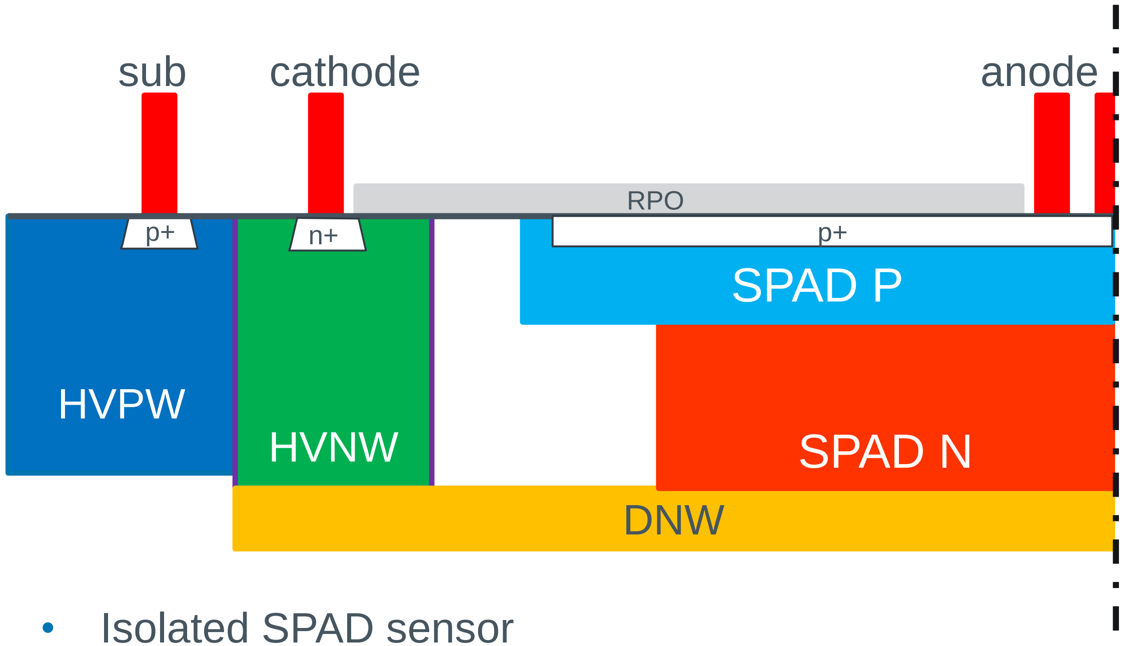
SPAD Details

SPAD cross section:



- Isolated SPAD sensor
- Modified process to generate SPAD P and SPAD N layer to reduce the breakdown voltage
  - + low DCR
  - + low jitter
  - + Low afterpulsing probability

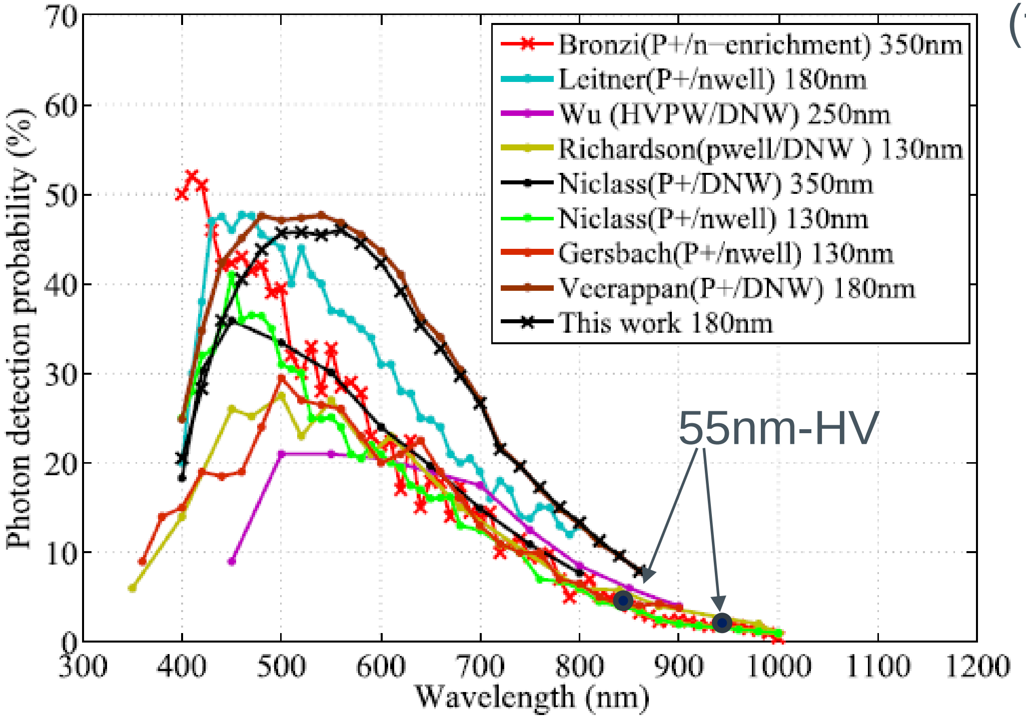
SPAD characteristics:

Parameter	Typ	Unit
BV	17.7	V
BV temperature coefficient	0.016	V/K
DCR @ 3V	0.28	cps/um²
PDP @ 940nm	1.5	%
Timing Jitter @ 940nm (FWHM)	80	ps
After pulsing probability	<0.5	%
Fill factor (SPAD + Quenching)	25	%

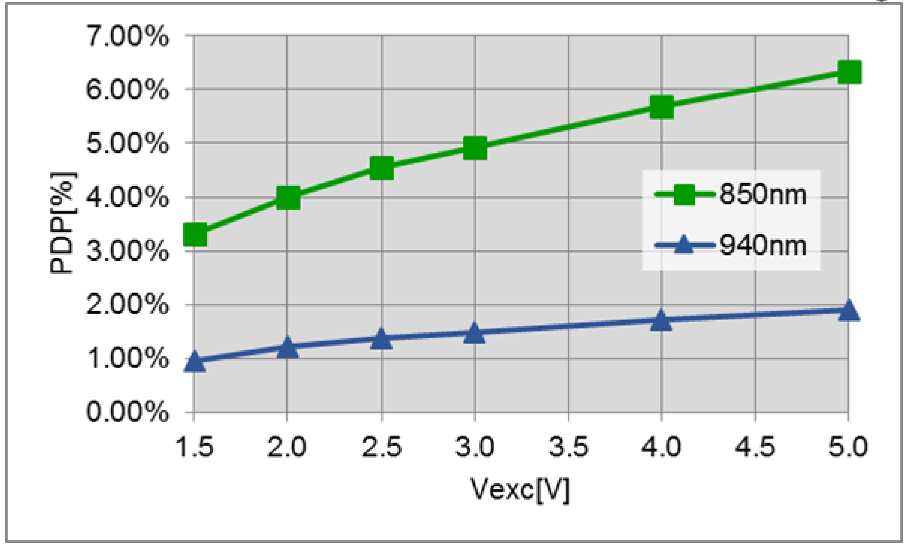
SPAD Key Characteristics

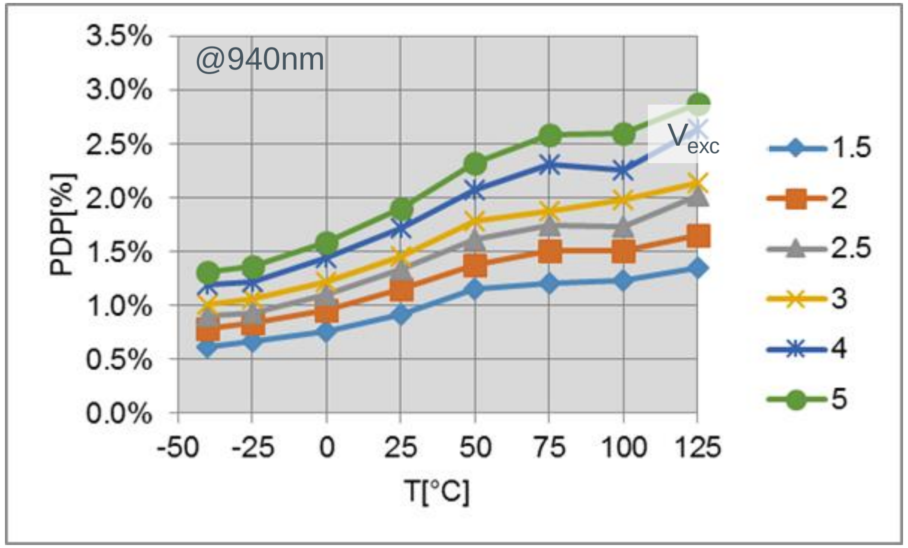
PDP=f(V_{exc}, T, λ)

- Photon detection probability PDP depends on wavelength and excess bias voltage.
- PDP increases with temperature for 940nm because bandgap decreases with temperature.
- PDP similar to state of the art.



(†)



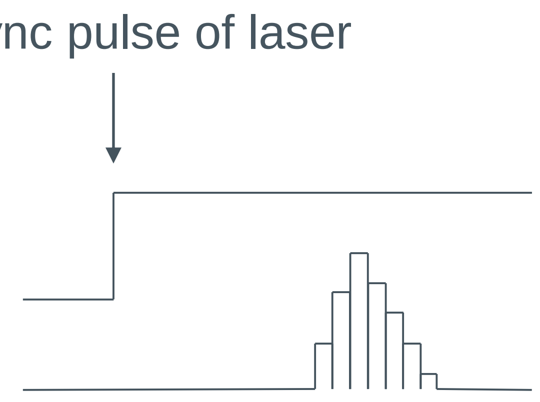


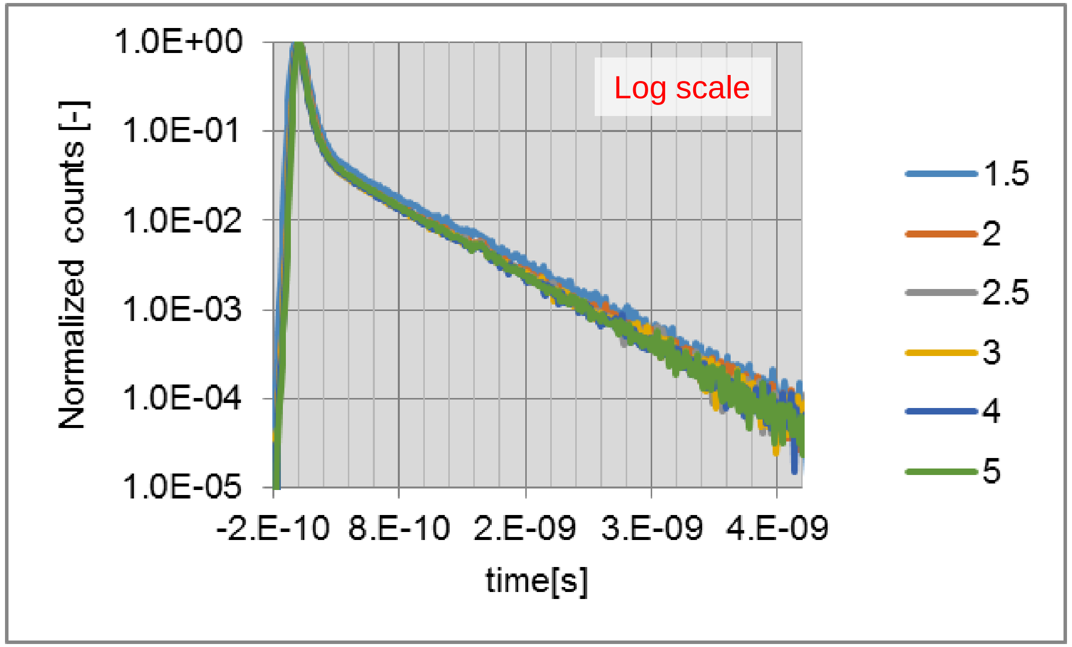
(†) Veerappan, C., Charbon, E., "*A Low Dark Count p-i-n Diode Based SPAD in CMOS Technology*," IEEE Trans. Electron Devices 63(1), 65–71 (2016).

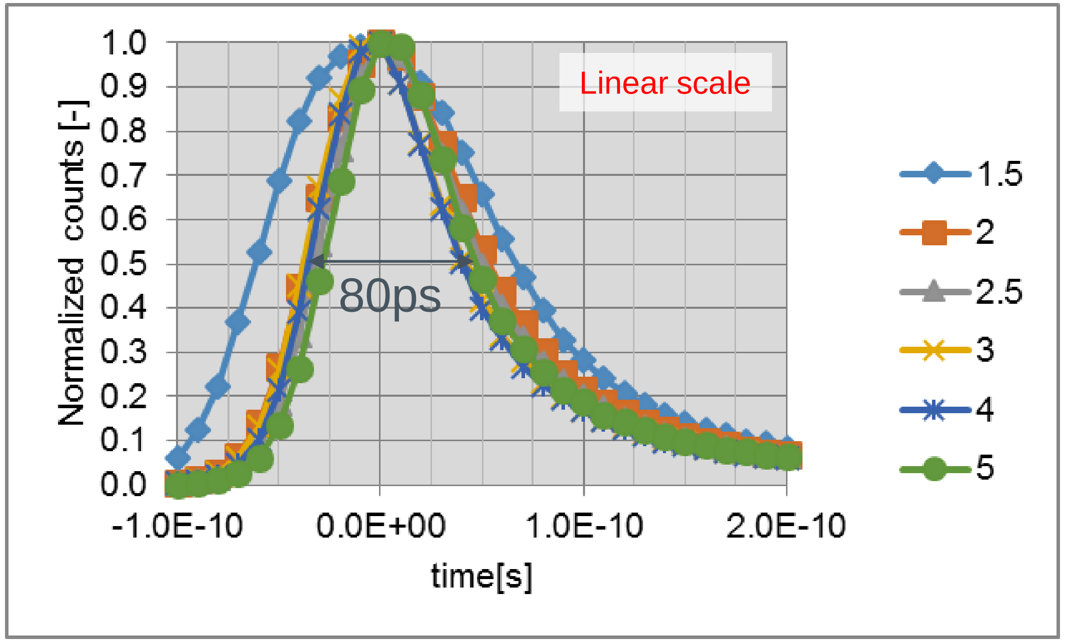
SPAD Key Characteristics

Timing Jitter @940nm

- The full width half maximum (FWHM) of the timing jitter decreases with excess bias voltage.
- The jitter tail is hardly impacted by the excess bias voltage.
- The FWHM at 3V excess bias voltage is 80ps including the jitter from the Laser source (42ps).

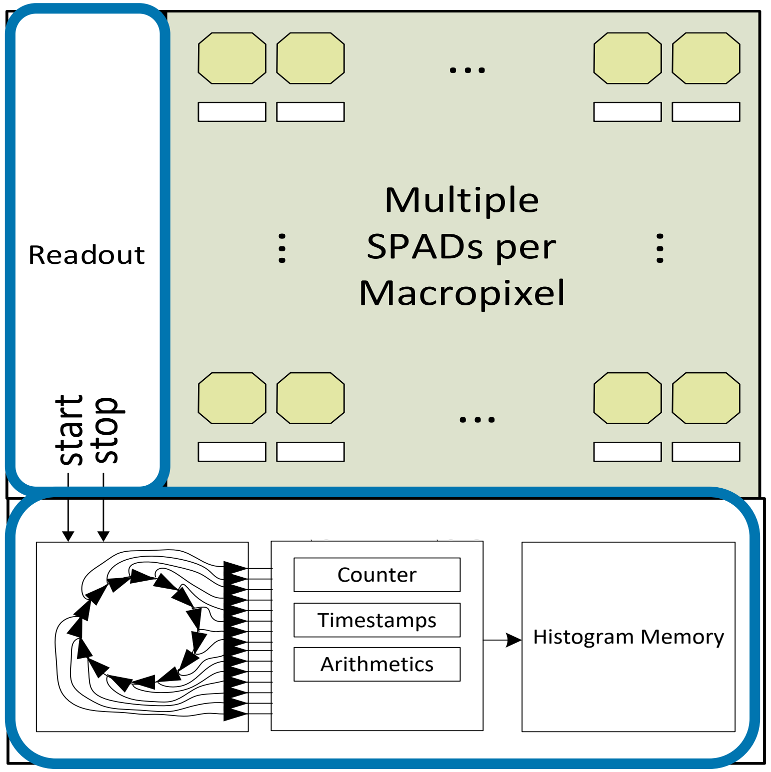






Distance Measurement

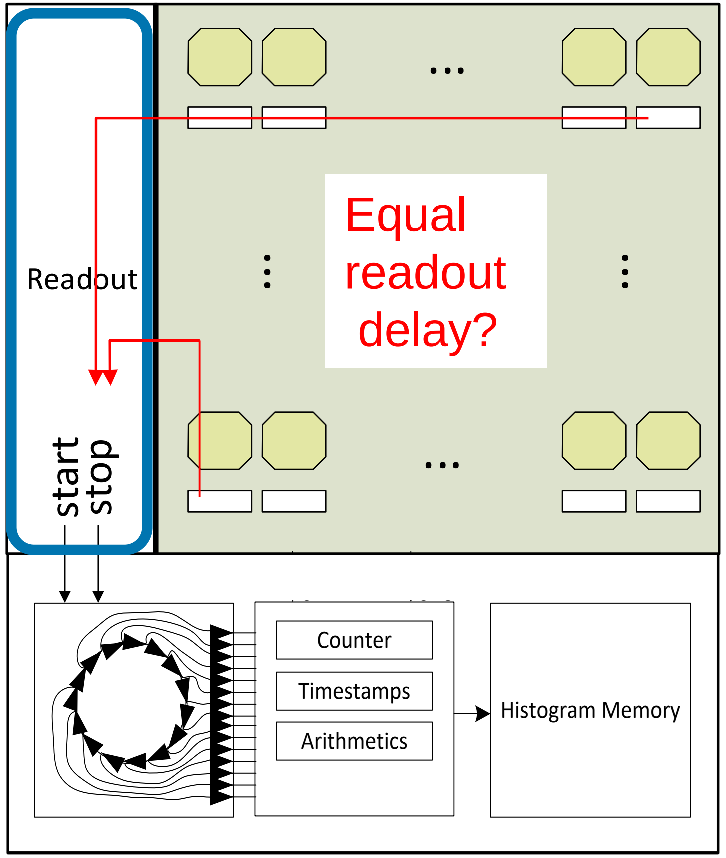
Readout and Time-to-Digital converter

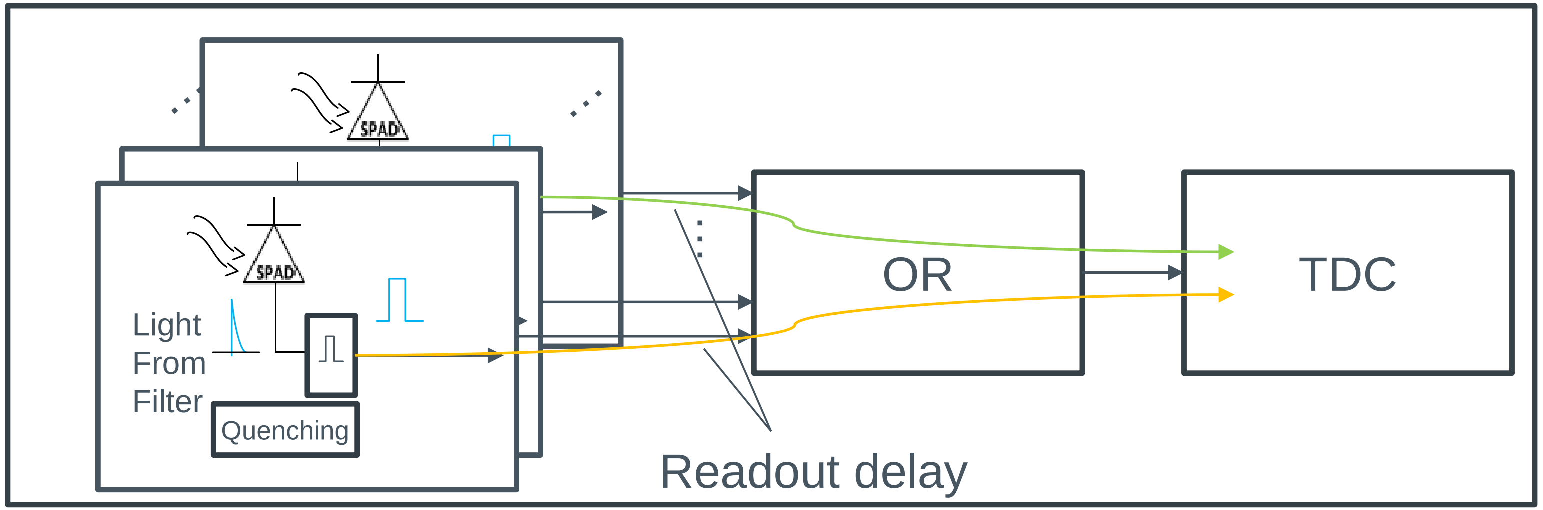


- SPAD readout circuitry
- Symmetrical digital gates
- TDC principle
- TDC architecture
- Distance processing and calibration
- Histogram storage

Sensor Readout

Overview



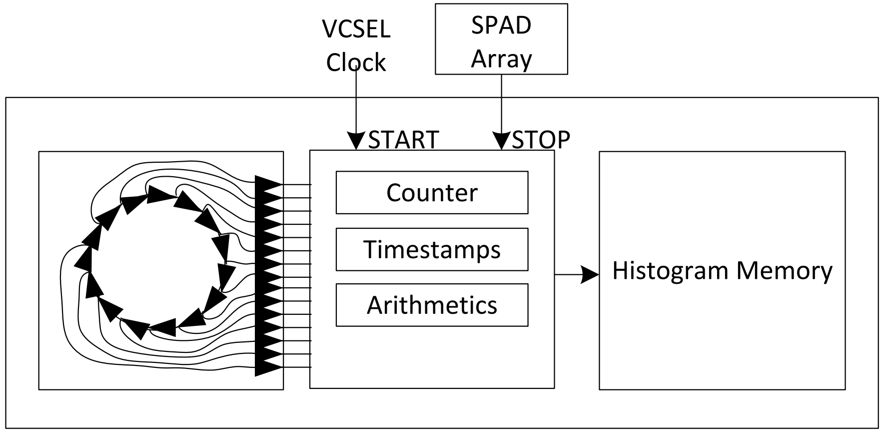


- Pulse shaper to generate a narrow event pulse independent on SPAD deadtime
- Multiple SPADs to be combined to a single TDC channel by using an OR-Tree
- Readout time must be equal from each SPAD to the TDC

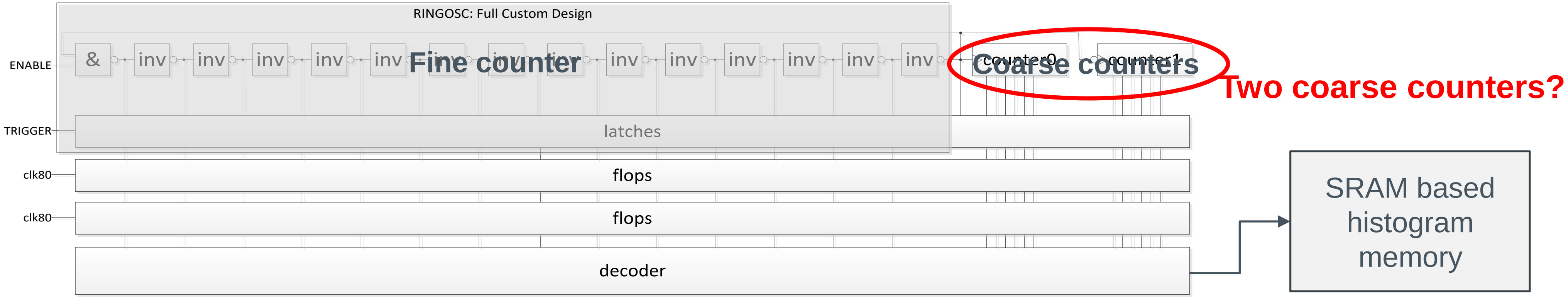
Time to Digital Converter

Overview

Time resolving unit of sensor:



TDC core architecture:

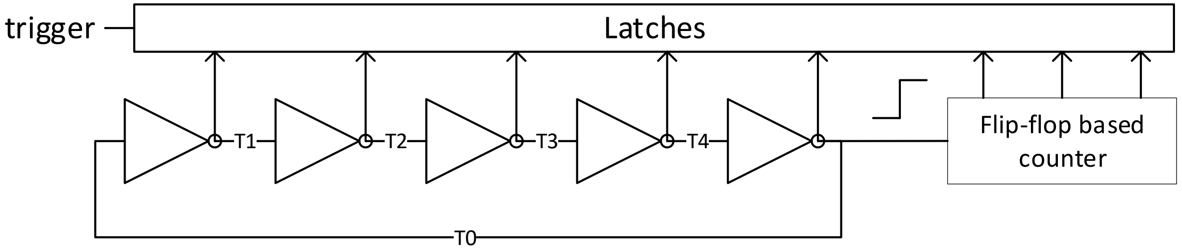


Free running ring oscillator with flip-flop based overflow counter and latches

- Fine Counter:
  - LSB represents propagation delay of inverting cell (~50ps)
- Coarse Counter:
  - Flip-flop based counter detecting overflow of fine counter
- Latch:
  - To store the actual state of the counter on-the-fly without disturbing oscillation
- Decoder: decode
  - Combines fine- and coarse- counter value to a timestamp
- Data is stored in SRAM based histogram memory
  - » Counter value represent address to be incremented

TDC Principle I

Simplified Example



T0	T1	T2	T3	T4	Fine Counter	coarse counter 0
0	1	0	1	1	8	0
0	1	0	1	0	9	0
1	1	0	1	0	0	0
1	0	0	1	0	1	0
1	0	1	1	0	2	0
1	0	1	0	0	3	1
1	0	1	0	1	4	1
0	0	1	0	1	5	1
0	1	1	0	1	6	1
0	1	0	0	1	7	1
0	1	0	1	1	8	1
0	1	0	1	0	9	1
1	1	0	1	0	0	1
1	0	0	1	0	1	1
1	0	1	1	0	2	1
1	0	1	0	0	3	2
1	0	1	0	1	4	2
0	0	1	0	1	5	2
0	1	1	0	1	6	2

trigger1

trigger2

Setup time FF

15
16
12
13
22
23

Unsafe region

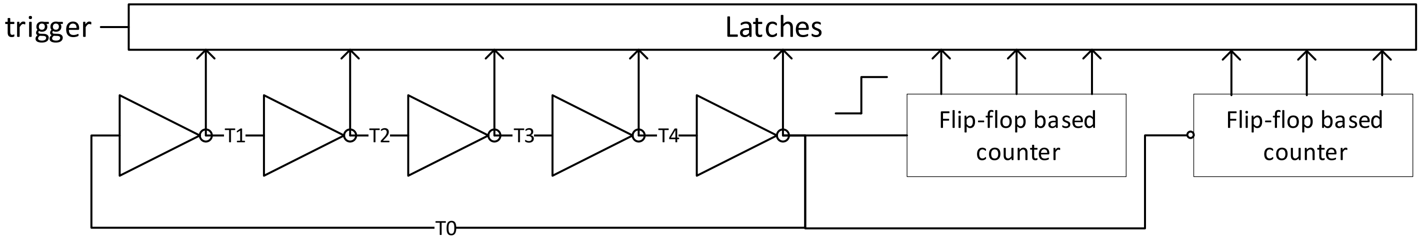
Safe region

Unsafe region

- Transparent latches immediately freeze counter values in case of an event
  - High probability that one latch of the fine counter is in metastable state
    - » could introduce 1LSB error
  - Coarse counter setup time causes delayed response on fine counter overflow
    - » Unsafe region of counter may introduce large error

TDC Principle II

Simplified Example



T0	T1	T2	T3	T4	Fine Counter
0	1	0	1	0	9
1	1	0	1	0	0
1	0	0	1	0	1
1	0	1	1	0	2
1	0	1	0	0	3
1	0	1	0	1	4
0	0	1	0	1	5
0	1	1	0	1	6
0	1	0	0	1	7
0	1	0	1	1	8
0	1	0	1	0	9
1	1	0	1	0	0
1	0	0	1	0	1
1	0	1	1	0	2
1	0	1	0	0	3
1	0	1	0	1	4
0	0	1	0	1	5
0	1	1	0	1	6
0	1	0	0	1	7

coarse counter 0	coarse counter 1
0	0
0	0(+1)
0	0(+1)
0	0(+1)
1	0(+1)
1	0(+1)
1	0
1	0
1	0
1	1
1	1
1	1(+1)
1	1(+1)
1	1(+1)
2	1(+1)
2	1(+1)
2	1
2	1
2	1

Setup time FF — 15, 16, 22, 23

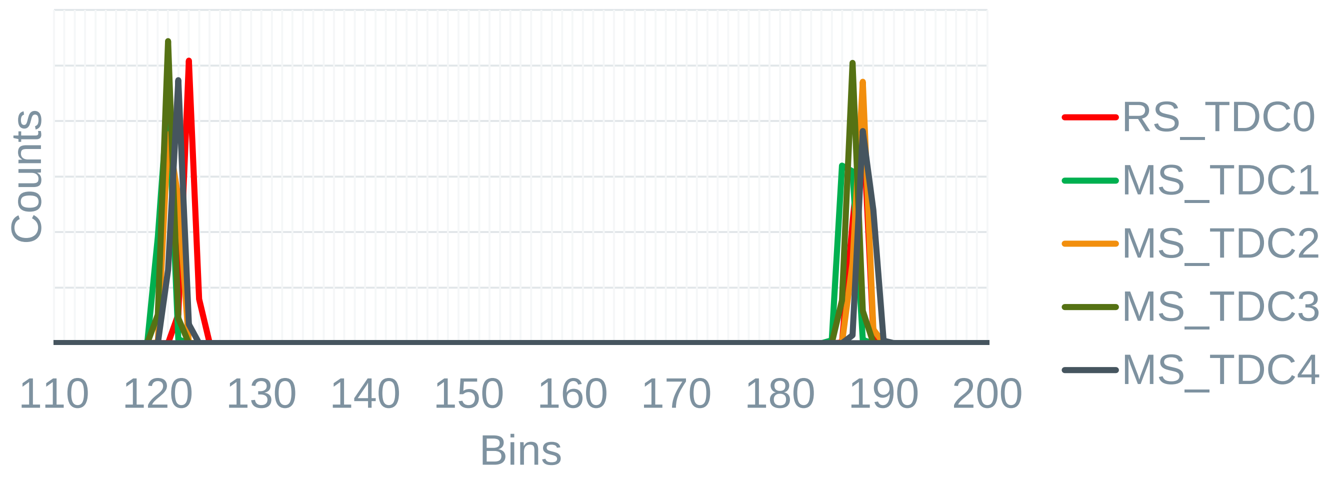
- 2 flip-flop based overflow counters with complimentary clock edge sensitivity
  - Consider only the "stable" coarse counter of a oscillation period when evaluating the latched counter value of the TDC at point in time of trigger signal
    - » Fine counter values indicates region and therefore coarse counter to be used
    - » Coarse counter value need to be corrected in certain region to cover overlap
  - Overall 1 LSB error could be introduced

How to calibrate the fine counter?

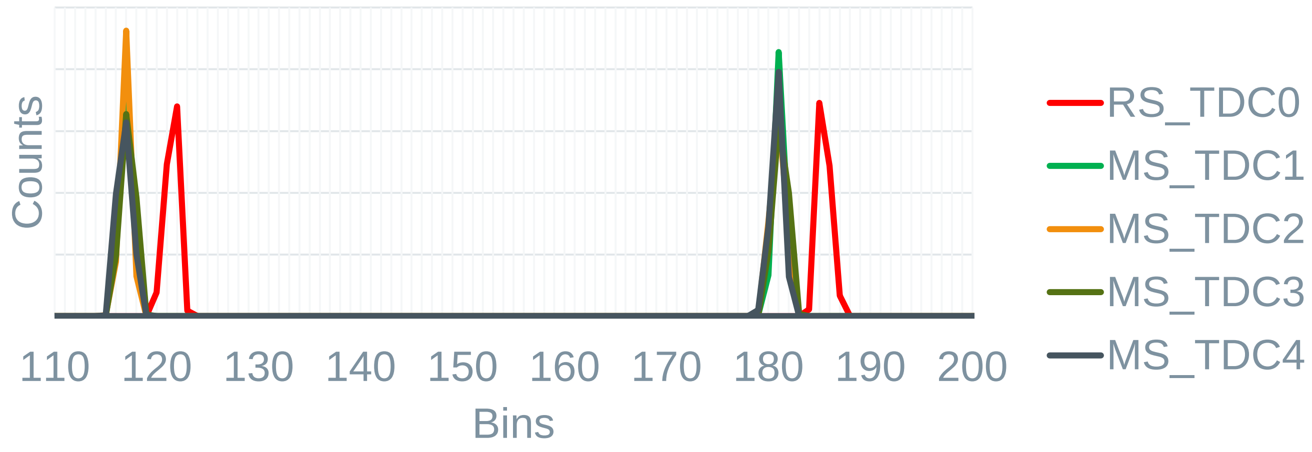
TDC Calibration

Digital Calibration Scheme

Before calibration



After calibration



- Each TDC contains one ring oscillator
  - Absolute ring oscillator speed is unknown (-50%..+100%)
  - Relative ring oscillator speed amongst each other (+-5%)
- Pure digital solution for calibration is used.
  - Each TDC is able to measure its own ring oscillator speed using the system clock as reference.
  - Correction factor can be determined for individual histograms

Illumination of scene

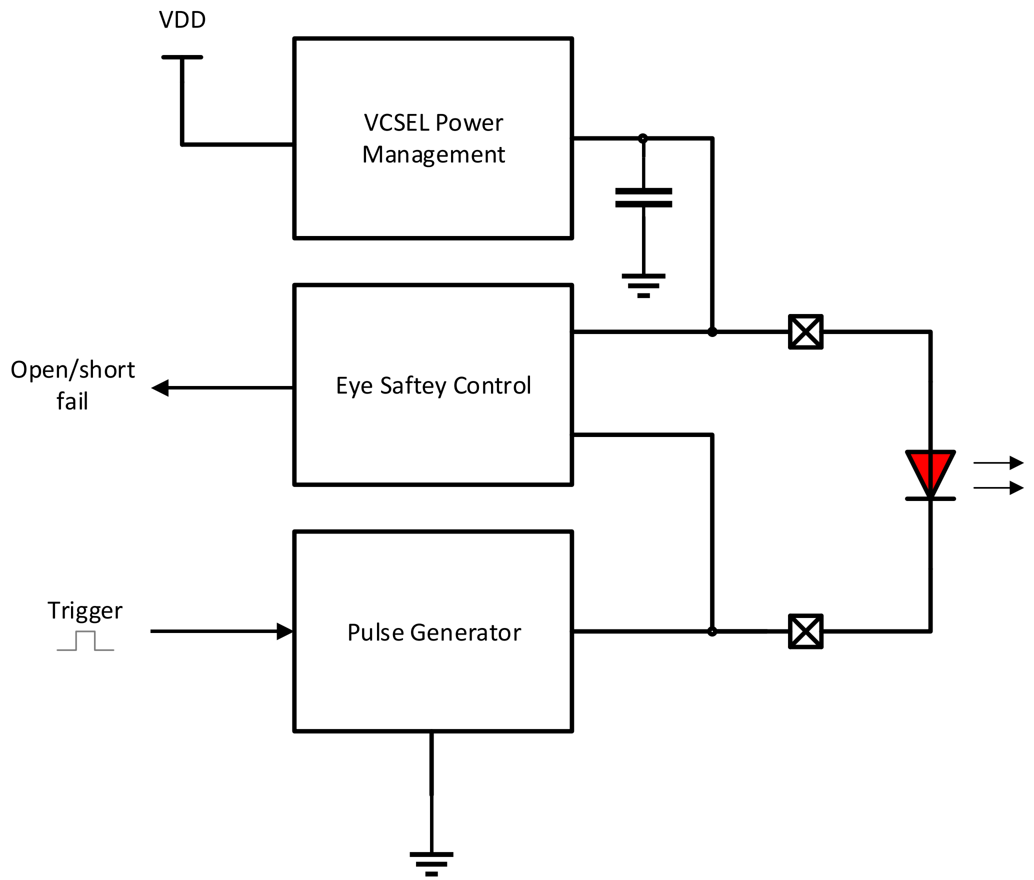
VCSEL and VCSEL Driver

- VCSEL architecture
- VCSEL driver
- Optical characteristics of beam

VCSEL Driver

Key Performance Parameter

Block Diagram



- Charge Pump
  - Decouples min supply voltage from VCSEL forward voltage
  - Small loop of VCSEL current (low EMI)
  - No extra PMOS switch required
- Eye Safety Control
  - Short on VCSEL anode/cathode
  - Current limitation through VCSEL (charge pump)
  - Clock failure detection (charge pump)
- Pulse generation
  - Pulse width: ~300ps FWHM
  - High peak current

- Laser safety: Class 1

System performance

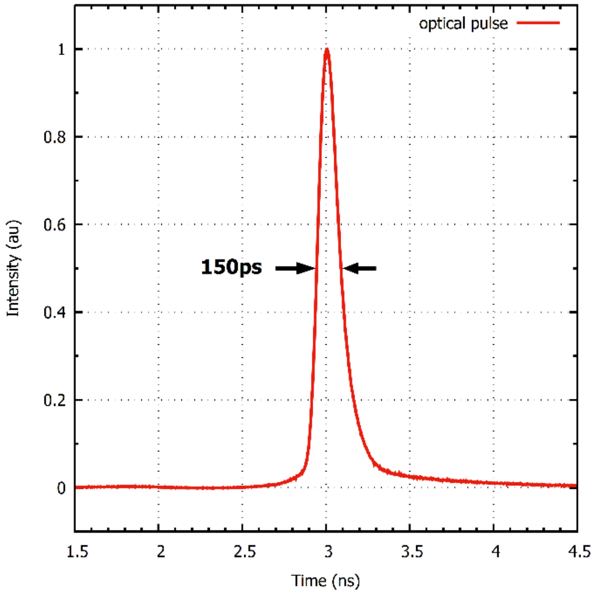
Measurement results

- VCSEL pulse
- Crosstalk and smudge removal
- High accuracy, Independent of object color
- Demonstration video

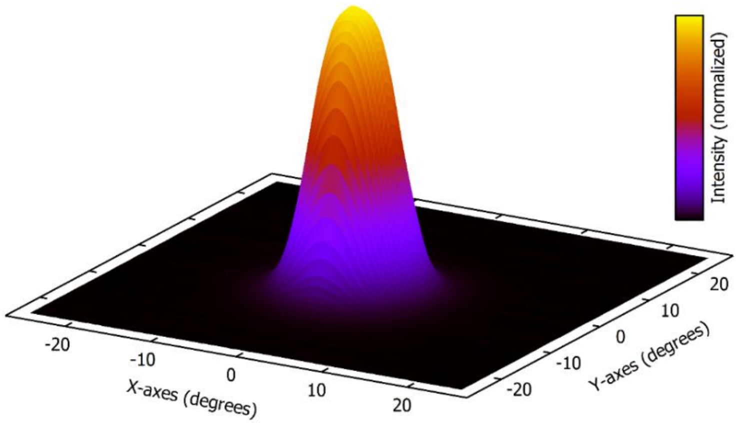
VCSEL beam measurements

Sensing is life.

Optical pulse



VCSEL emission profile



Characteristics:

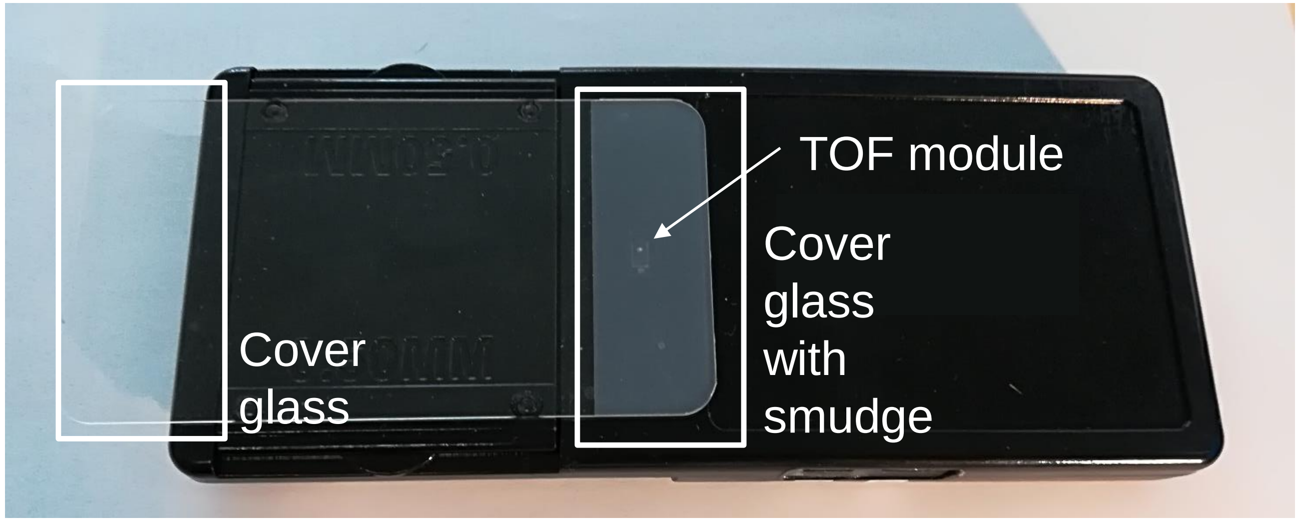
- Optical pulse 150ps
- FOI 15° (1/e²)

- Sub-ns pulsed mode allows increased peak power

Measurement conditions

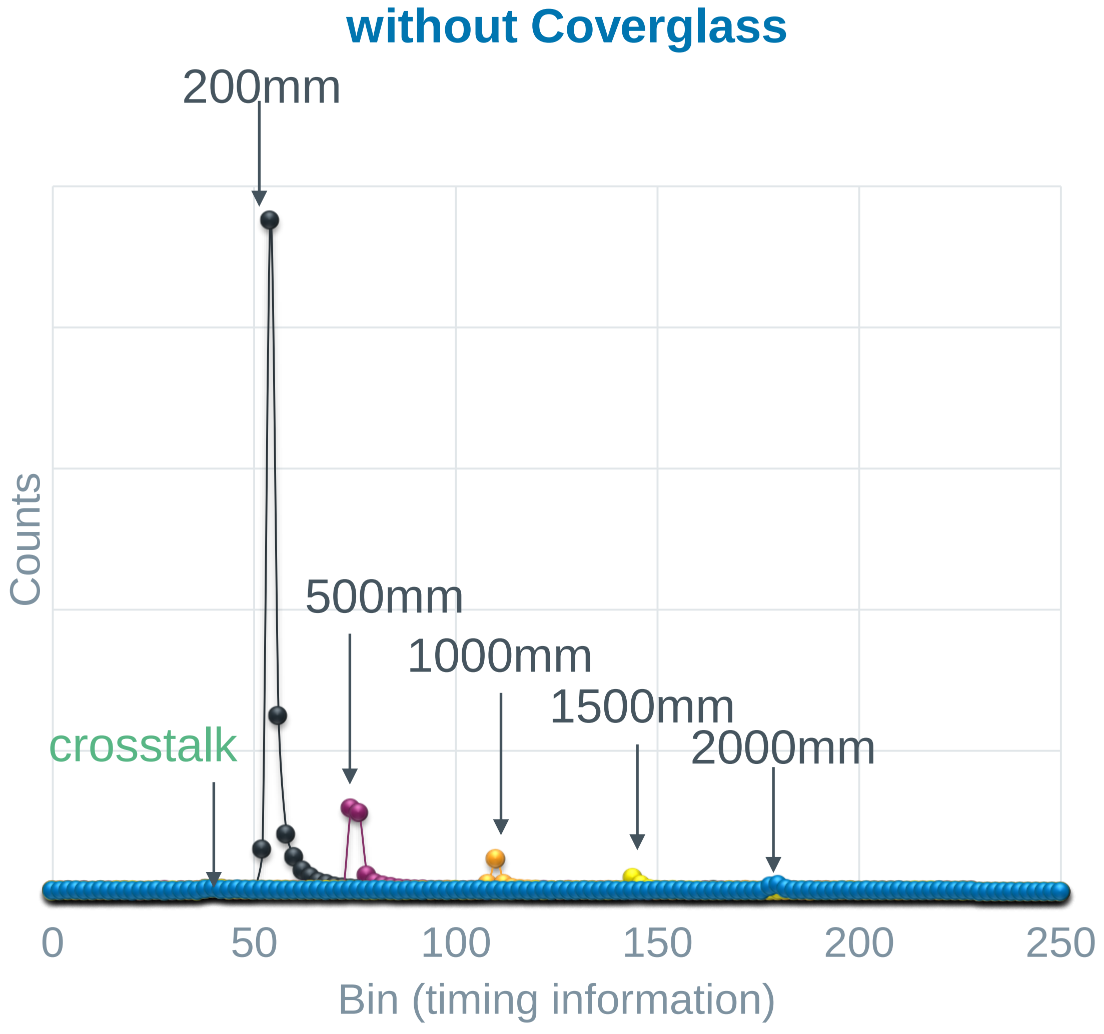
200mm to 3000mm in 50mm steps

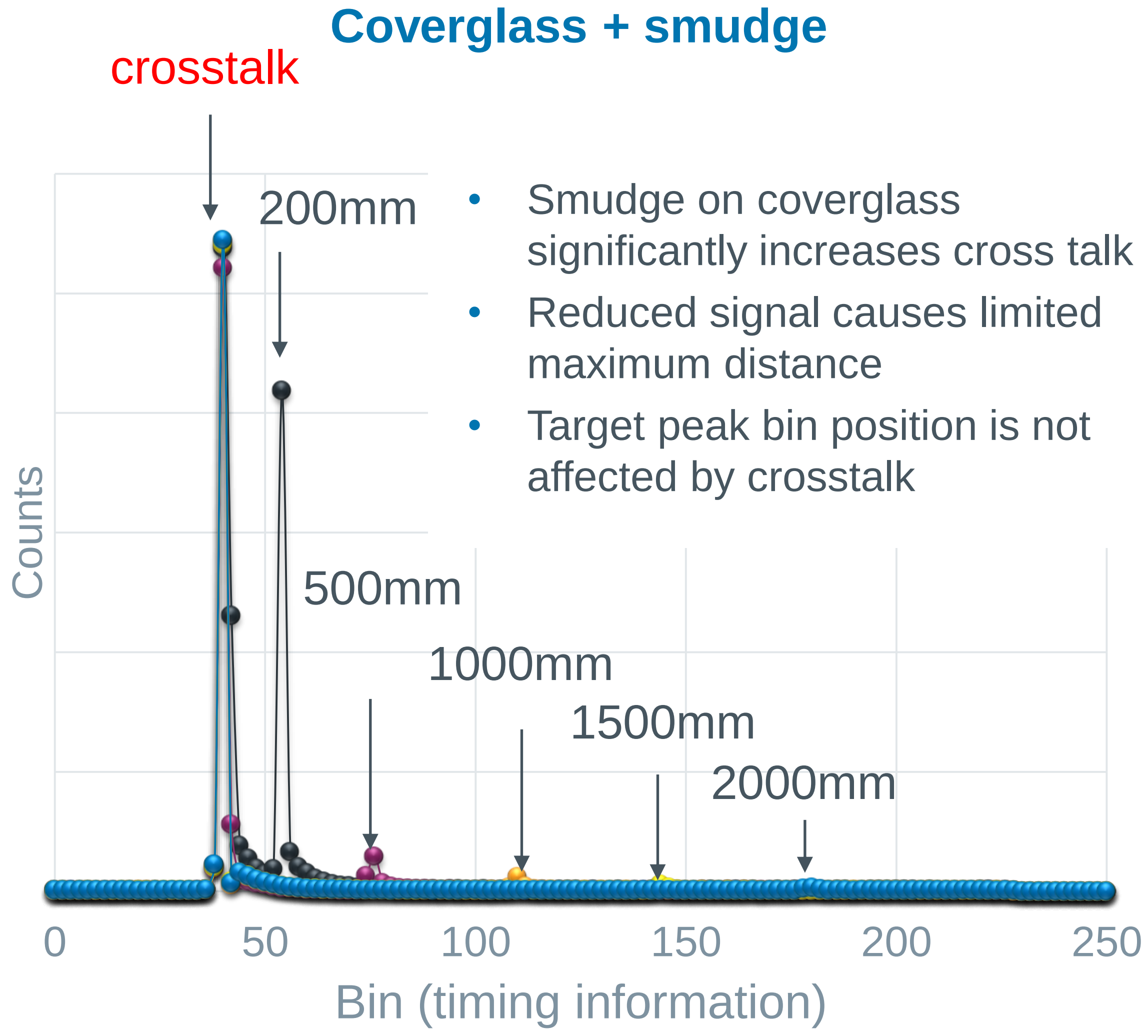
- Target size:
  - 1m x 1m
  - 50fps/800 000 integration cycles
- Color:
  - 90% white
  - 18% grey
  - 4% black
- Conditions:
  - Without cover glass
  - With cover glass (85% transmissivity)
  - Cover glass + smudge
- Background light on the target:
  - 0.2klux
  - 1klux
  - 5klux
  - 10klux
  - 20klux



Histogram comparison

without background light

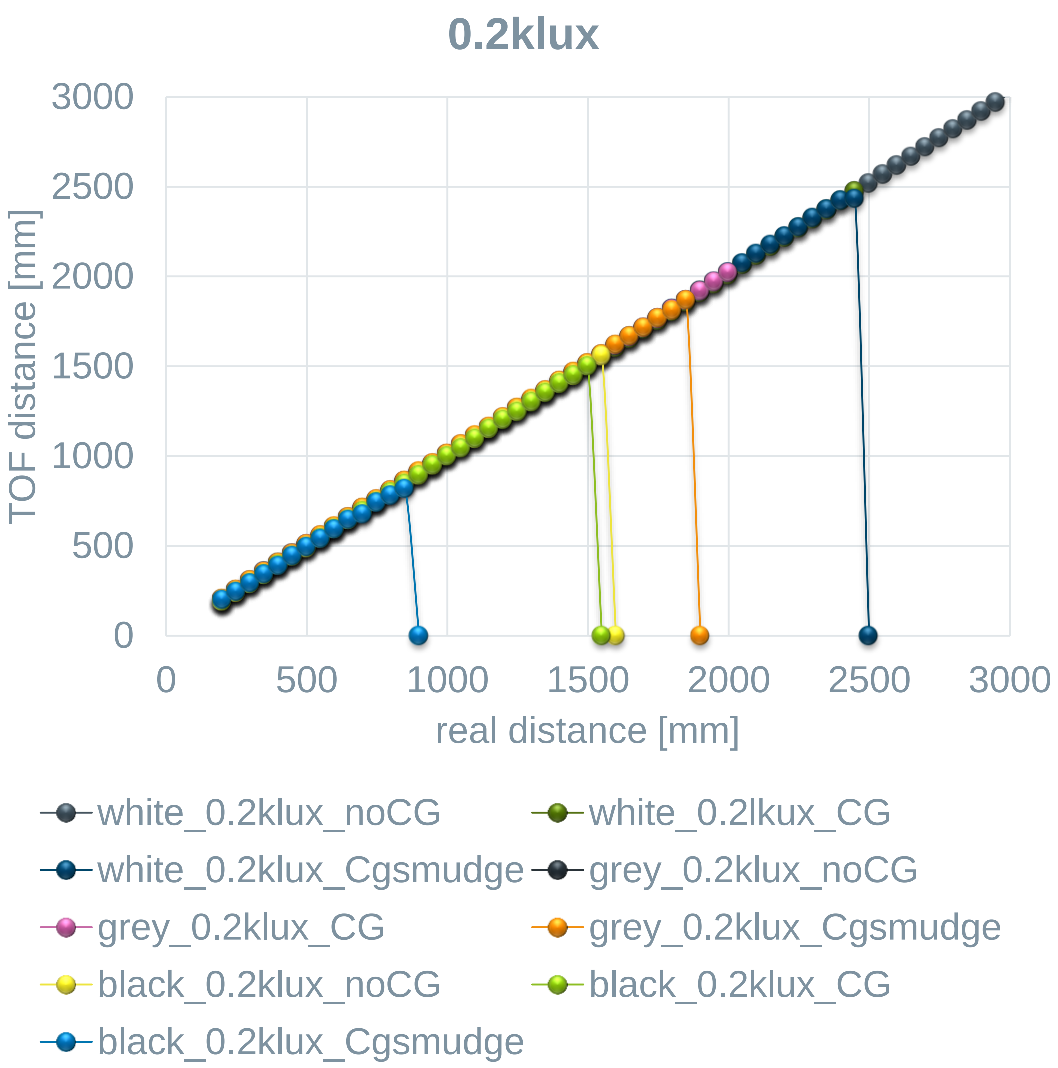


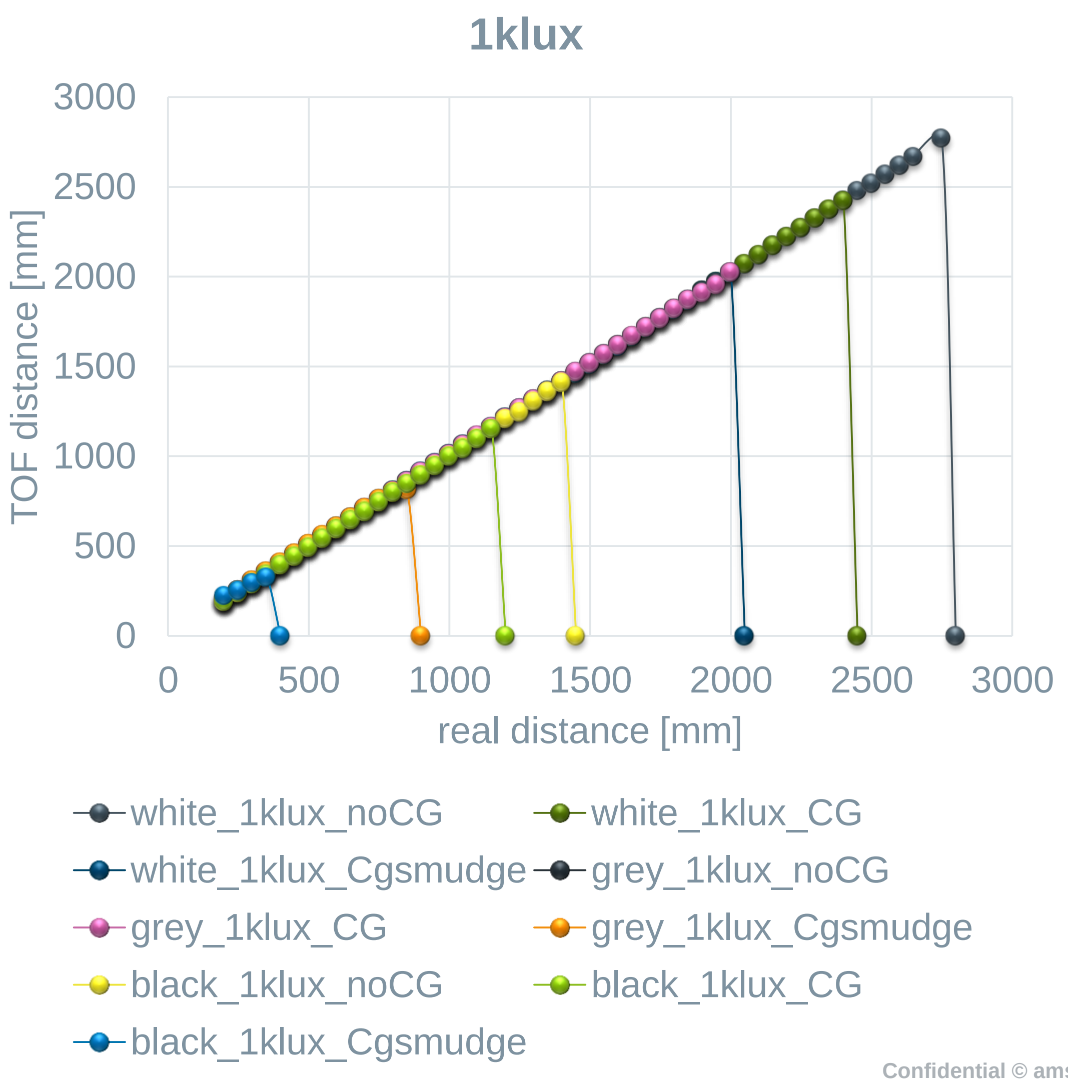


- Smudge on coverglass significantly increases cross talk
- Reduced signal causes limited maximum distance
- Target peak bin position is not affected by crosstalk

Distance measurement I

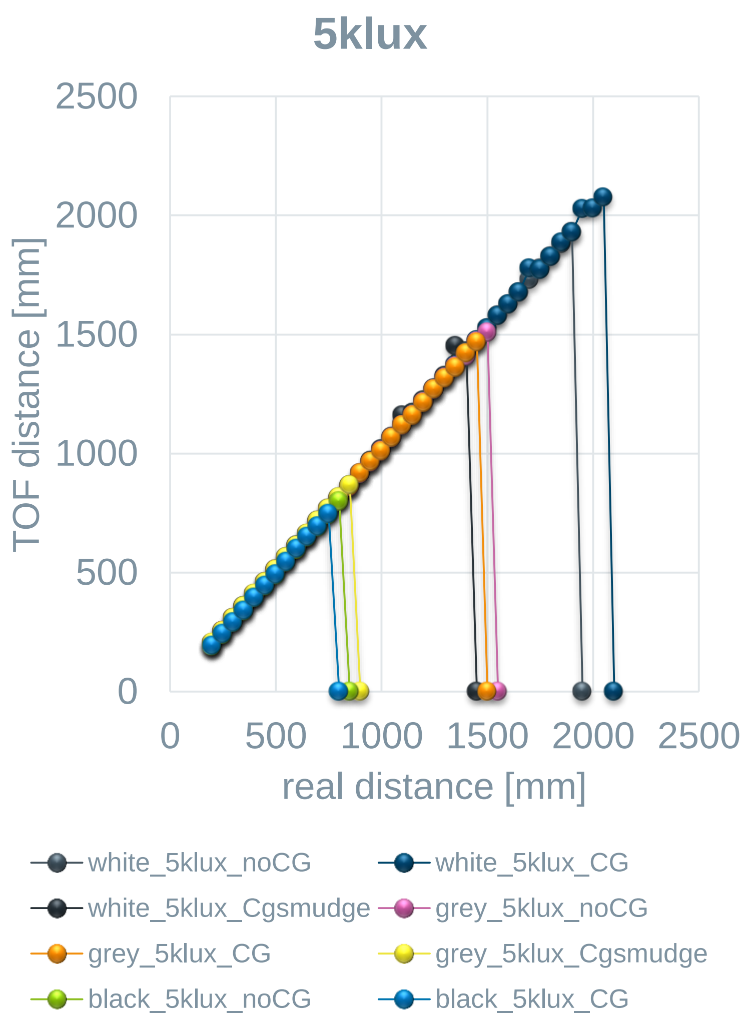
0.2klux and 1klux

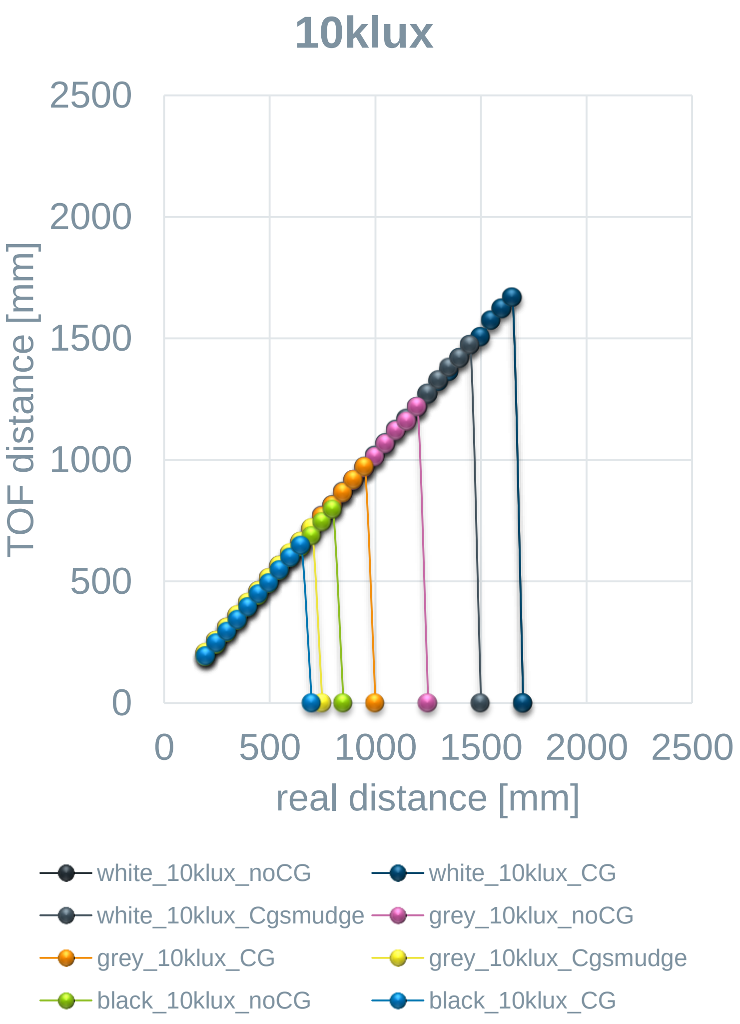


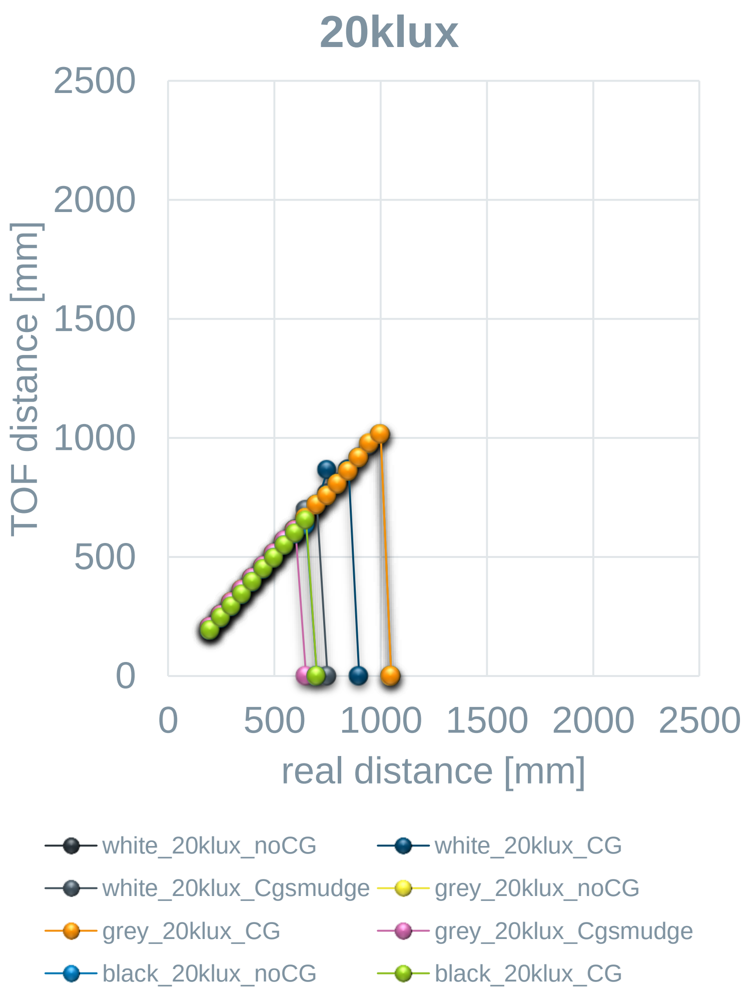


Distance measurement II

5klux, 10klux and 20klux







Conclusion

- Direct Time of Flight system using robust histogram-based architecture
- Custom developed SPAD sensor in 55nmHV process node
- Symmetrical readout structure
- Free running TDC architecture
  - Digital calibration scheme
  - Double differential measurement principle
- 940nm VCSEL laser in pulsed operation
  - Laser class 1 safe
- Distance measurement over a wide range of conditions
  - Distance measurement insensitive to crosstalk and smudge
- Multi-object
- Multi-zone capability

Thank you!

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