Industrialised SPADs in Deep-submicron CMOS technology

Sara Pellegrini

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Outline of Presentation

- ST SPAD history
- 40nm technology introduction
- SPAD device description
- Pixel and readout
- Characterization results
- Conclusions

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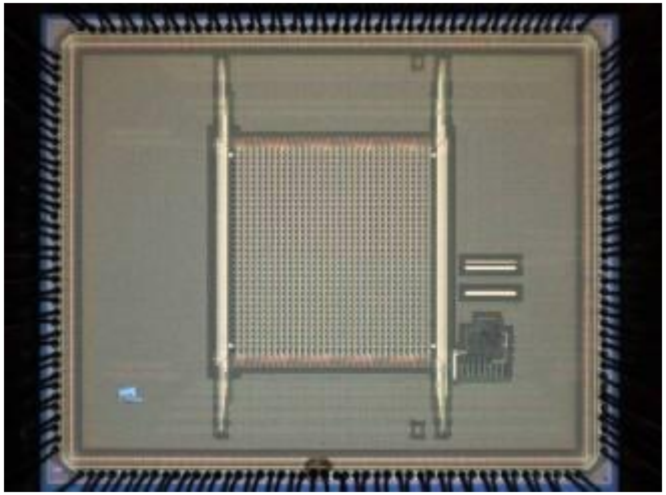
ST SPAD development history

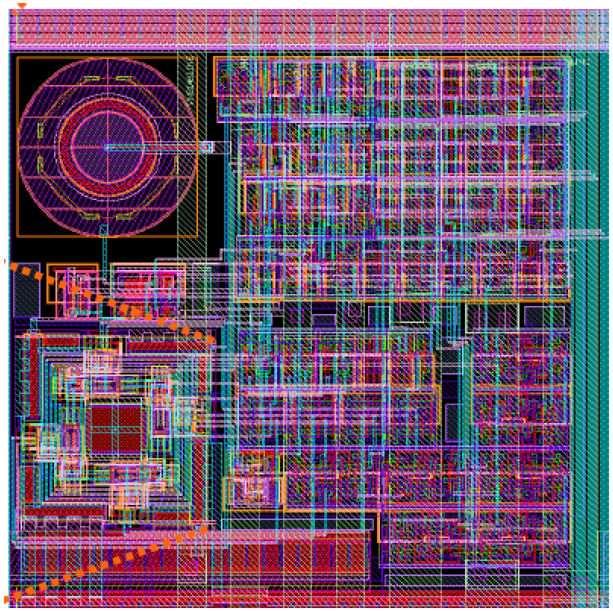
MEGAFRAME FP6 for Biomedical

- start: jun’06 - end: apr’10
- 32x32 SPAD array
- In pixel TDC

MEGAFRAME 32x32 imager - 2009

- 50 μm pitch, 6 μm diameter SPAD, 1.2% fill-factor
- 50ps time resolution, 50ns full-scale, 7-bit intensity dynamic range





- SPAD fill factor very low and digital area very high

[Richardson, CICC, 2009]

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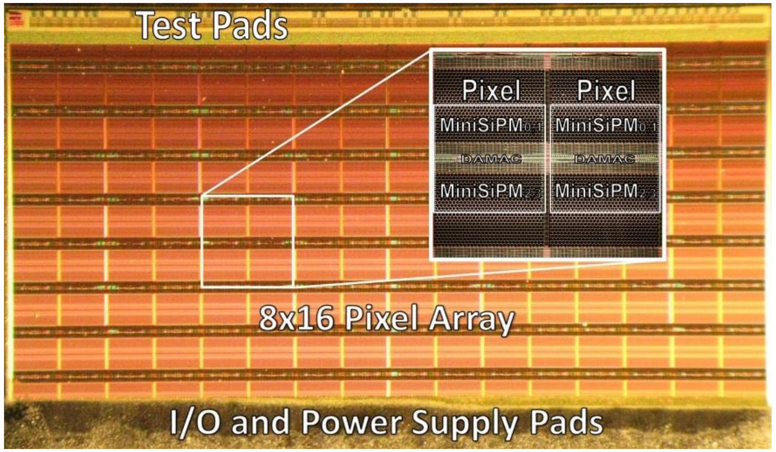
→ stand alone SPAD pixel

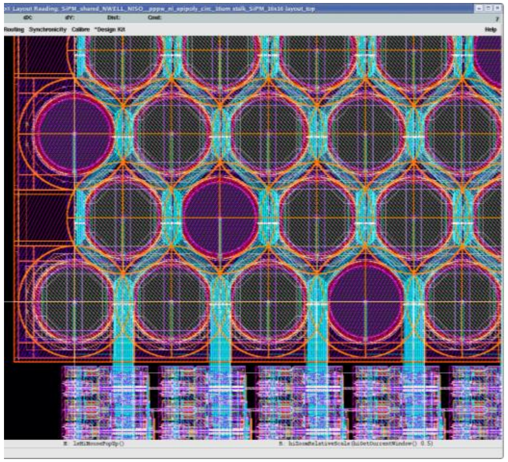
SPADnet sensor PET/MRI

- start: jul’10 - end: dec’14
- High fill factor, 2 x embedded TDCs per pixel
- 16 x 16 SiPM pixel array, 180 SPADs/pixel Energy detection & time sampling

SPADnet

- 19.3 μm pitch, 64% fill-factor
- All logic is pushed at the edge of the array





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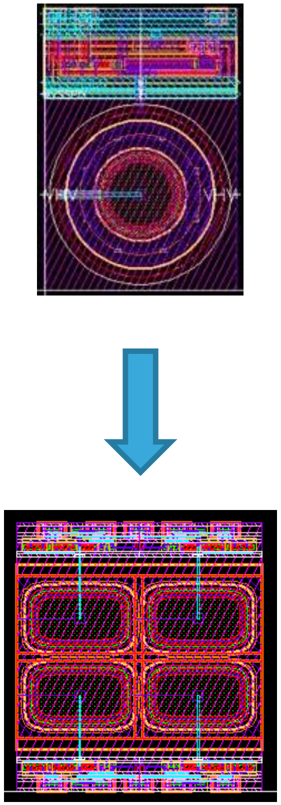
  Energy detection & time sampling

→ well sharing SPAD pixel

ST industrial 130nm CMOS SPAD - 2013

- Pixel only containing passive quenching circuit



Metric	IMG175SPAD Value (@ 60°C) [SPIE Photon Counting Conference]
VHV0	13.8V
DCR Median	~1k cps
PDP	3.1% (850nm)
Fill Factor	6% → 21.6%
Pulse Width	25ns
Max Count Rate	37Mcps
Jitter	120ps FWHM, 870ps FW1%M
Current per Pulse	0.08pA
After-Pulsing	<0.1%
Cross-Talk	<0.01% (isolated SPAD)

ST SPAD developments history

MEGAFRAME for Biomedical

SIXTH PROGR

- start: jun'06 - end: apr'10
- 32x32 SPAD array
- In pixel TDC

→ stand alone SPAD pixel

Flight Sense

SPADnet sensor PET/MRI

SEVENTH FRAMEWORK PROGRAMME

- start: jul'10 - end: dec'14
- High fill factor, 2 x embedded TDCs per pixel
- 16 x 16 SiPM pixel arra, 180 spads/pixel Energy detection & time sampling

→ well sharing SPAD pixel

POLIS technology pilot line for sensors

- start: jan'14 - end: dec'18

→ 40nm SPAD pixel and 3D stacked technology

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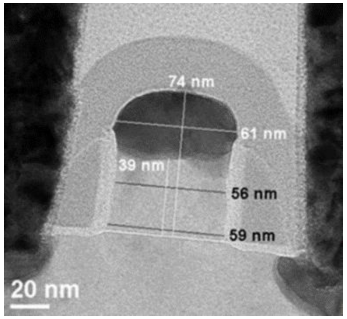
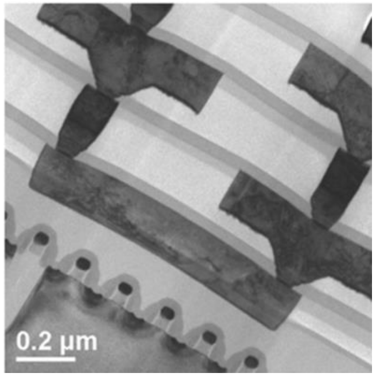
CMOS 40nm : Technology Overview



- CMOS45LP main features:
  - Low Power (LP): 85% reduction vs 130nm CMOS
  - Cell density : 80% reduction in gate area vs 130nm CMOS
  - Vdd=1.1V : improved dynamic power
  - Copper metal & Ultra Low K dielectric (k=2.55) :

    reduces parasitic capacitance, enabling faster switching speeds and lower heat dissipation
  - Technology available since 2010 - Source : STCrolles 12”



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40nm benefits vs 130nm

- Higher digital integration
  - Smaller die size
  - Higher computing power → more complex FW
  - Quicker operations
  - Potential to increase SPAD array size
  - Enables parallel read-out options
  - Wider memory size
- Low-power digital operation
- Opens the door for further technology roadmap
  - 3D stack
  - DTI/CDTI

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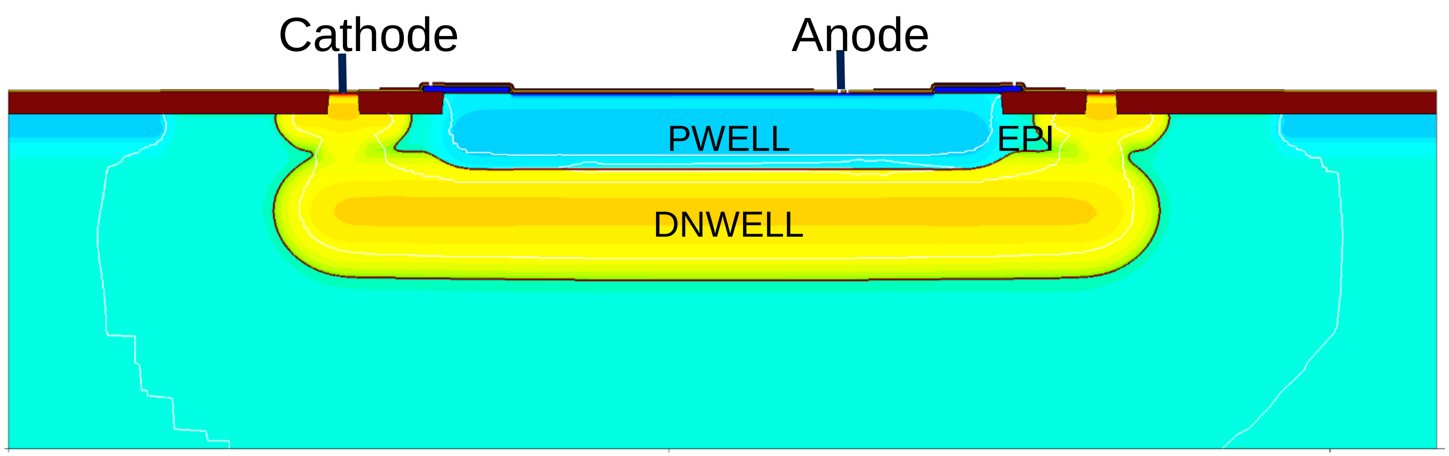
SPAD device description

- Doping Profile
  - PWELL and DNWELL define the avalanche region
  - EPI guard ring avoids edge breakdown



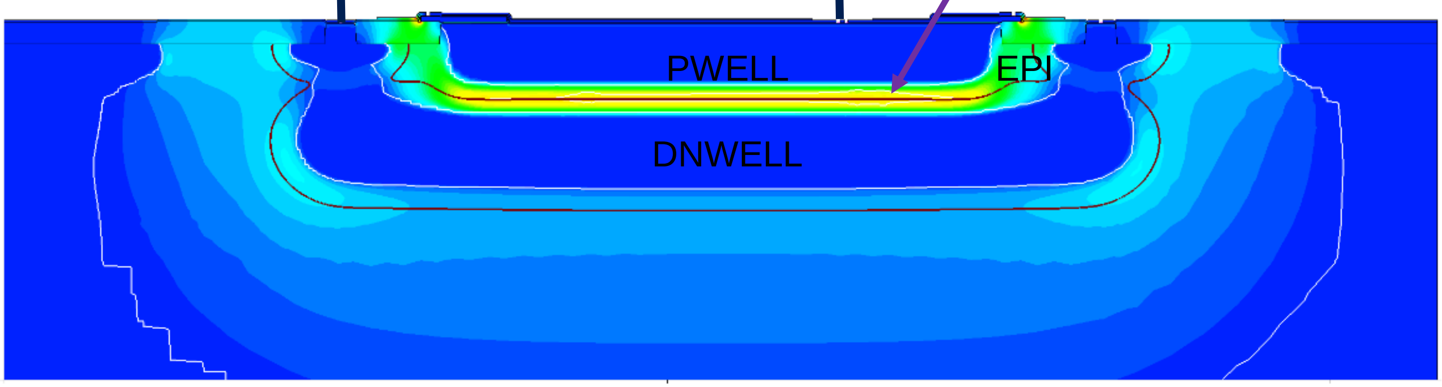
SPAD device description

- Electric Field Profile at breakdown

The **high field avalanche region** is confined between PWELL and DNWELL

V breakdown

0V

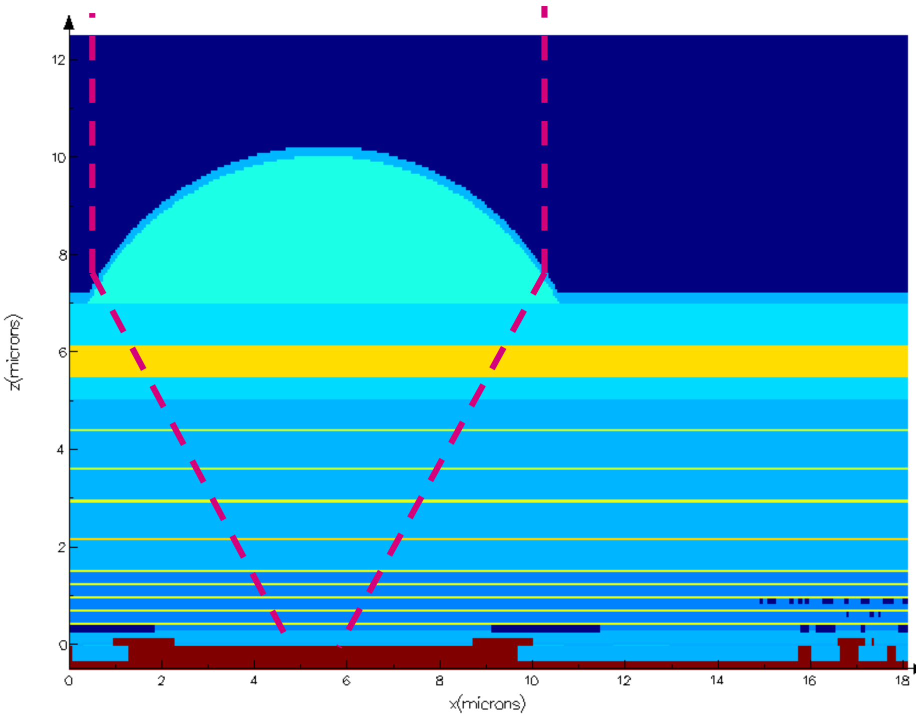


SPADs microlenses

- Several metal layers →

  Tall optical stack

- Large microlenses focus the beam back onto the SPAD



SPADs microlenses

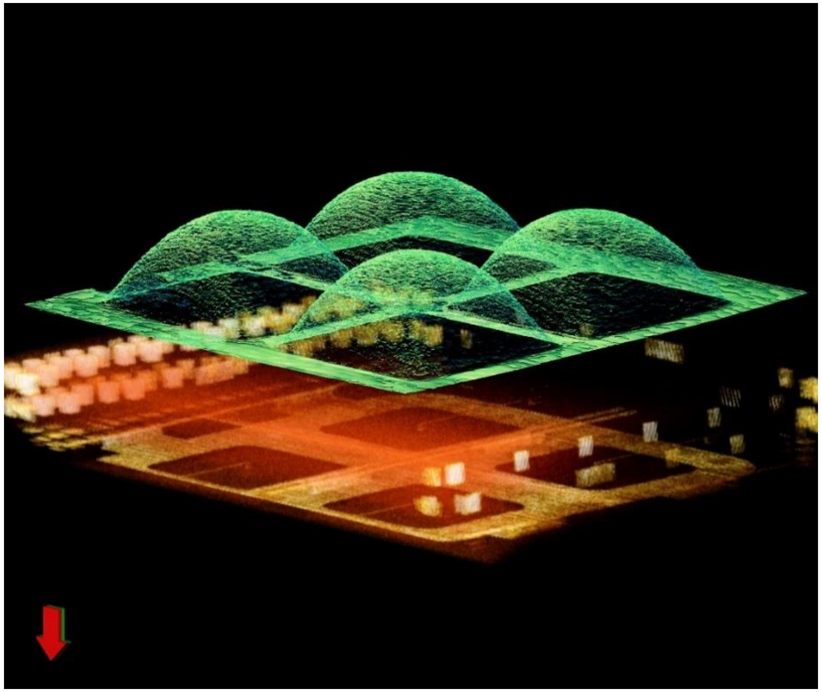
- Several metal layers →

  Tall optical stack

- Large microlenses focus the beam back onto the SPAD

- 3D FIB-SEM characterization

- **SPAD fill factor > 70%**



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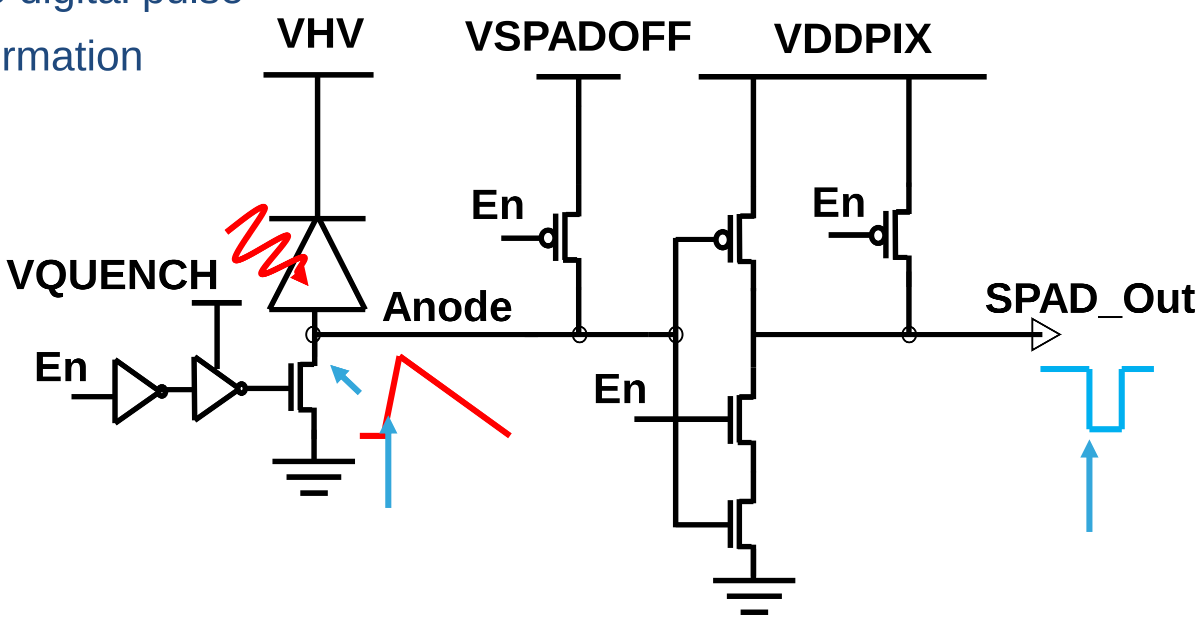
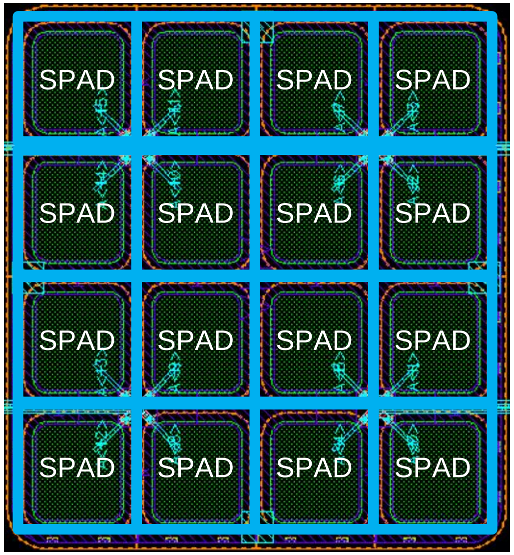
SPAD pixel quenching

- Passive quenching with disabling
  - Bias is beyond breakdown
  - Tunable quench resistance
  - Individual SPADs can be disabled
  - The output is a true digital pulse containing timing information



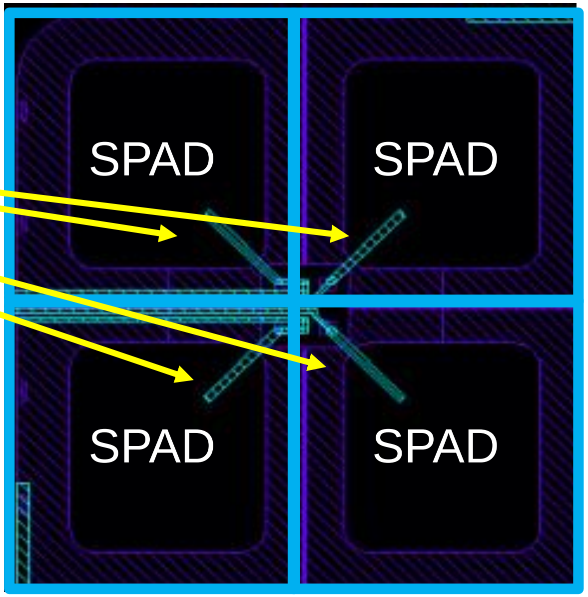
SPAD pixel

- 4 x 4 SPADs sharing NWELL



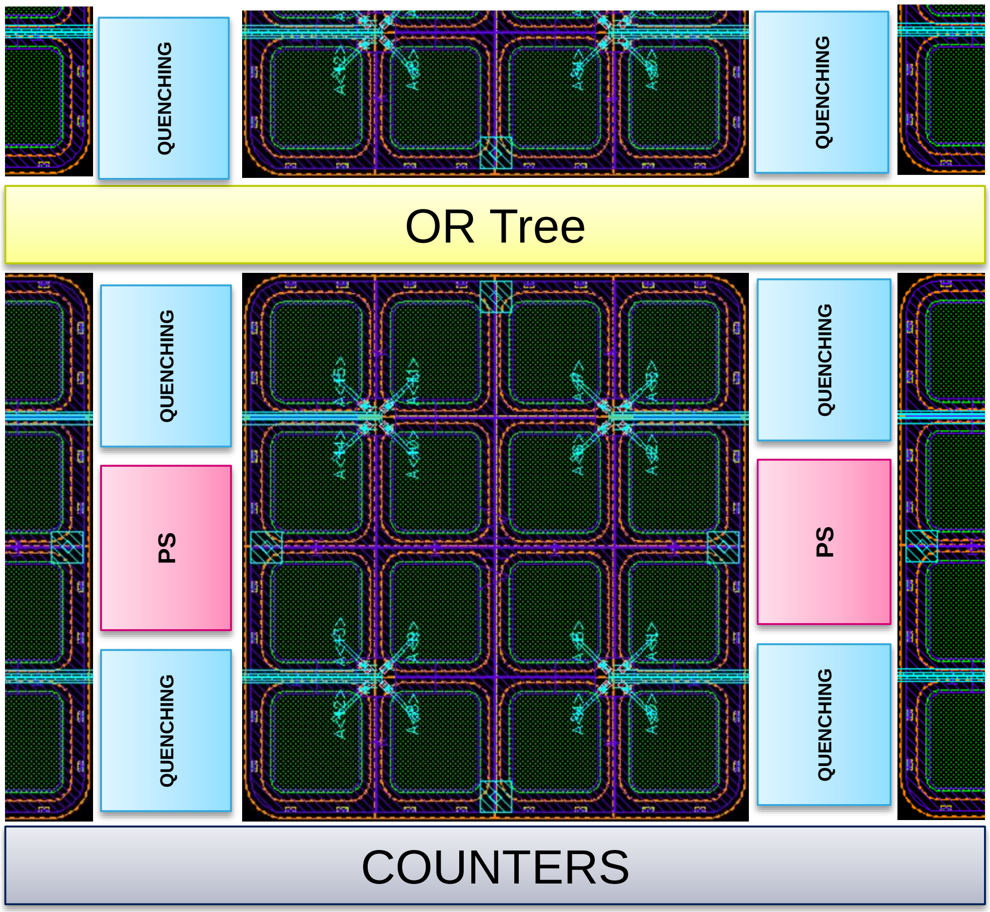
SPAD pixel

- 4 x 4 SPADs sharing NWELL
- Anode design
  - Optimal matched track length
  - Angular symmetry
  - Best optical transmission



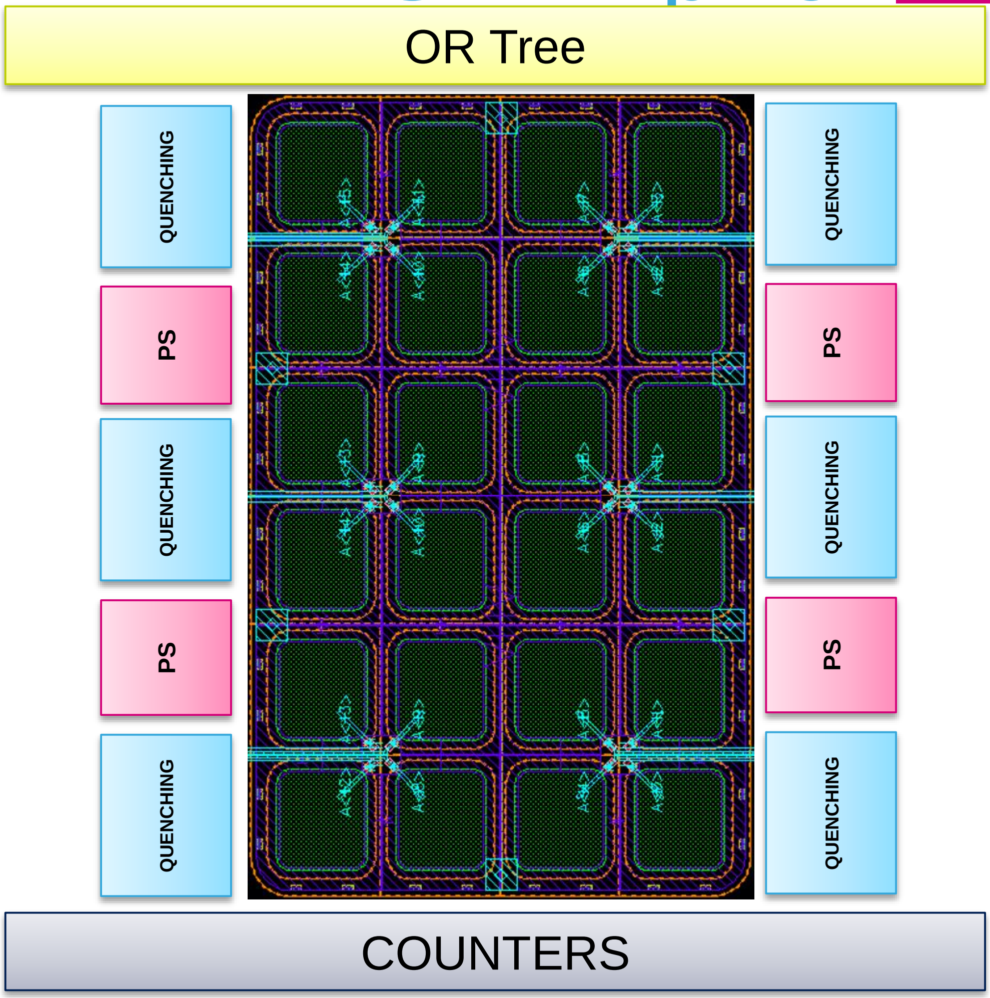
SPAD pixel

- 4 x 4 SPADs sharing NWELL
- Logic
  - individual quenching and enabling
  - pulse shaper
  - OR tree
  - counters
- Well sharing between neighbouring pixel is possible



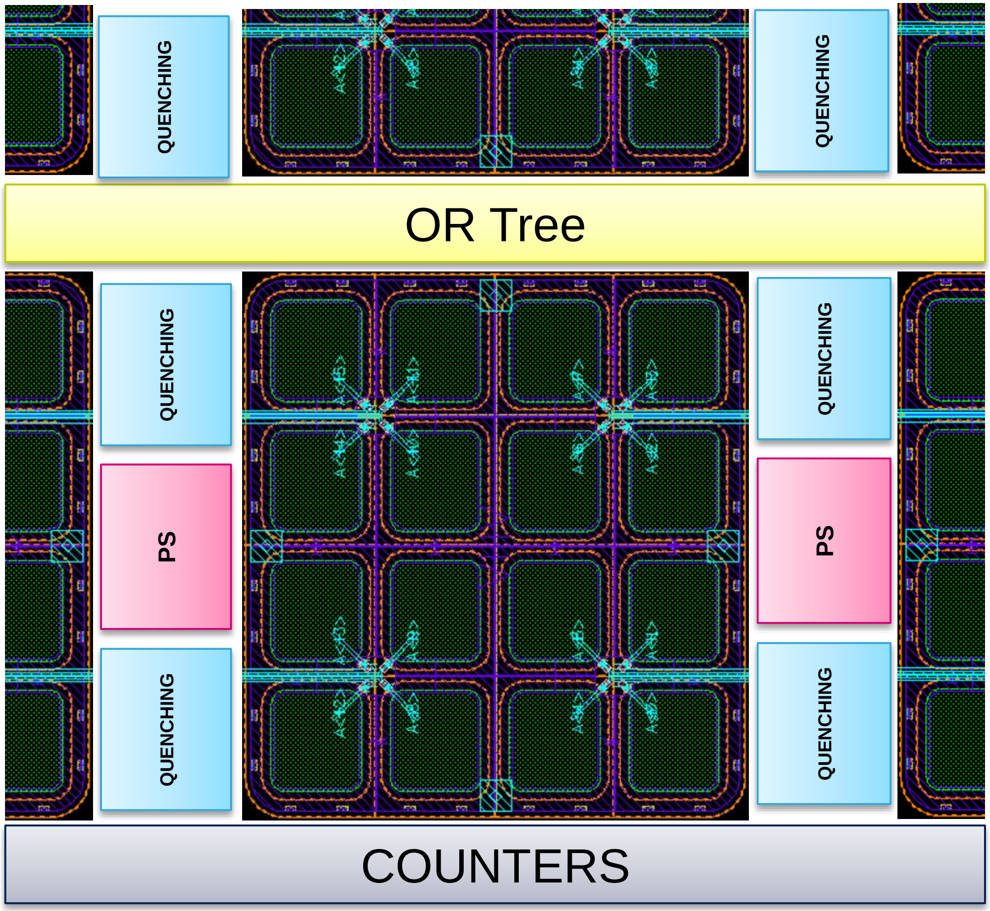
SPAD pixel

- 4 x 4 SPADs sharing NWELL
- Logic
  - individual quenching and enabling
  - pulse shaper
  - OR tree
  - counters
- Well sharing between neighbouring pixel is possible
- Varied configurations of the well sharing and surrounding circuit possible



SPAD pixel

- 4 x 4 SPADs sharing NWELL
- Logic
  - individual quenching and enabling
  - pulse shaper
  - OR tree
  - counters
- **Pixel fill factor ~ 40%**



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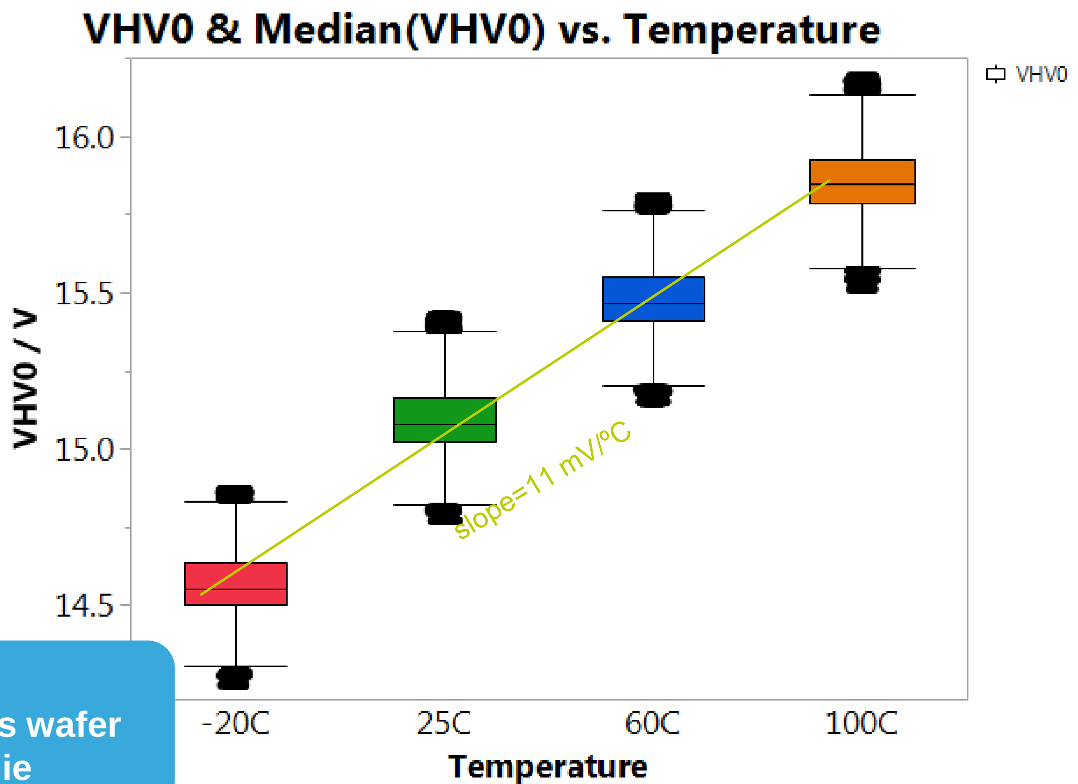
SPAD characterization

- Breakdown voltage (VHV0)
- Dark Count Rate (DCR)
  - Temperature dependence
  - Voltage dependence
  - Dark Count Rate distribution
- Photon Detection Probability (PDP)
- Timing Jitter
- Cross Talk

VHV0 vs Temperature

- VHV0 = Minimum reverse diode voltage required to produce pixel output pulse
  = Diode Reverse Bias Breakdown Voltage + Inverter Threshold Voltage



VHV0 @ 60°C = 15.5V
VHV0 Spread = ~0.10V stdDev across wafer
VHV0 Spread = 0.01V stdDev intra-die

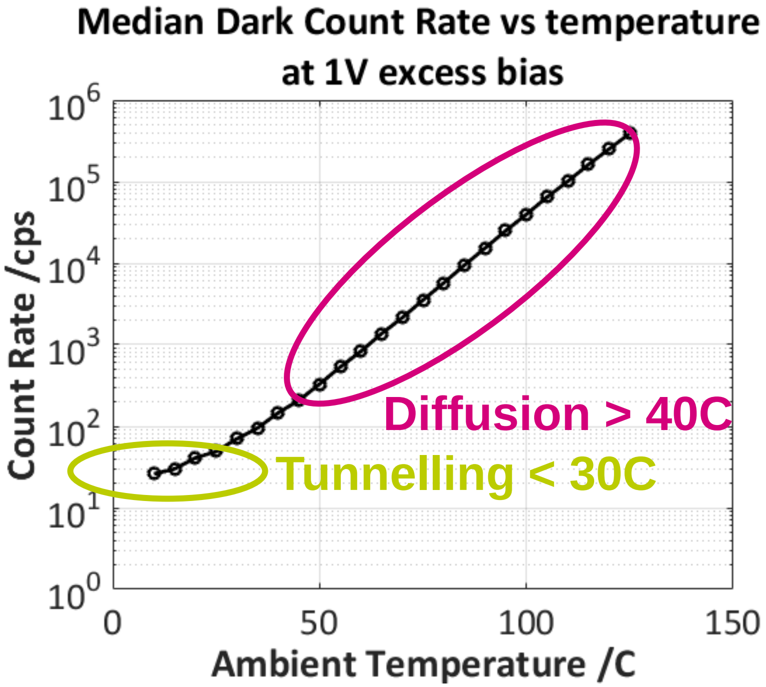
Dark Count Rate

- SPAD Dark Count Rate (DCR) is the main detector noise source. It is the count rate of the detector when no light impinges on it. DCR sources include:
    - Diffusion current
    - Tunnelling
    - Trap-assisted generation

Dark Count Rate vs Temperature

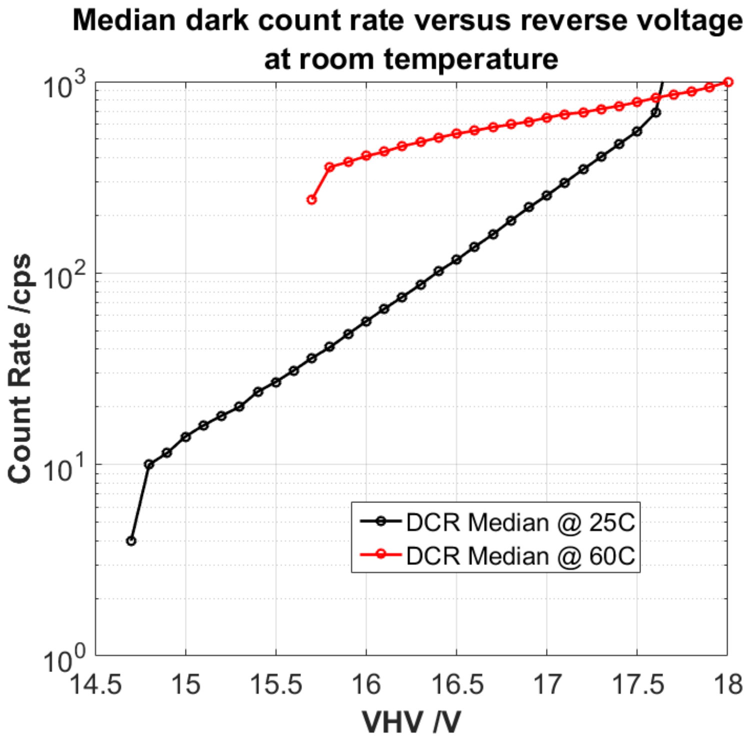
- Generation due to tunnelling has low temperature dependence

- DCR associated to diffusion has a doubling temperature of 7.6°C

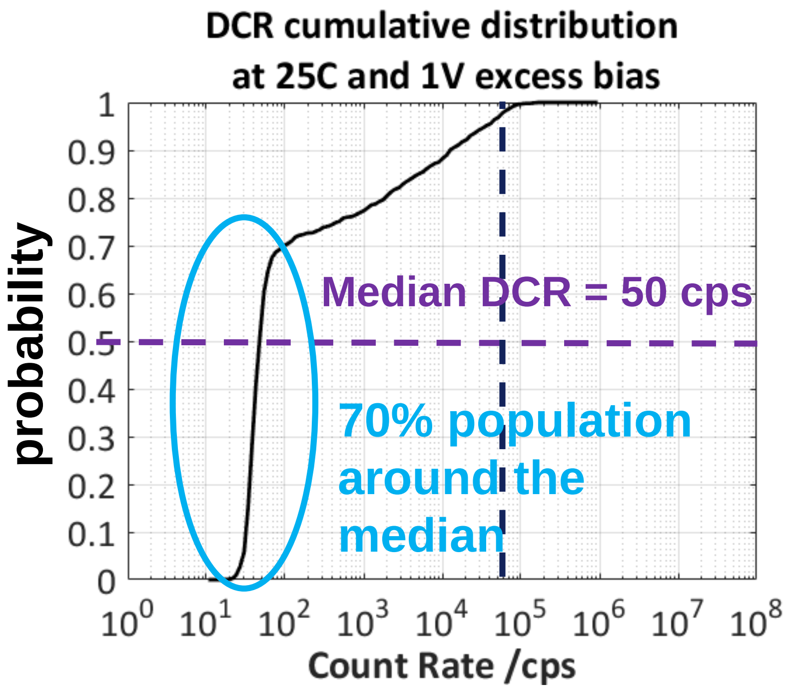


Dark Count Rate vs Reverse Bias

- At room temperature the increase is exponential due to tunnelling
- At 60C the dependence on VHV is linear, as avalanche multiplication dominates



Dark Count Rate Cumulative Distribution

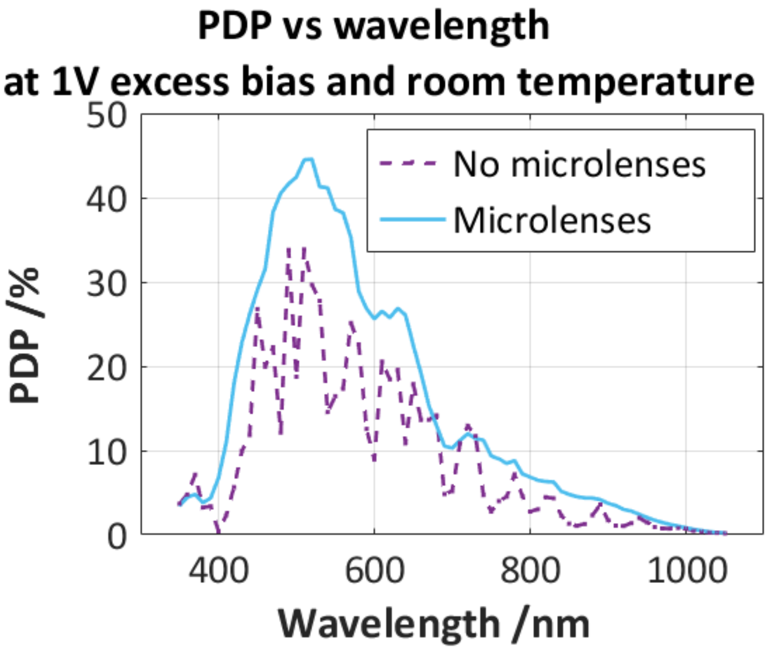


- Median DCR = 50 cps
  - at 25C and 1Vex
- 70 % of the population is around the median
- **60 kcps → yield > 95%**

Photon Detection Probability

- PDP is the probability of a photon impinging on the surface to trigger an avalanche in the SPAD

Photon Detection Probability



- Very strong oscillations due to nitride stack
- Microlenses increase PDP and smooth oscillations
- **PDP = 5% at 850nm**
  - This is the highest PDP value reported for industrial SPADs
- Process variability ~ ±15%

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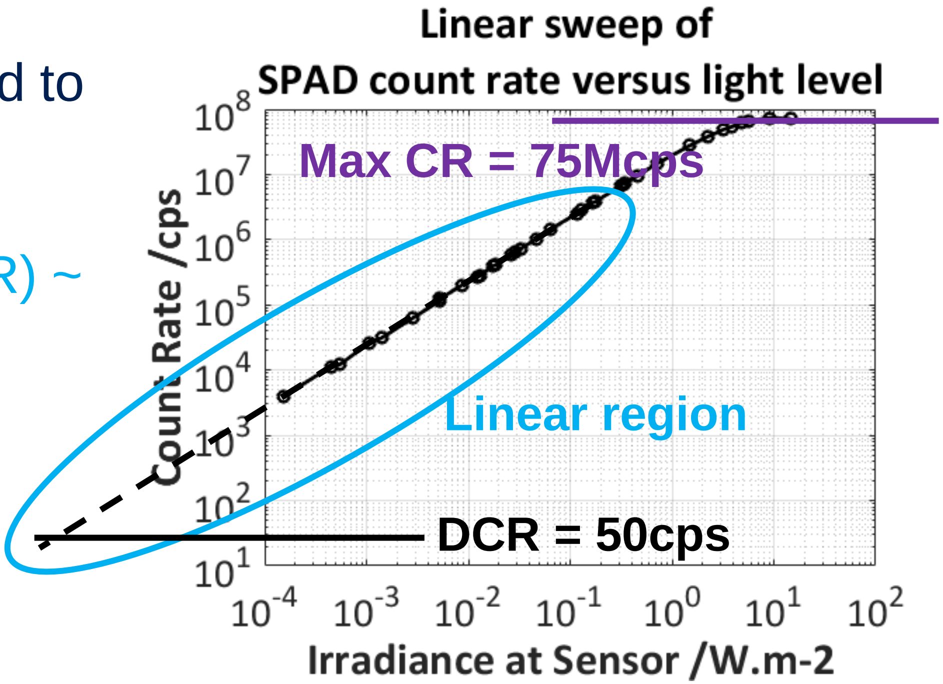
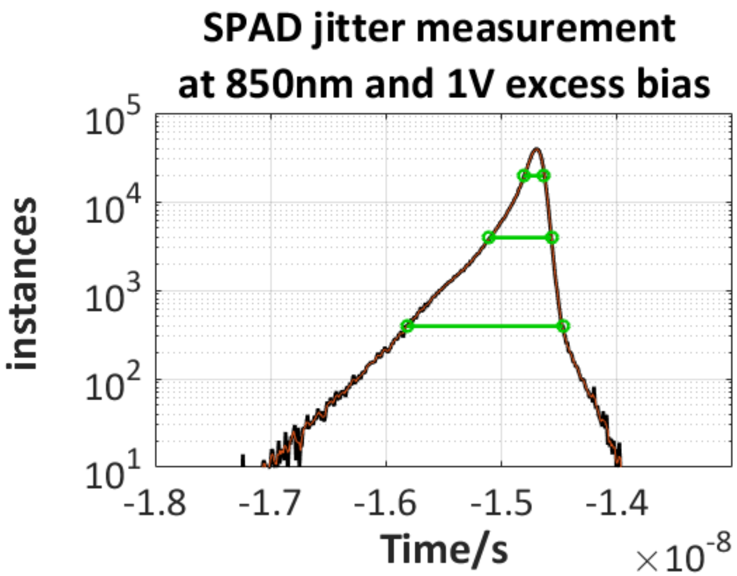
SPAD Dynamic Range

- Max CR = 150Mcps
- SPAD linearity is maintained to 15 Mcps
- Dynamic range (50cps DCR) ~ 6 orders of magnitude
- Dynamic range can be increased by grouping all SPADs using an OR Tree
  - Readout bandwidth limited



SPAD Pixel Timing Jitter at 850nm

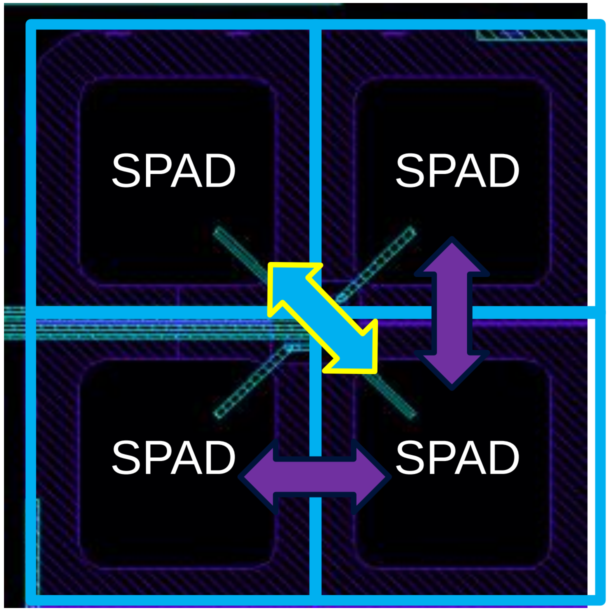
- SPAD time response ambiguity when illuminated with a very short laser pulse



- **FWHM = 140 ps**
- **FW10%M = 540 ps**
- **FW1%M = 1.3 ns**

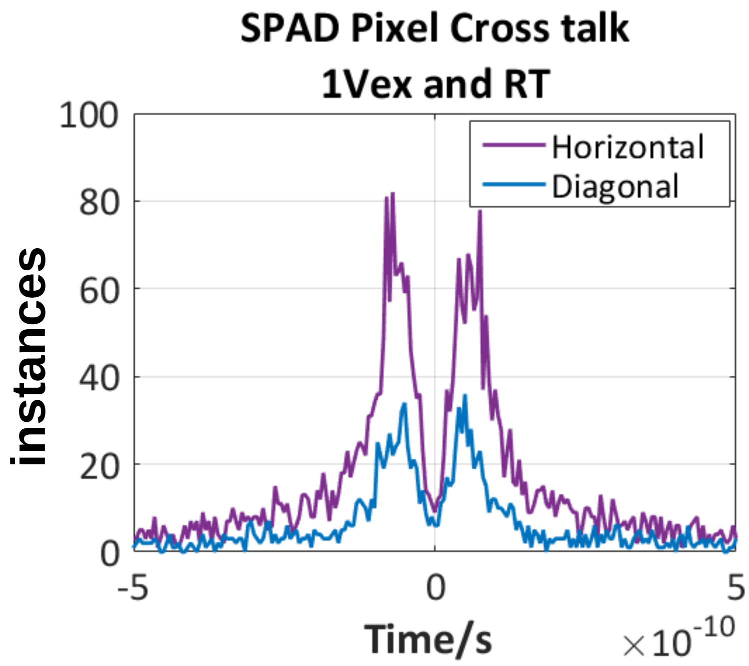
SPAD Pixel Cross Talk

- Cross talk is due to optical emission from avalanche in a SPAD to its neighbour
- **Horizontal and vertical** contribution are similar due to symmetry
- **Diagonal** will be smaller due to geometry



SPAD Pixel Cross Talk

- Cross talk is due to optical emission from avalanche in a SPAD to its neighbour
- **Horizontal and vertical < 2%**
- **Diagonal ~ 0.6%**



Summary performance table

Metric	IMG175SPAD Value (@ 60°C) [SPIE Photon Counting Conference]	40nm SPAD (@60°C)
VHV0	13.8V	15.5V
DCR Median	~1k cps	700 cps
PDP	3.1% (850nm)	5% (850nm)
SPAD Fill Factor	6%	>70%
Max Count Rate	37Mcps	150Mcps
Jitter	120ps FWHM, 870ps FW1%M	140ps FWHM, 1.3ns FW1%M
Current per Pulse	0.08pA	0.06pA
After-Pulsing	<0.1%	<0.1%
Cross-Talk	<0.01% (isolated SPAD)	<2% (Shared well)
Digital gate density		80% higher than 130nm CMOS
Power consumption		85% lower than 130nm CMOS

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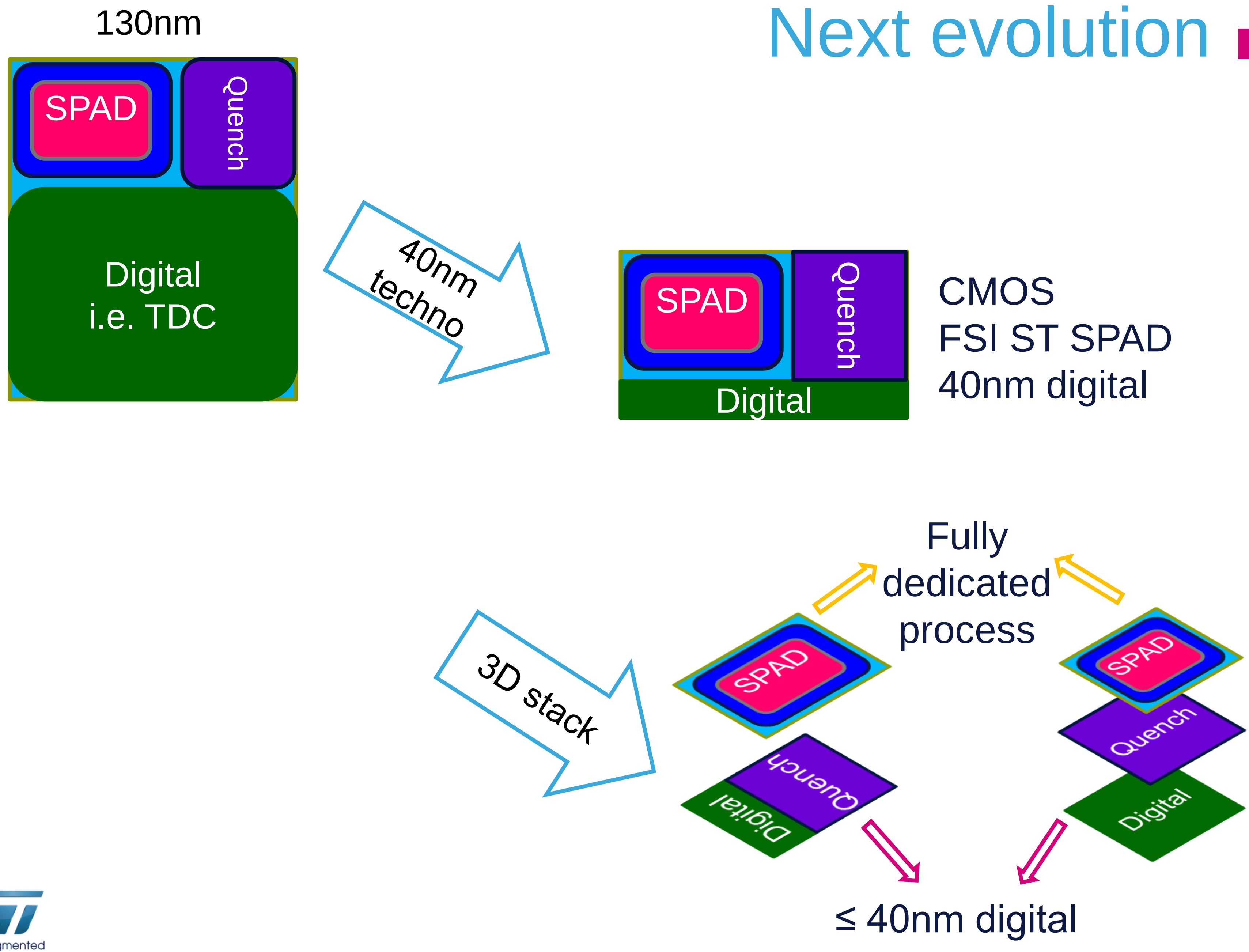
Next evolution



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